Vertex and Tracking Detectors for Future Lepton Colliders

VERTEX 2025 – 33rd International Workshop on Vertex Detectors

University of Tennessee, Knoxville
August 2025

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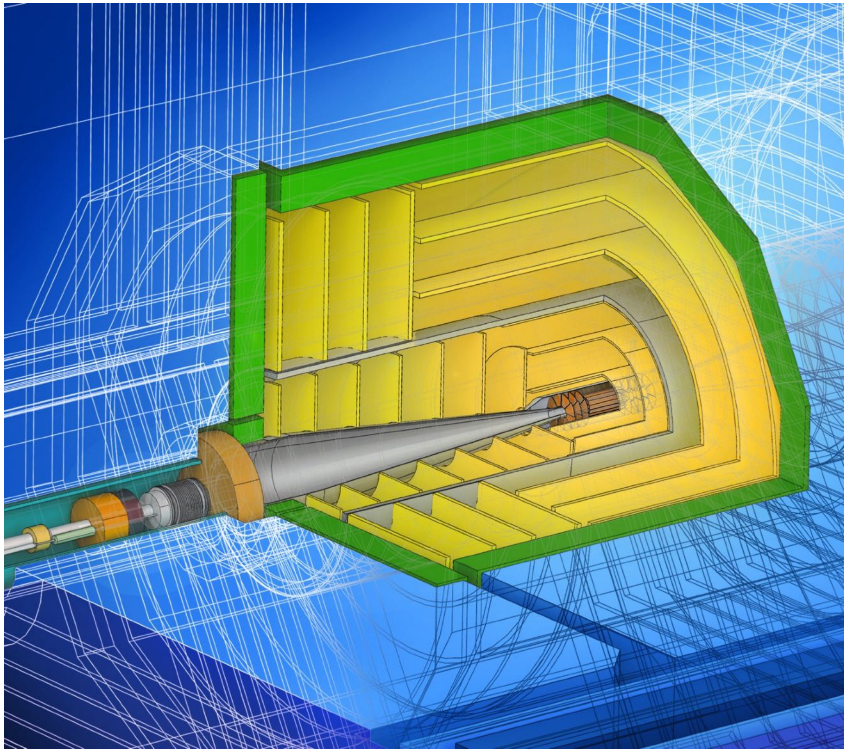
Outline

- Future e^+e^- Higgs Factories
- Vertex and tracker requirements
- Detector concepts
- Technology R&D examples
- Conclusions

Disclaimer:
Not a complete overview;
showing only few examples of the
many ongoing developments!

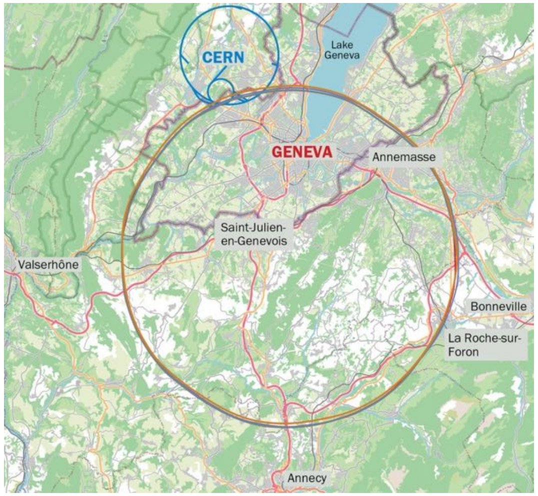


e^+e^- Higgs Factory proposals

- European Strategy Update for Particle Physics in 2025/26:
  - Higgs Factory highest-priority post-LHC project
  - No decision yet about which and where
- Several e^+e^- collider Higgs-Factory proposals:
  - $\sqrt{s}$ ~ 350 GeV - 3 TeV
  - Circular / linear collider designs
  - Possible sites in Europe and Asia
  - Time scale ~2045

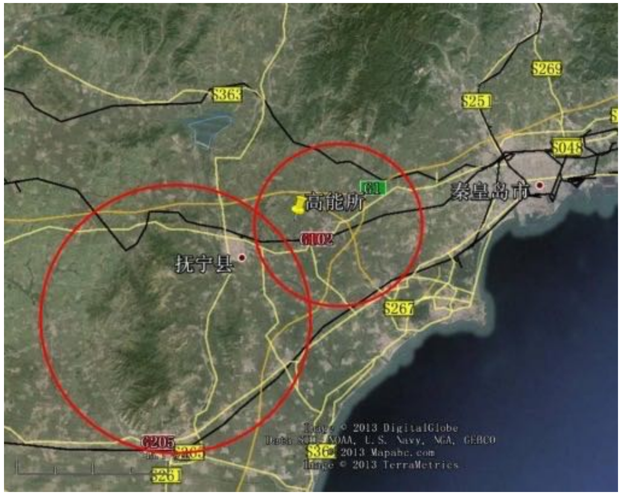
FCC-ee @ CERN

$\sqrt{s}_{max}$ =240-365 GeV



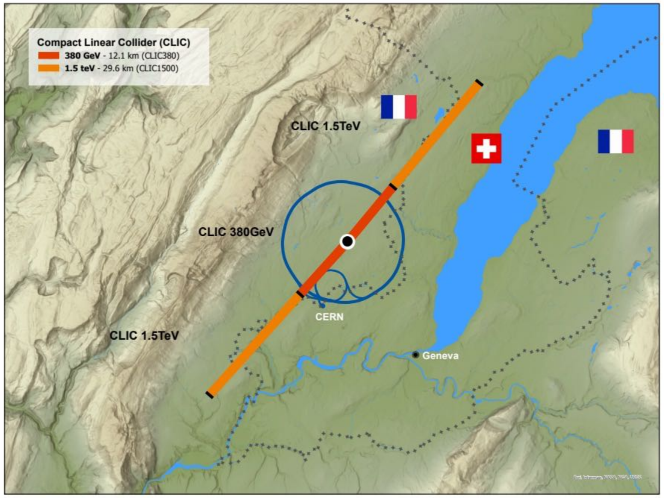
CEPC in China

$\sqrt{s}_{max}$ =240-360 GeV



CLIC / LCF @ CERN

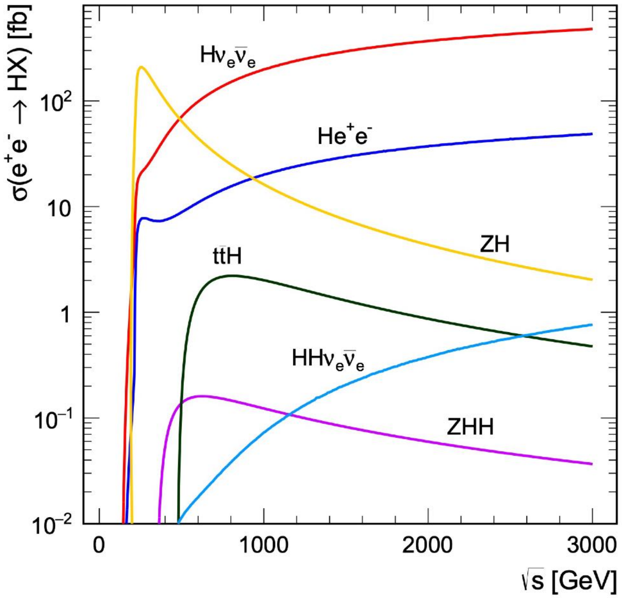
$\sqrt{s}_{max}$ =380 GeV – 1.5 TeV (3 TeV)



Higgs Factory vertex/tracker physics requirements

- Physics goals for post-LHC future Lepton Colliders:
  - Precision Higgs / EW / top measurements
  - Direct/indirect BSM searches

Higgs production processes



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  - Flavour tagging (c, b), life-time measurements

→Vertex resolution: $\sigma(d0)\sim 5\oplus 15/(p[\mathrm{GeV}]\sin^{3/2}\theta)$ μm

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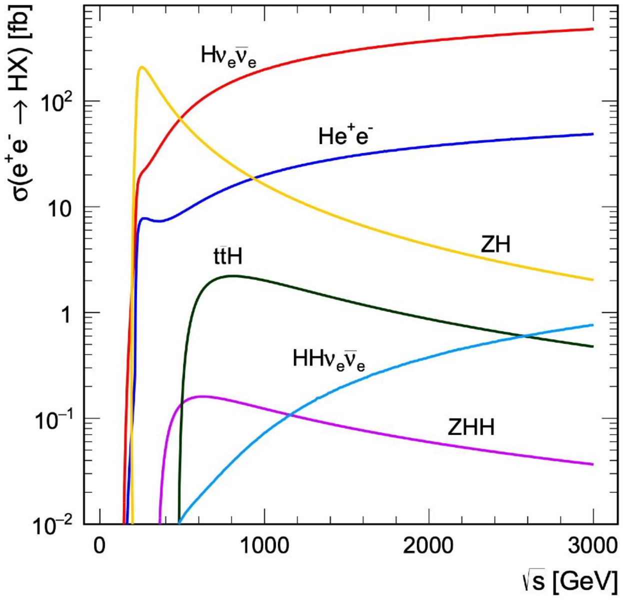
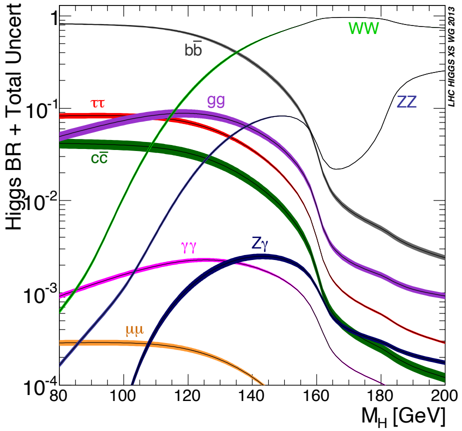


Higgs branching ratios



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  - Precise measurement of leptonic final states (e.g. recoil-mass measurement in ZH)

  →Track-momentum: $\sigma(p_T) / p_T^2 \lesssim 2 \times 10^{-5}$ GeV^{-1}

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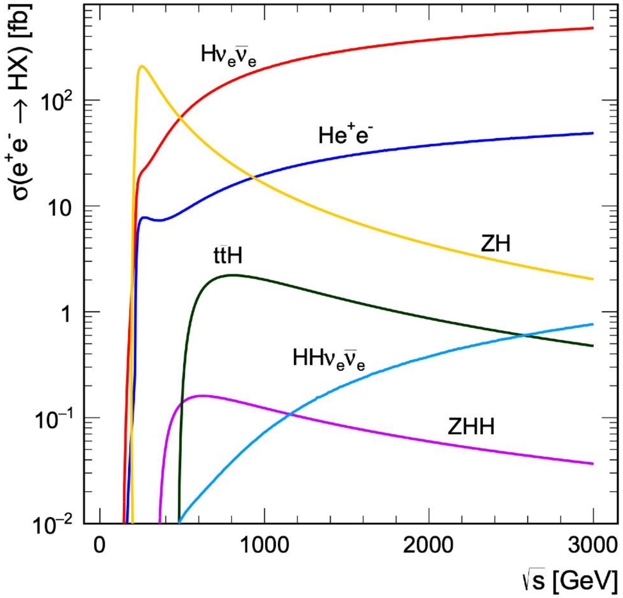

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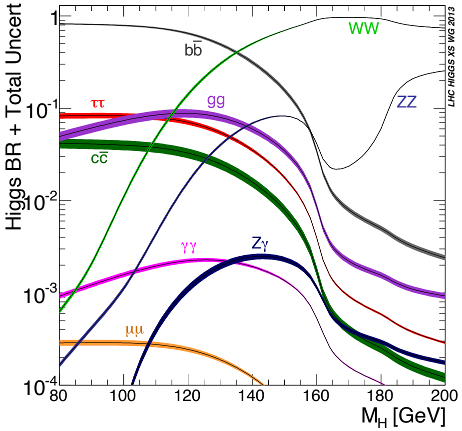
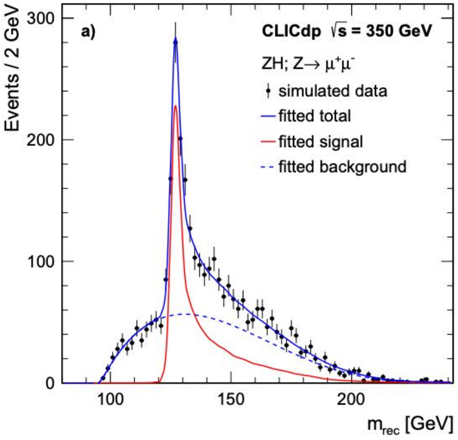


Higgs recoil mass reconstruction



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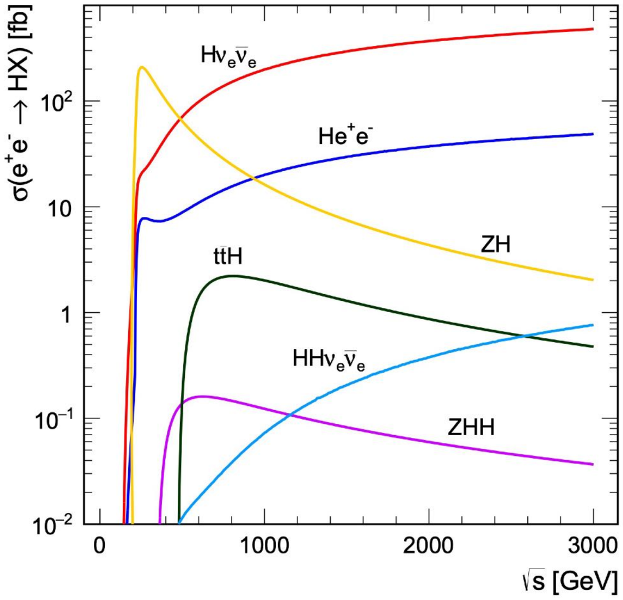
  - Heavy-flavor physics → PID (K/pi separation) by dE/dx, dN/dx and/or 10’s of picosecond timing layers
  - Background rejection → low-angle coverage, timing
  - Exotics (e.g. highly ionizing or feebly coupled particles)

  → dE/dx, many layers, large radius, precision timing

Higgs production processes



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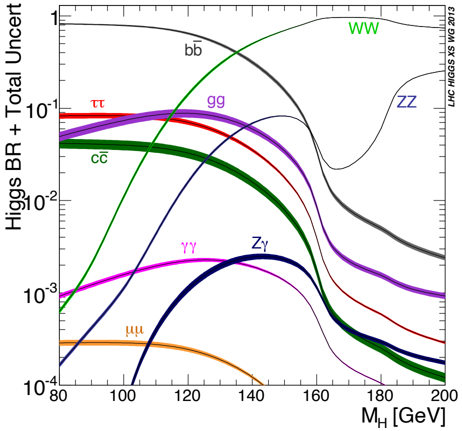

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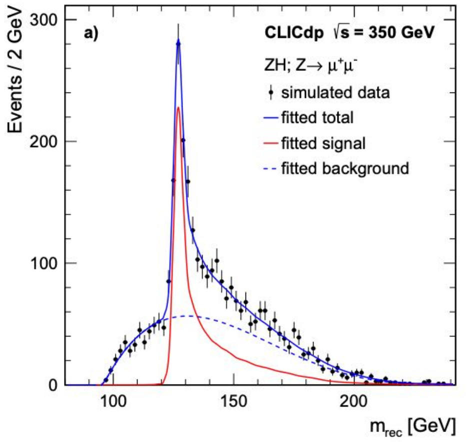
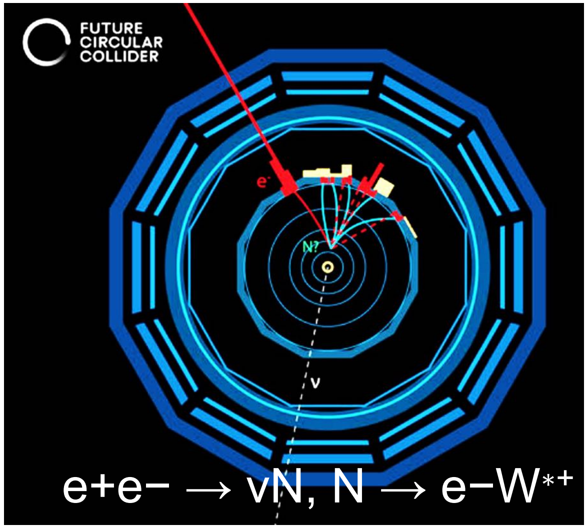


Decay of Heavy Neutral Lepton (1m from IP)



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  - Back
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- Similar physics requirements for trackers in all collider concepts
- More focus on asymptotic position resolution for high-energy Linear-Collider stages
- More focus on material budget and particle ID (dE/dx, dN/dx, ToF) for high-luminosity low-energy Circular-Collider stages

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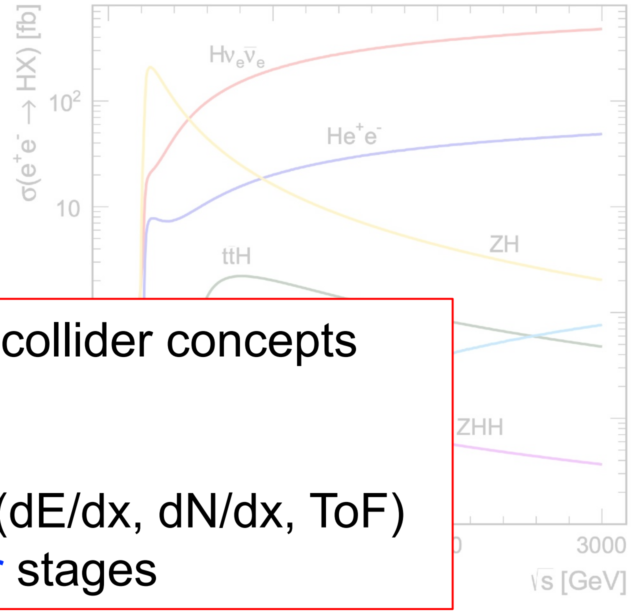

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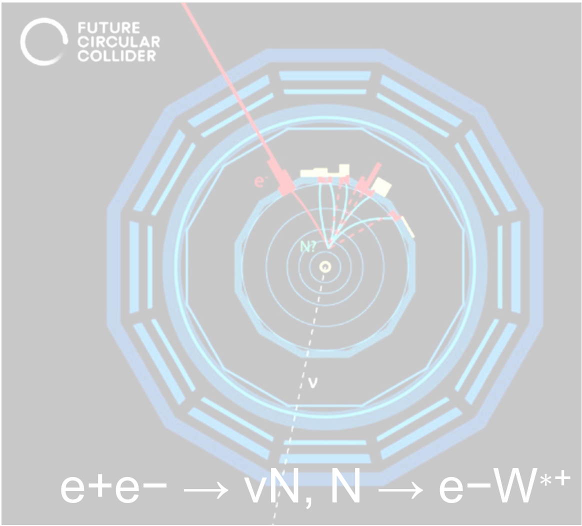

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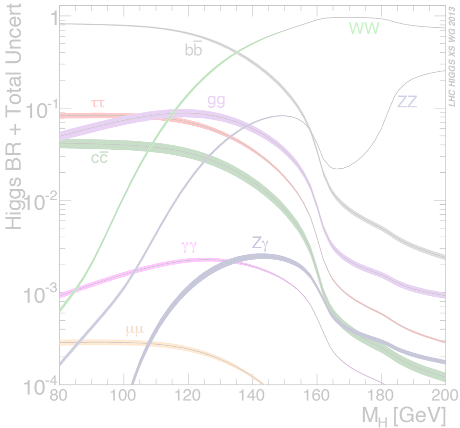

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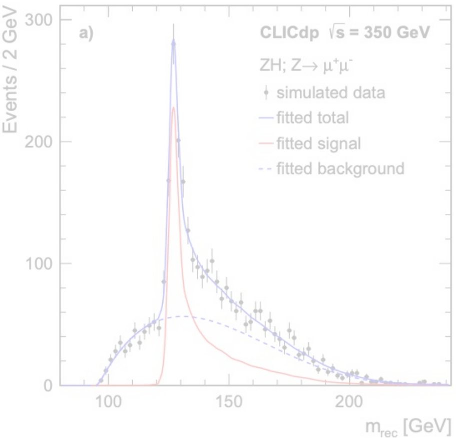


Experimental constraints on vertex/tracker

Main experimental constraints in **linear lepton colliders**:

- Significant rates of beam-induced backgrounds (incoherent e^+e^- pairs, $\gamma\gamma \rightarrow$ hadrons):
  - Constrains layout, granularity, impacts physics
- Backgrounds concentrated in very short bunch trains

→ High instantaneous hit rates (up to 6 GHz/cm^2 @ 3 TeV CLIC)

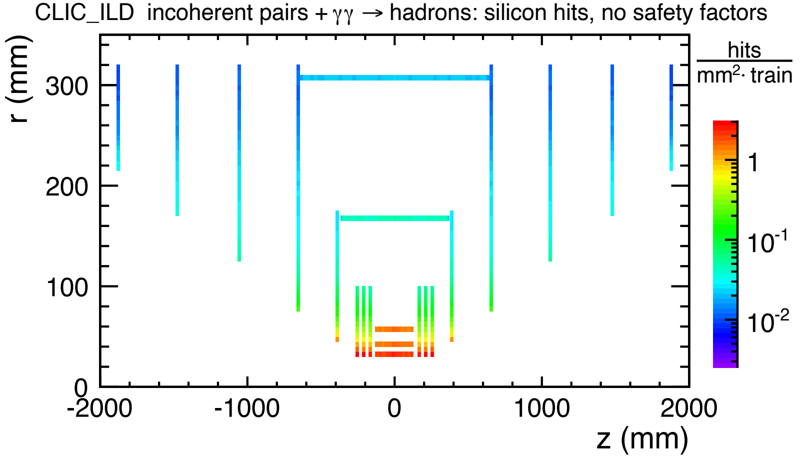
→ Time-stamping: few ns @ 3 TeV CLIC, ~1-10 µs @ LCF

→ Fast detector signals / frontend

- Low duty cycle: ~20-200 ms gaps between bunch trains

→ trigger-less readout, pulsed powering

CLIC backgrounds in tracking region



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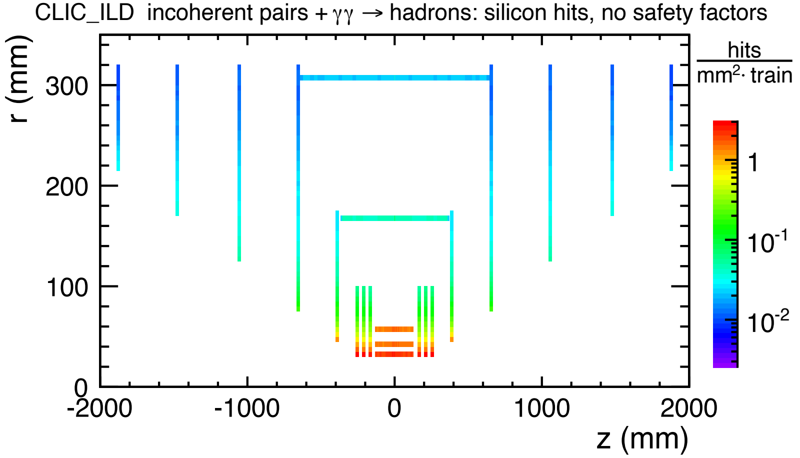


Main experimental constraints in **circular lepton colliders**:

- 30 mrad crossing angle of beams, focusing quadrupoles inside det. volume

→ B-field limited to ~2 Tesla

- High rate of physics events (up to 100 kHz, bunch spacing down to 30 ns)

→ Integration time <~1 μs required for occupancy and pile-up (30 ns @ Z-pole)

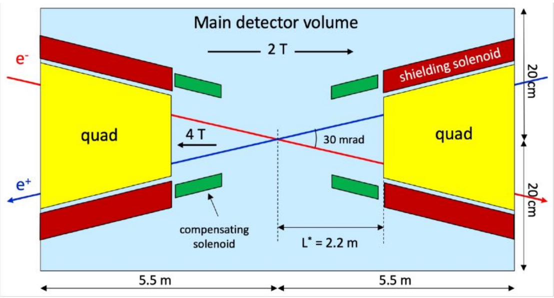
→ Fast detector frontend and DAQ

- Main backgr.: synchr. rad. (requires shielding), incoh. pairs (up to ~200 MHz/cm²)
- Continuous collisions (100% duty cycle)

→ Beam-induced backgrounds more spaced out, less severe impact on detectors,

→ Pulsed powering not possible

FCC-ee detector region



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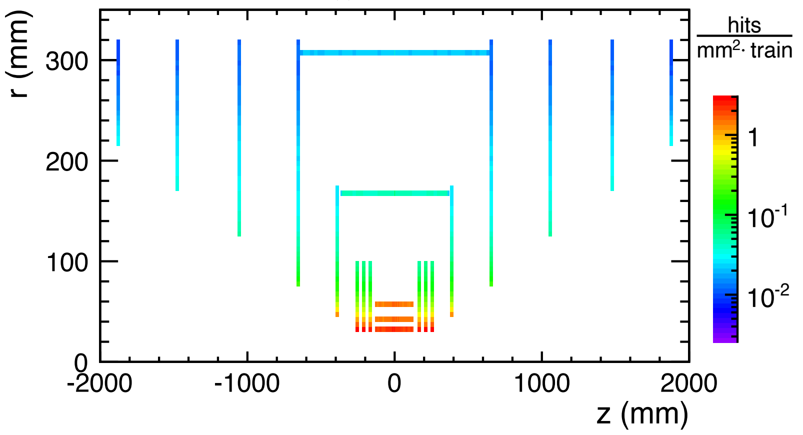

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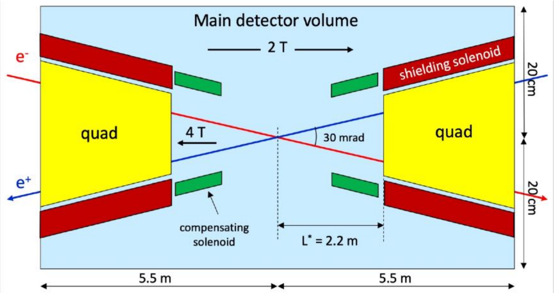


Moderate radiation exposure for all lepton-collider proposals:

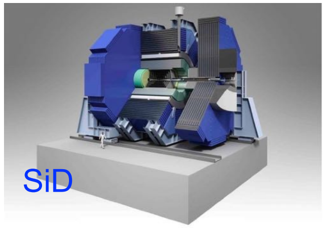
- NIEL: < 10^{14} $n_{eq}/cm^2/y$
- TID: < 100 kGy / year

Vertex/tracking detector concepts

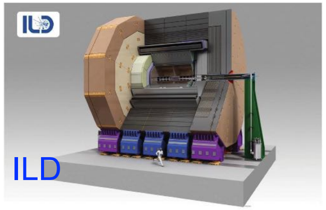
Collider	**LCF**		**CLIC**	**FCC-ee**				**CEPC**	
Detector Concept	SiD	ILD	CLICdet	FCC-ee ILD	CLD	FCC-ee IDEA	ALLEGRO	CEPC baseline	CEPC IDEA
B-field [T]	5	3.5	4	3.5	2	2	2	3	2
Vertex inner radius [mm]	14	16	31	16	17 → 12	17 → 12	17 → 12	16	16
Tracker out. radius [m]	1.25	1.8	1.5	1.8	2.2	2.0	2.0	1.81	2.05
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
Tracker	Si-strips	TPC/ Si-strips	Si-pixel	TPC/ Si strips	Si-pixel	DC/ Si-strips	DC/Si-strips or Si-pixel	TPC/Si-strips or Si-strips	DC/ Si-strips

https://europeanstrategyupdate.web.cern.ch/sites/default/files/Submitted_Input_2025.05.26.pdf

arXiv:1811.10545

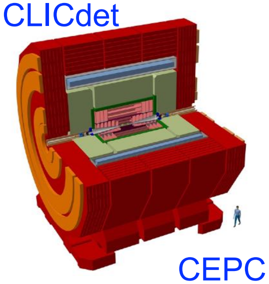


SiD

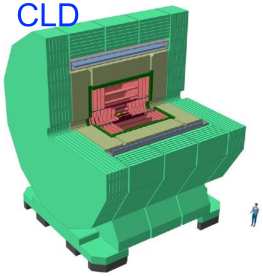


ILD

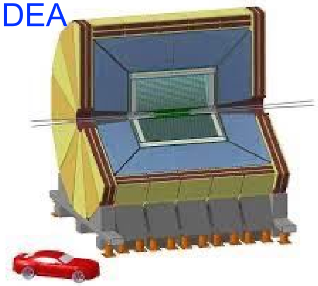
CLICdet



CLD

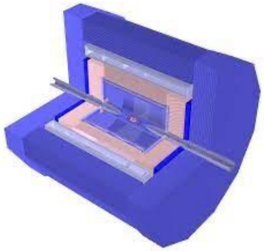


IDEA



ALLEGRO

CEPC baseline



Vertex/tracking detector concepts

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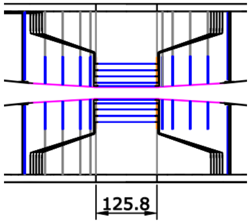
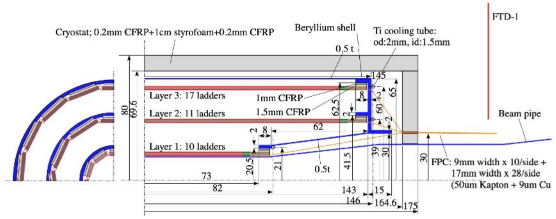
arXiv:1811.10545

All concepts contain silicon-pixel vertex detectors:

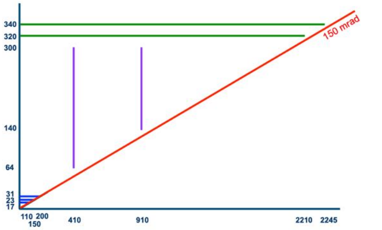
- 5-6 barrel and up to 6 endcap layers (in doublets or singlets)
- high single point resolution per layer: σ_{SP}~3 μm → pixel sizes <~25 μm2
- low material budget: $\lesssim$ 0.2% X_0 / layer (equivalent to ~200 μm silicon) → thin sensors, low-power ASICs for air cooling (~50 mW/cm^2)

SiD vertex-detector

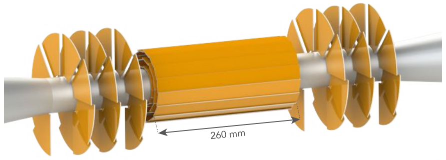




IDEA vertex-detector



CLIC vertex-detector



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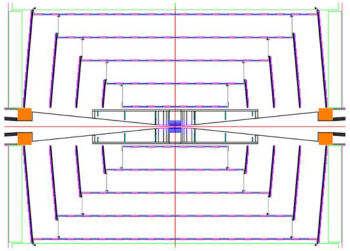
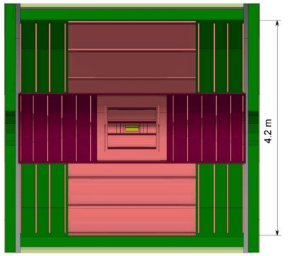
Silicon-based large-area trackers:

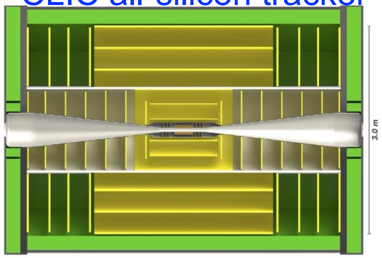
- many layers (barrel/endcap), large outer radius (scaling with B field)
- Large pixels or strip detectors
- ~7 µm single-point resolution in bending plane
  → ~25-50 µm Rφ pitch
- ~1-2% X0 per layer
  → low-mass supports + services,
  low power ~150 mW/cm^2



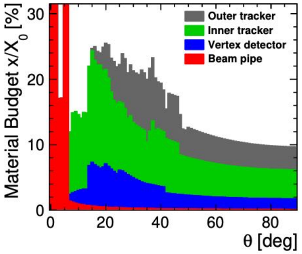
CLD all-silicon tracker



CLIC all-silicon tracker

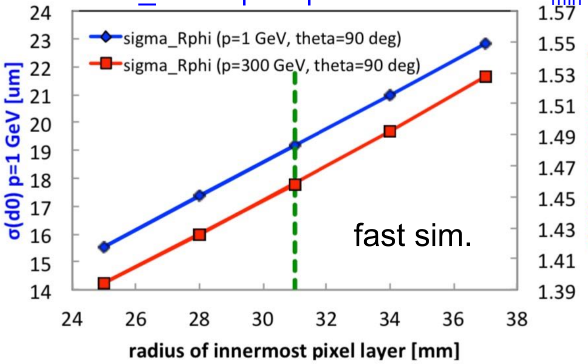


CLIC inner det. mat. budg.

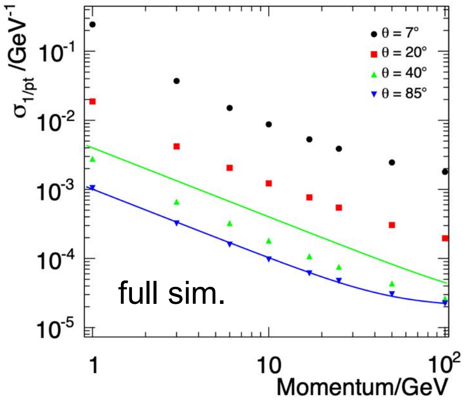


Detector concept optimization / validation

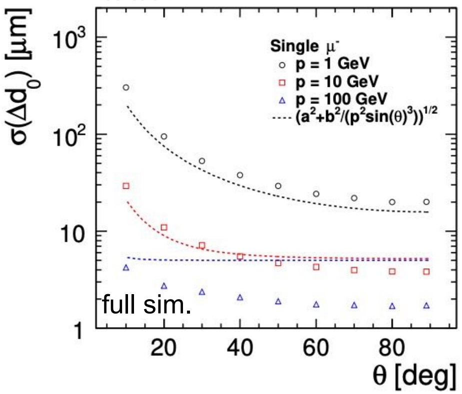
CLIC_ILD Impact-param. resol. vs. R_{min}



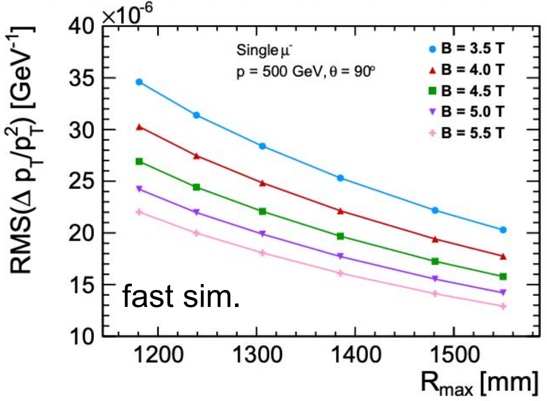
ILD momentum resolution



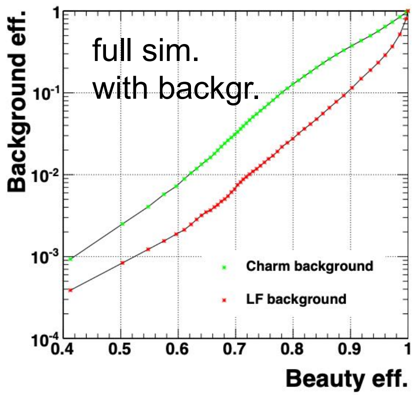
CLD d_0 resolution



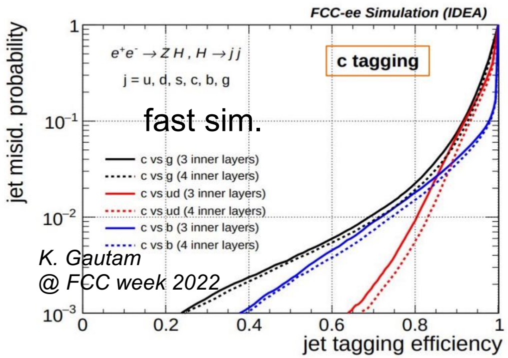
CLICdet momentum resol. vs. B-field and R_{max}



SiD b-tagging performance



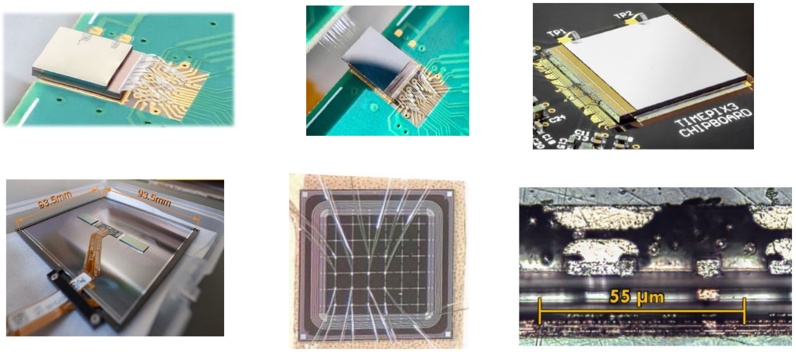
IDEA c-tagging performance



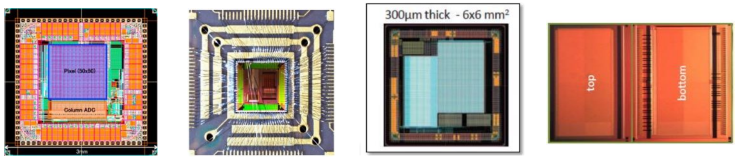
- Detecor concepts are optimised with fast parametric and full Geant-4 simulations;
- All detector concepts fulfil physics requirements in simulations;
  - So far: SiD,ILD,CLICdet,CLD validated in Geant4 based full-detector simulations
  - Other concepts validated in fast simulation, full simulation in progress
- All concepts contain 4π trackers with barrel+endcap → similar to ATLAS, CMS, *ALICE3,* but different from Belle, ALICE ITS3, Mu3e with their barrel-only inner trackers

Silicon pixel-detector R&D

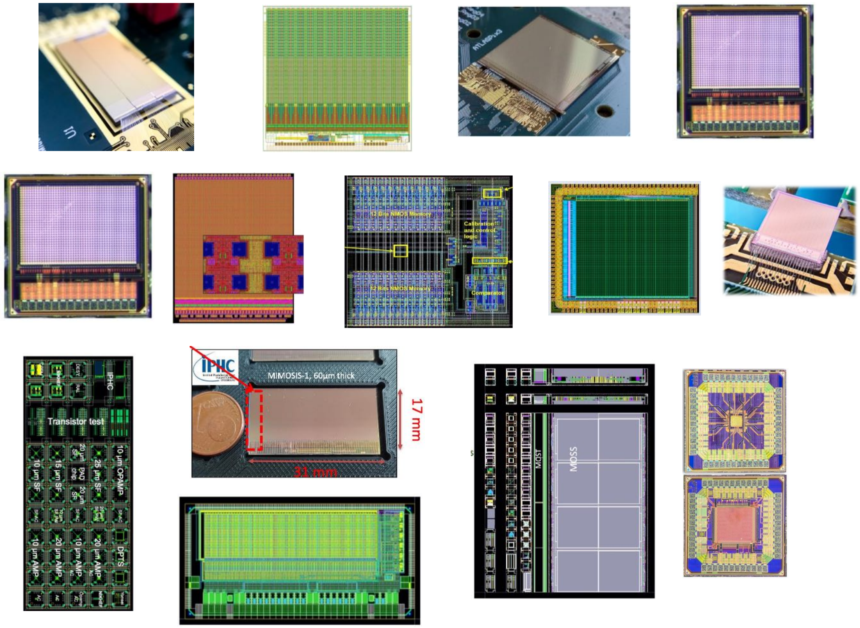
Hybrid detectors



Silicon on Insulator

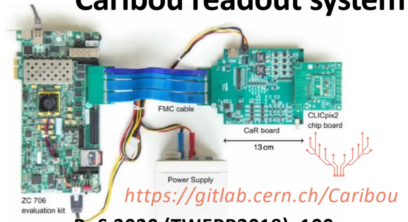


Monolithic Sensors



Tools

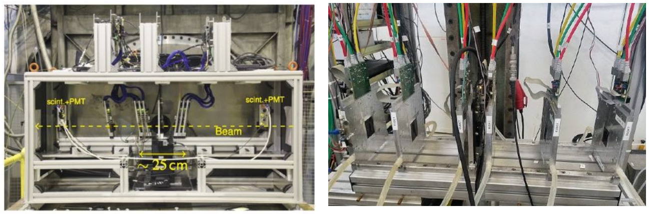
Caribou readout system



https://gitlab.cern.ch/Caribou

PoS 2020 (TWEPP2019), 100

CLICdp + AIDA telescopes



MC Simulation framework: Allpix Squared

https://gitlab.cern.ch/allpix-squared/allpix-squared

NIM A 901 (2018) 164-172

Analysis & reconstruction framework: Corryvreckan

https://gitlab.cern.ch/corryvreckan/corryvreckan

2021 JINST 16 P03008

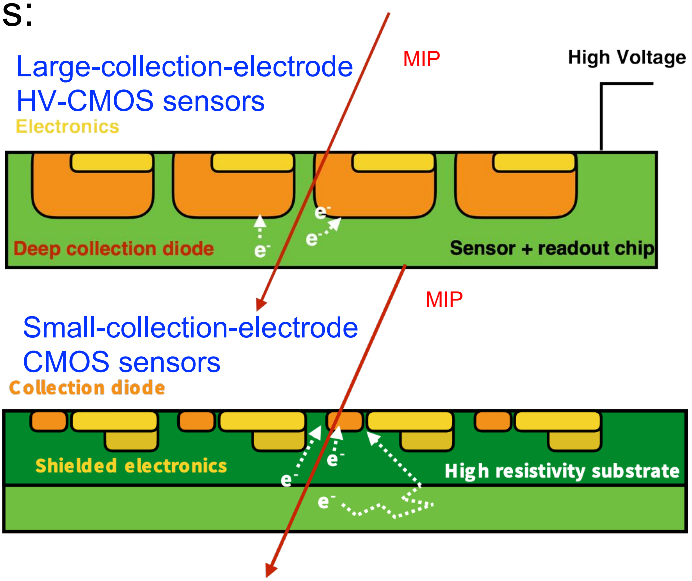
- Diverse R&D performed within various collaborative frameworks (ILD, SiD, CLICdp, IDEA, CERN EP R&D, AIDAinnova, DRD3/7), with strong links to other developments (HL-LHC, Belle II, Mu3e, CBM@FAIR, ALICE ITS3, …)
- Mostly focusing on conceptual studies + technology demonstrators

→ Flexible tools developed, to support the R&D and exploit synergies between the various R&D lines

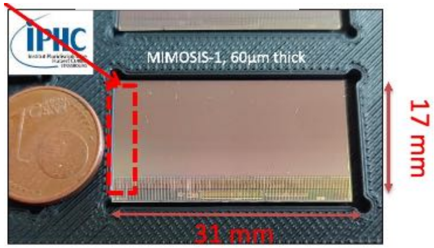
Monolithic CMOS sensors

Monolithic CMOS sensors using (adapted) industry technologies:

- Sensor and readout electronics fully integrated
- Different concepts:
  - Large-collection electrode High-Voltage (HV-CMOS) for large + fast signals, radiation hardness
  - Small-collection-electrode designs for low capacitance, high signal/noise, low power
- Simplified construction (no bonding)
- Challenges: complex non-uniform sensor structures (simulation), interplay sensor/readout, process modifications are foundry dependent / parameters not publicly available
- Many ongoing developments, exploiting progress in semiconductor industry and synergies (HL-LHC, Mu3e, Belle II, CBM@FAIR, ALICE ITS3, …)
- Trend towards smaller feature sizes (180 nm → 65 nm) for improved performance
- Target: vertex/tracker of all Higgs Factory detectors

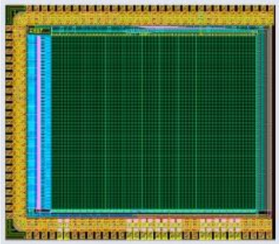


MIMOSIS-1
180 nm CMOS

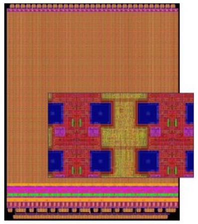


CLICTD
180 nm CMOS

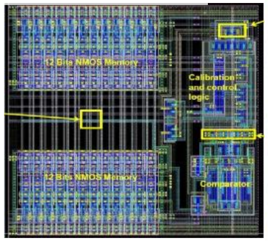
JadePix2
180 nm HV-CMOS



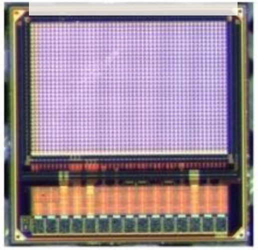
ARCADIA MD1
110 nm CMOS



Chronopix
90 nm CMOS

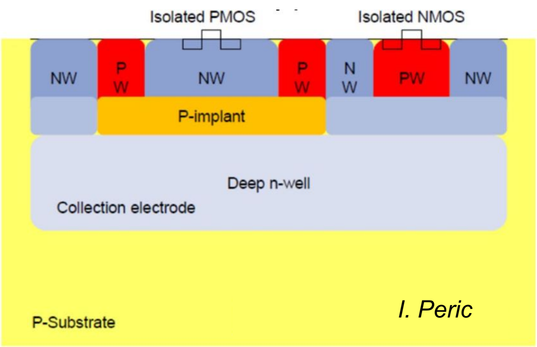


CE-65
65 nm CMOS



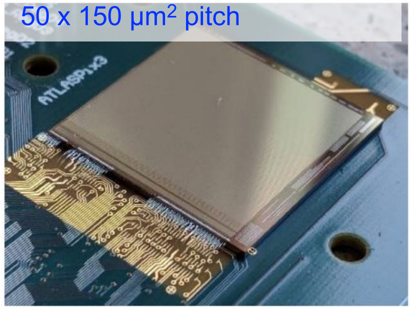
180 nm High-Voltage CMOS

- Active HV-CMOS sensors with fully integrated readout
- Large collection electrode shielding CMOS circuitry, depleted thin sensors (high-resistivity substrates, >100 V bias), fast frontend
  → large signal (dE/dx), fast, radiation hard
- Studies for CLIC tracker + IDEA outer vertex / tracker
- Same technology initially considered for ATLAS outer tracker and chosen for Mu3e tracker (MuPix8), also under study for LHCb Mighty Tracker upgrade and for DESY beam-telescope timing+trigger planes
- Very good performance observed in test beam:
  - >99.7% efficiency (ATLASpix3)
  - Timing precision ~4 ns (ATLASpix3)
  - Spatial resolution <10 µm (Telepix, 25 µm pitch in R/phi)
  - Power consumption down to 140 mW/cm^2 (ATLASpix3)
- Plans for dedicated CEPC design in 55 nm HV-CMOS process

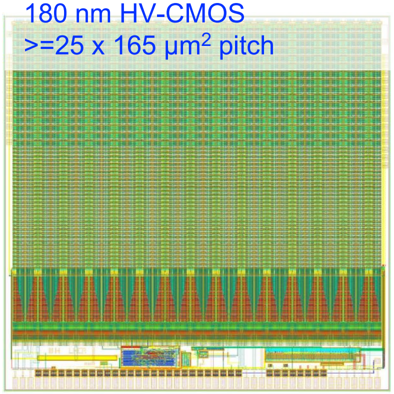


I. Peric

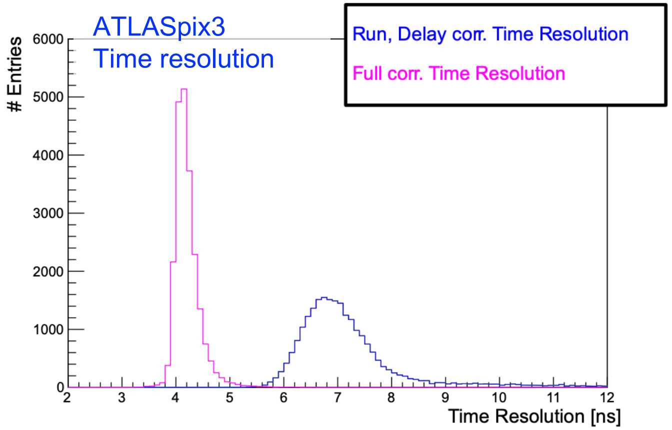
ATLASpix3
180 nm HV-CMOS
50 x 150 µm^2 pitch



LHCb/CLIC/Telepix
180 nm HV-CMOS
>=25 x 165 µm^2 pitch

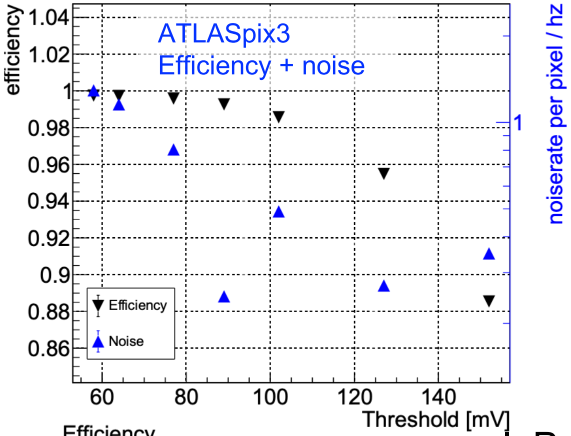


ATLASpix3
Time resolution



Time resolution (RMS) for every pixel
Uncorrected 6.7ns +- 0.5ns
ToT corrected 4.1ns +- 0.1

ATLASpix3
Efficiency + noise



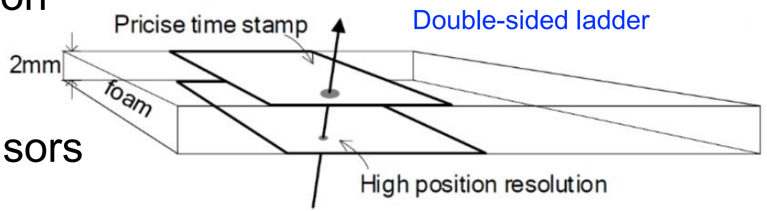
Efficiency

I. Peric et al.

https://agenda.linearcollider.org/event/9211/contributions/49477/

180 nm small-collection-electrode CMOS (I)

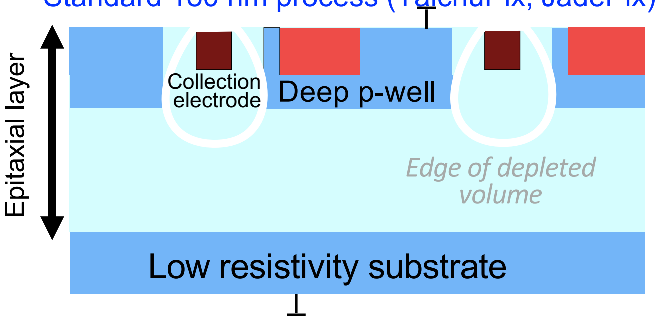
Several ongoing developments targeting Higgs-factory vertex detectors with separate layers for timing (~1 µs) and position resolution (<=3 µm)



TaichuPix and JadePix (IHEP et al.) 180nm monolithic sensors

- Standard 180 nm CMOS imaging process with small-collection electrode + high-resistivity epitaxial layer
- Main target: CEPC vertex detector
- Several prototypes, focusing on different aspects (spatial resolution, data rates, timing, full-scale tests)

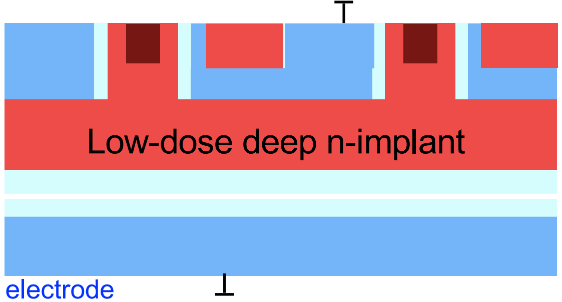
Standard 180 nm process (TaichuPix, JadePix)



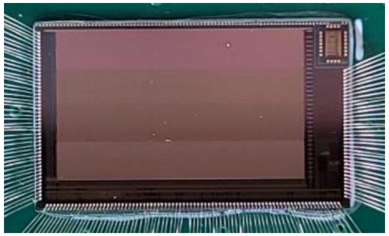
MIMOSIS (IPHC)

- 180 nm CMOS imaging process with small-collection electrode + high-resistivity epitaxial layer + modifications for improved performance, including AC coupled electrodes
- Main target CBM@FAIR, in the future: LCF vertex detector
- Evolution of monolithic sensors since 1999, used in various experiments (EUDET telescopes, STAR-PXL, ALICE-ITS2)

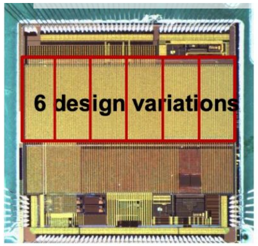
Modified 180 nm process (MIMOSIS)



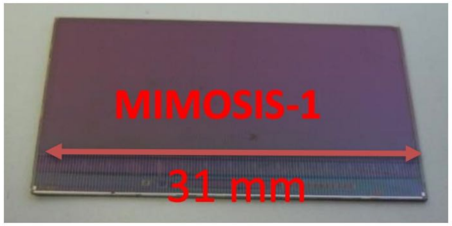
JadePix 3



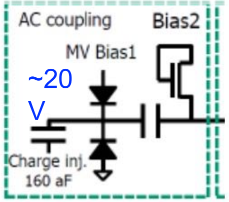
TaichuPix 2



MIMOSIS-1



AC-coupled electrode



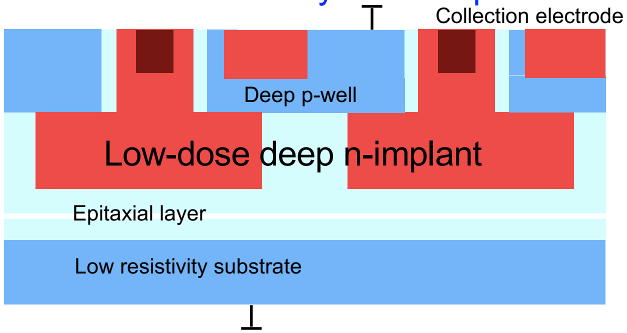
→ Presentation on MIMOSIS by Ajit Kumar in next session

180 nm small-collection-electrode CMOS (II)

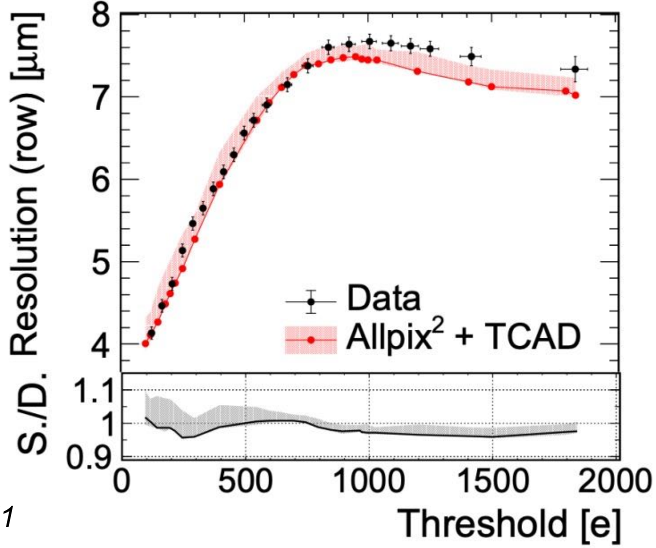
CLICTD 180nm monolithic sensor

- Modified 180 nm CMOS imaging process with small-collection electrode
- Target: CLIC tracker
- Innovative sub-pixel segmentation, Channel pitch: (8 x 37.5) µm x 30 µm
- Simultaneous time and energy measurement per channel
- Exploring large parameter space of sensor-design modifications, substrate materials (epitaxial, high-resistivity Czochralski) and thicknesses (40-300 µm), in collaboration with ATLAS MALTA / STREAM
- Detailed TCAD/Geant4-based simulations (Allpix^2), validated with test-beam data

CLICTD sensor layout example



CLICTD spatial resolution in TB and simulation



	Required (CLIC tracker)	Epi	Cz*
Spatial resolution (transv.)	< 7 µm	4.6 µm	4.3 µm
Time resolution*	~ 5 ns	5.2 ns*	4.4 ns*
Efficiency	> 99.7 %	> 99.7 %	> 99.7 %
Material content	< 200 µm	40 - 100 µm	100 µm

IEEE TNS 67.10 (2020): 2263-2272
NIM A 1006 (2021) 0165396
NIM A 1041 (2022) 167413

K. Dort, CERN-THESIS-2022-071

- Excellent performance observed in test-beam measurements and reproduced by simulations
- Validated simulations used for parameter extraction
- Results have served as input to sensor optimization, also for 65 nm process

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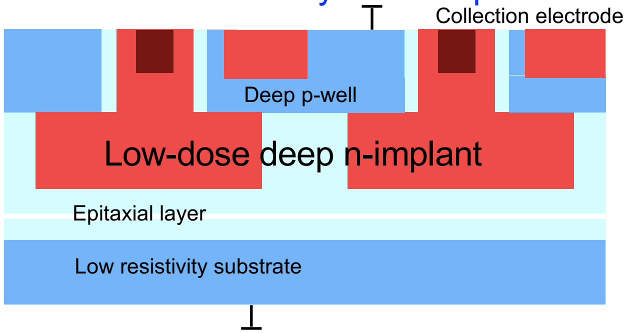
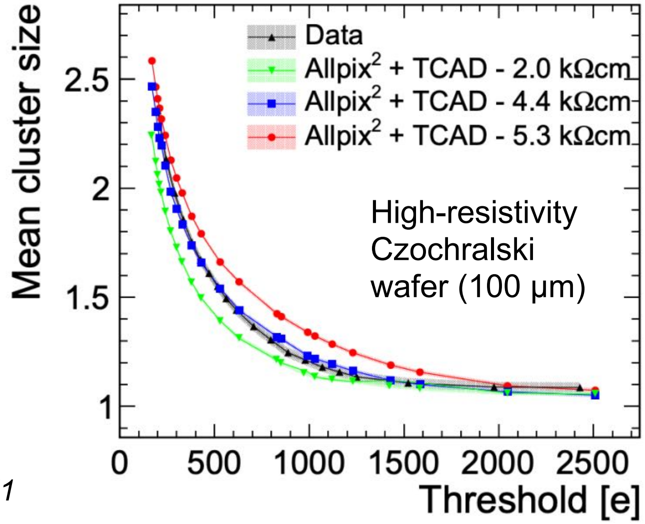
CLICTD sensor layout example



CLICTD cluster size in data and simulation



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- Validated simulations used for parameter extraction
- Results have served as input to sensor optimization, also for 65 nm process

65 nm monolithic CMOS (I)

TPSCo 65 nm ISC CMOS imaging process validation for HEP

- 10 µm epitaxial layer, 7 metal layers, 300 mm wafers with stitching
- Collaboration CERN EP R&D, ALICE ITS3, DRD3/7, many institutes + other projects
- Smaller feature size → smaller pixels (~10-35 µm), enhanced performance
- Candidate technology for several Higgs-Factory vertex/tracker developments
- Encouraging results from MLR1 and ER1 runs in 2021/22:
  - Common submission of technology demonstrators from various groups
  - Stitched sensors (MOSS/MOST) for ALICE ITS3
  - Successful large-scale testing + simulation campaigns
  - Process modifications and sensor-design optimizations proven to work as expected

  → Full efficiency, <100 ps sensor timing for optimized designs, up to 10^{15} n_{eq}/cm^2

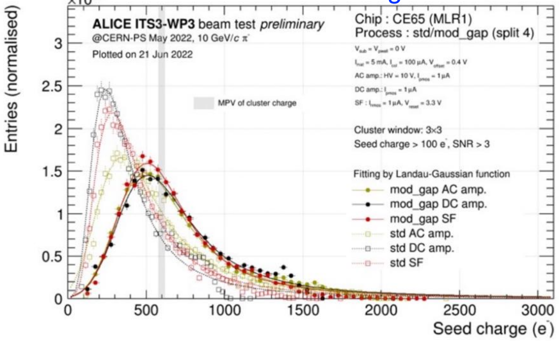
  → Feasibility of stitching for wafer-scale sensors

  → Feasibility of porting hybrid r/o architecture to monolithic process (H2M)

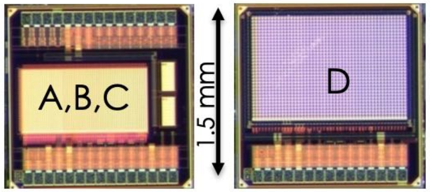
  → Thinning to <20 µm w/o performance loss

Overview of 65 nm results in presentation by Giacomo Ripamonti in CMOS session; Details on MOSS/MOST in presentation by Livia Terlizzi

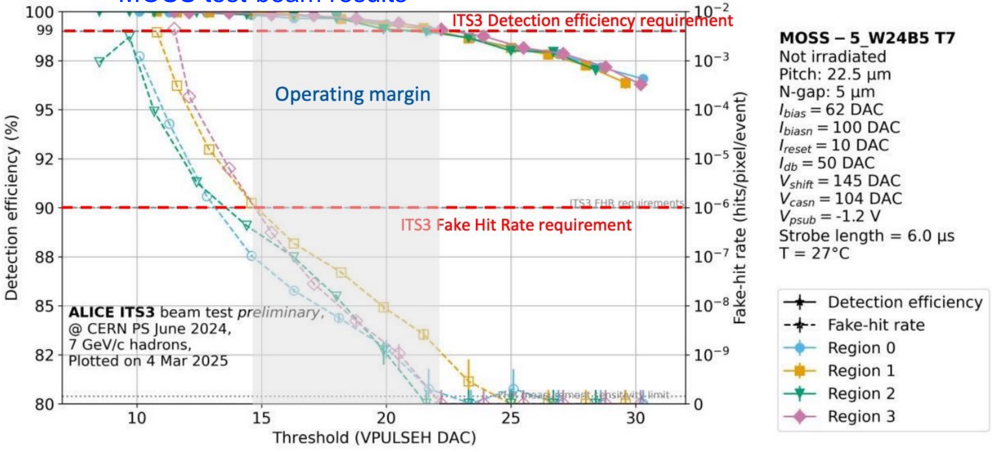
CE-65 cluster-seed charge in test beam



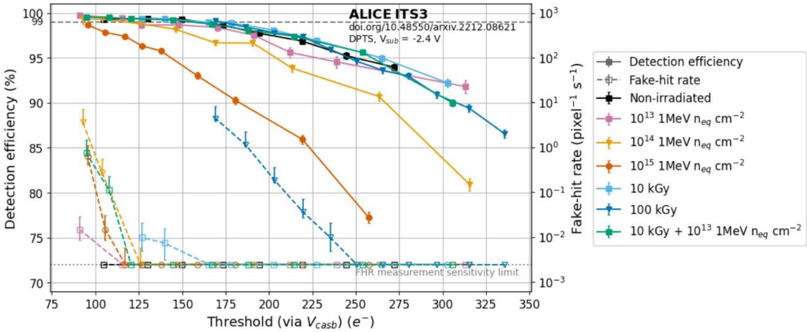
CE-65, 15-25 µm pitch IPHC



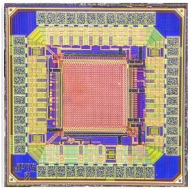
MOSS test-beam results



DPTS efficiency + fake-hit rate in test beam



Digital pixel test structure (DPTS) 15 µm pitch CERN

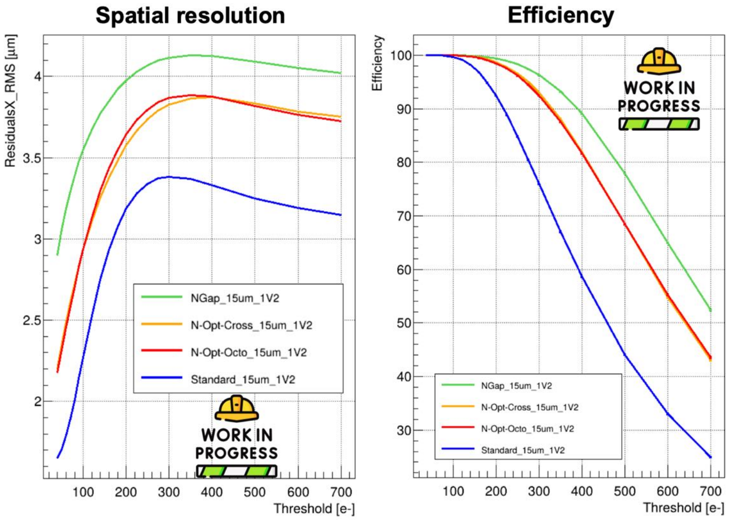


65 nm monolithic CMOS (II)

- Several ongoing developments in DRD3/7, targeting future lepton-collider vertex/tracking detectors:
  - **OCTOPUS** [13 institutes]
    - 3 µm single-point resolution, few ns timing, 100 MHz/cm^2, <50 mW / cm^2
  - **MANTA** (a.k.a. *Versatile MAPS project*) [16 institutes]
    - ~10 µm single-point resolution, ~1-100 ns, 2-200 MHz/cm², 20-100mW/cm², >$10^{14}n_{eq}$/cm²
    - Versatility: flexible pixel grouping / tuning of operation parameters for different applications
  - **NAPA** [SLAC]
    - Low-power, large-area, ultra-low-mass detector with 100 ps timing TDC
    - Prototype NAPA_p1 produced, plan to submit NAPA_p2 in 2026

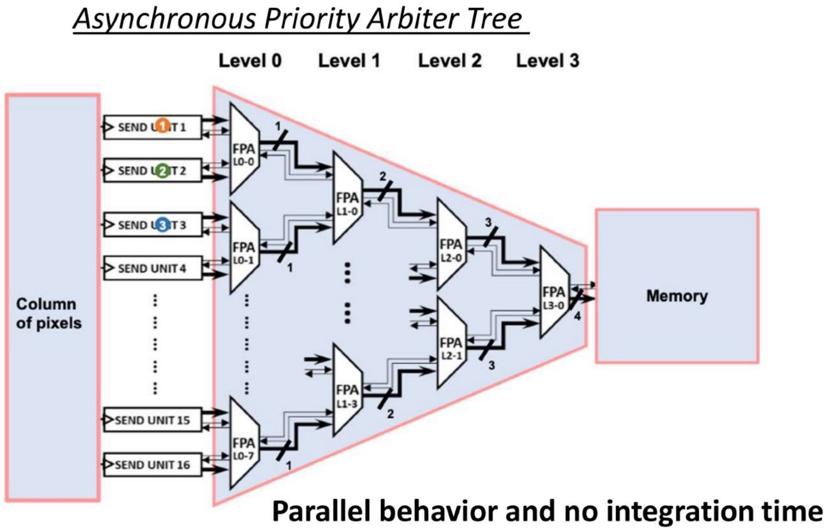
Projects share fixed-priority arbiter (FPA) asynchronous readout concept similar as implemented in SPARC ER2 sensor; plan for common prototype submission in 2026

Simulated OCTOPUS performance

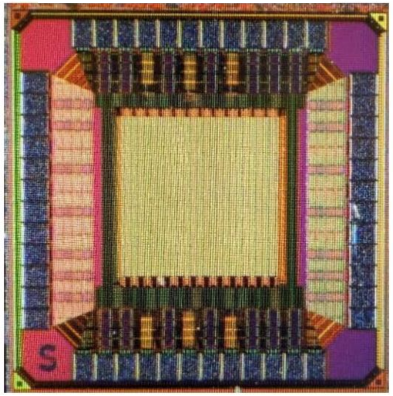


https://indico.cern.ch/event/1469148/contributions/6459242/

FPA architecture considered for OCTOPUS/MANTA



NAPA_p1 layout



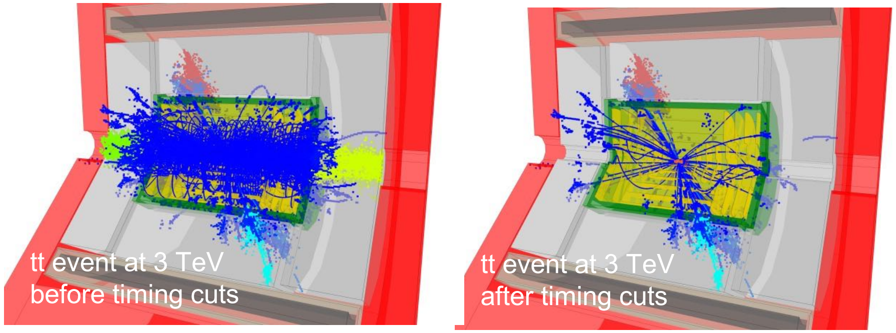
https://indico.cern.ch/event/1507215/

Silicon track-timing detectors

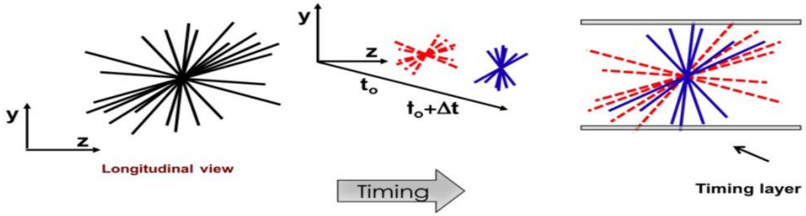
- Several (technology-driven) developments targeting ~20-100 ps pixelated timing for MIPs
  - Dedicated timing layer or integrated in tracker
- Use cases for precision timing:
  - enhanced background/backscatter rejection
  - 4D tracking
  - particle ID by Time-of-Flight for heavy-flavour physics → <30 ps / 2m for K/pi/p separation up to 3 GeV

Not part of the core Higgs-Factory requirements

CLIC background suppression with nanosecond timing

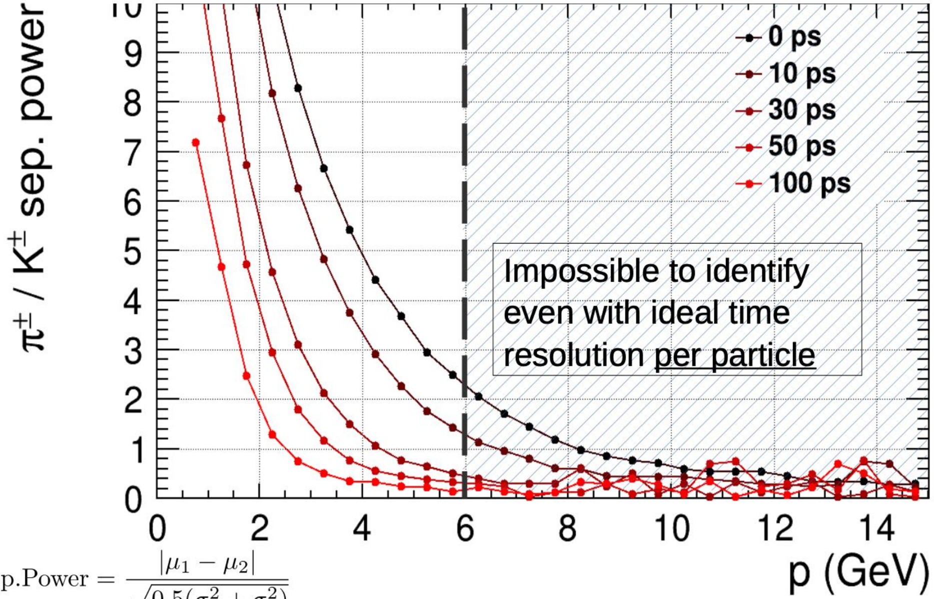


4D tracking



https://agenda.linearcollider.org/event/8217/contributions/44430

pi/K separation with timing layer 1.8m from interaction point



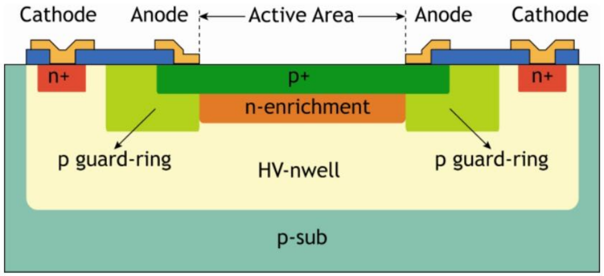
$$\text{Sep.Power} = \frac{|\mu_1 - \mu_2|}{\sqrt{0.5(\sigma_1^2 + \sigma_2^2)}}$$

Bohdan Dudar, ECFA Workshop 2022
https://indico.desy.de/event/33640/contributions/128388/

Track-timing detectors: Sensors with internal gain

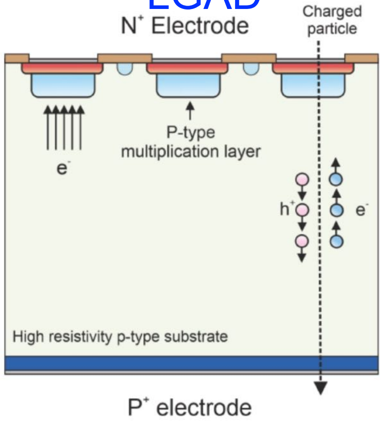
Silicon Photomultipliers (SiPM):
- Arrays of Single Photon Avalanche Detectors (SPADs)
- High gain (~10^6) from thin highly doped multiplication layer
- Challenges: fill factor, quenching, readout, rad. hardness
- Several ongoing developments (hybrid / monolithic)

SPAD

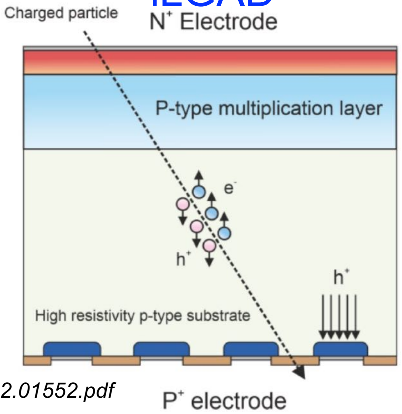


Low Gain Avalanche Detectors (LGAD):
- Signal amplification in thin multiplication layer, ~10-40x gain
→large (4 fC) and fast (<70 ps RMS) MIP signals
- Achieved so far: ~1 mm^2 cell sizes, ~95% fill factor, rad.hard. >10^{15} n_{eq}/cm^2
- In production now for ATLAS and CMS timing layers (6-16 m^2)
- Challenges:
  - Hybridisation
  - Resolution limited by time walk / readout ASIC
  - Cell size / fill factor limited by inactive regions between pixels
    → inverted LGADs (iLGAD): continuous multiplication layer on backside
    → trench-isolated LGADs (TI-LGAD): JTE replaced by deep etched trenches filled with di-electric

LGAD

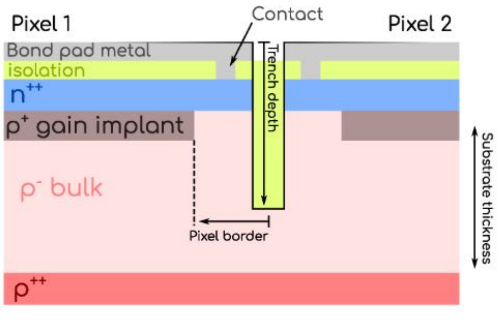


iLGAD



https://arxiv.org/pdf/2202.01552.pdf

TI-LGAD



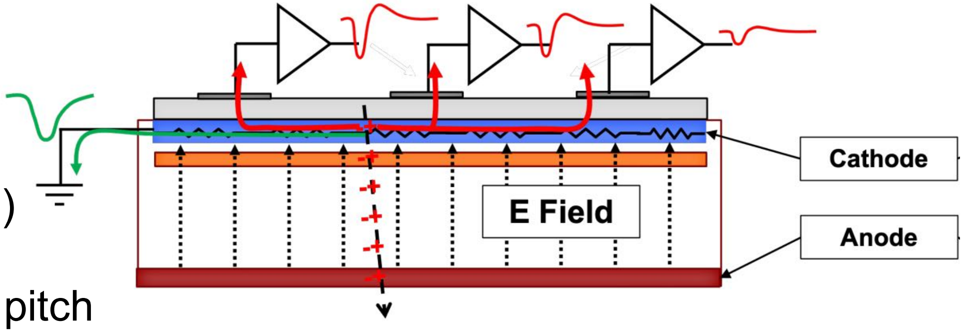
https://www.mdpi.com/1424-8220/23/13/6225

Track-timing detectors: AC-coupled LGAD

Resistive (AC-coupled) LGAD (RSD)

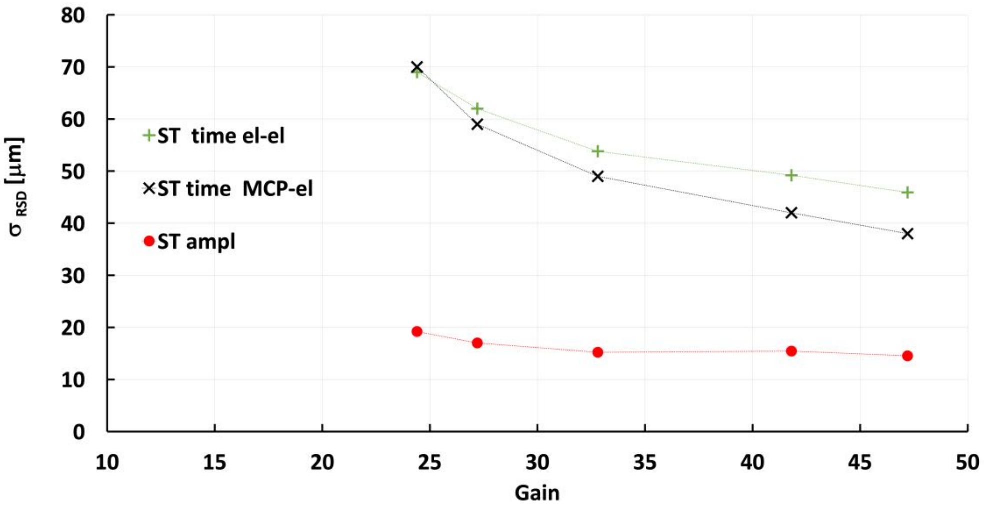
- Resistive cathode, AC-coupled to r/o pads
  → enhanced position resolution through amplitude interpolation
  → suitable as timing layer in low-occupance regions
- Time resolution of ~60 ps achieved (limited by FAST2)
- Position resolution of 15 µm for 450 µm r/o pitch
  → significantly better than standard LGAD with same pitch
- 100% fill factor

RSD-based tracking detector



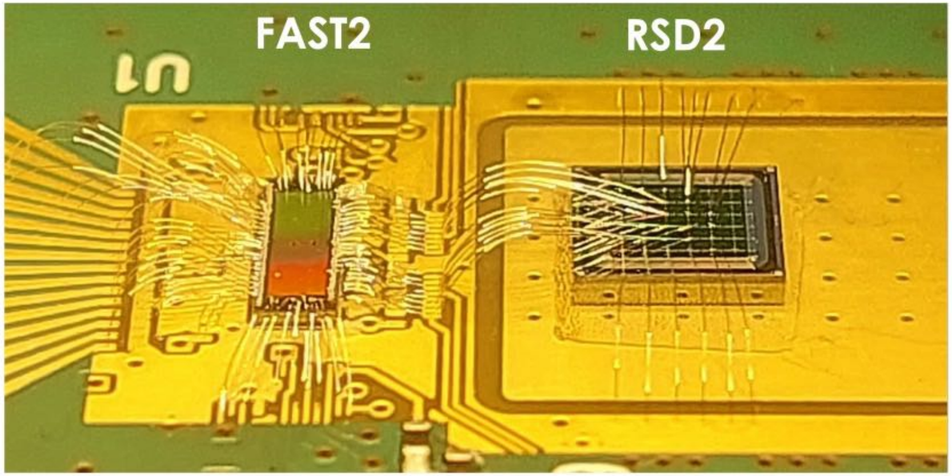
http://dx.doi.org/10.1016/j.nima.2022.167228
N. Cartiglia et al.

Position resolution in test beam for different reconstr. methods



https://doi.org/10.1016/j.nima.2024.169380

RSD prototype, 450 µm pitch

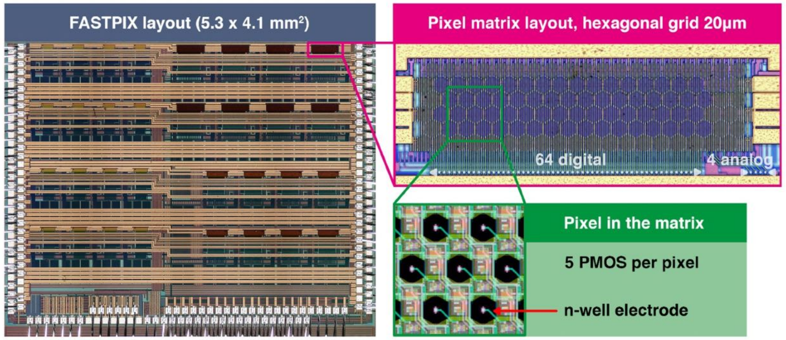


→ Presentations on AC-LGAD by Simone Mazza and Issei Horikoshi on Tuesday

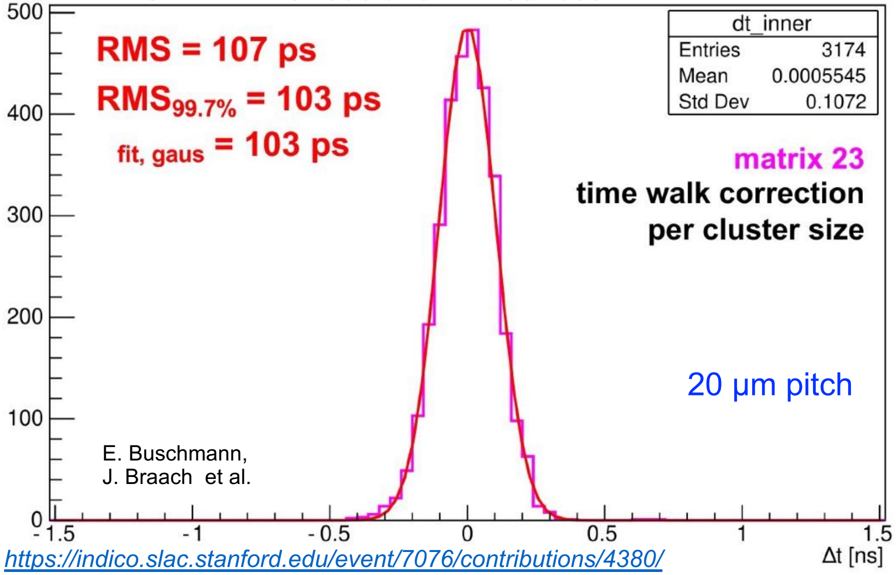
Track-timing detectors: monolithic

FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process, design optimisations for for fast charge collection
- Small hexagonal pixels (8.7 - 20 µm pitch)
- Focus on sensor performance, with limited in-pixel circuitry and not optimised for low power yet
- Exploring large parameter space of process and design variations
- Time resolution ~100 ps in test beam @ >99% effic.
- Position resolution ~1 µm for 8.7 µm pitch



FASTPIX time resolution in test beam



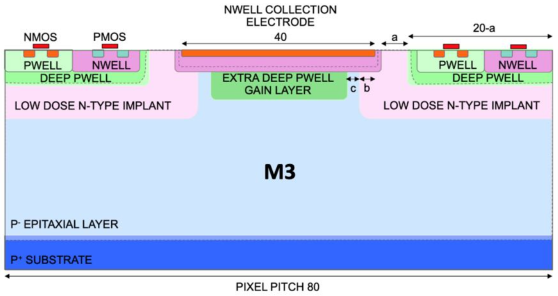
E. Buschmann, J. Braach et al.

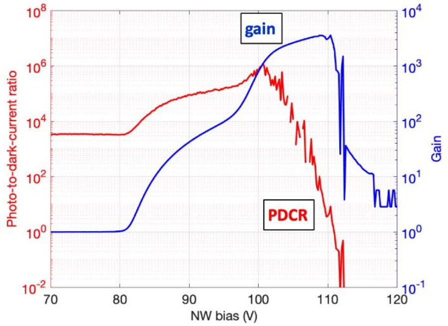
https://indico.slac.stanford.edu/event/7076/contributions/4380/

http://dx.doi.org/10.3390/instruments6010013

CASSIA - CMOS Active Sensor with Internal Amplification

- Modified 180 nm CMOS with deep p-well gain layer
- CASSIA1 (3x3 pixels, 80 µm pitch):
  → demonstration of sensor gain (I/V, laser)





- CASSIA2 (in production):
  - front-end amplify. + discrim. (LGAD mode, 5x5 px)
  - quenching circuit (SPAD mode, 4x4 px)

https://indico.cern.ch/event/1507215/contributions/6540427/ CERN, Univ. Zagreb

Small-pitch monolithic timing also explored in SiGe BiCMOS process: MONOLITH https://arxiv.org/abs/2412.07606

Conclusions + Outlook

- Stringent requirements for Higgs-Factory vertex and tracking detectors:
    - Precision physics needs
    - Environmental conditions

- Several optimized detector concepts with different technology choices are proposed

- Broad silicon R&D profiting from advancements in semiconductor industry + simulation-based process optimisations

- Focus on sensor (test-beam) performance; engineering/system aspects not yet fully addressed (many of them depend on accelerator choice)

- Large synergies with approved projects, but no complete overlap of requirements

- Fulfilling all Higgs-Factory requirements simultaneously remains challenging

Thanks to everyone who provided material for this talk!

Additional Material

Motivation for a Linear Lepton Collider

- Synchrotron radiation losses in circular lepton colliders limit **energy** and **luminosity** reach and efficiency

→ Linear lepton colliders can reach **higher centre-of-mass energies** at **lower power budget**

- Linear colliders can be extended in length (**staged construction**) to increase the energy towards **multi-TeV**

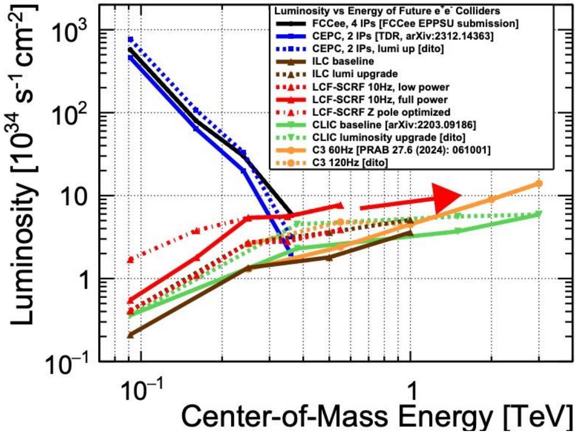
→ Unique combination of **high collision energies** with **high luminosity** and **clean e^+e^- environment**

→ **Flexible** running and upgrade scenarios, adaptable to physics results and advancements in accelerator technology

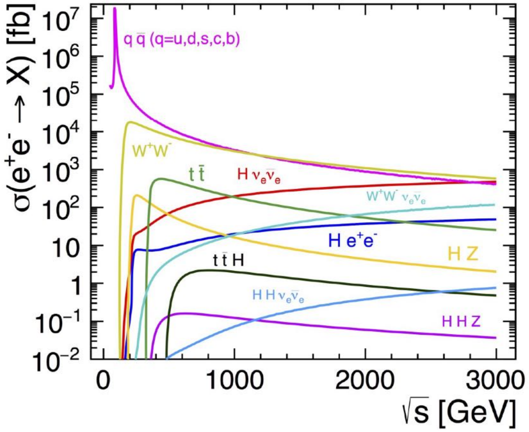
  → Probe various **Higgs-** and **top-production** processes dominant at different energy scales

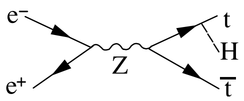
  → Sensitivity to **new physics** with electroweak-sized coupling strength or through mixing with known particles

Energy and luminosity reaches for circular and linear colliders:



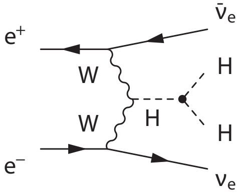
Complementary Higgs measurements by accessing wide energy range:





Radiation off top-quarks: e^+e^-→ttH

- Measure top Yukawa coupling
- Needs **$\sqrt{s} \gtrsim 500$ GeV**

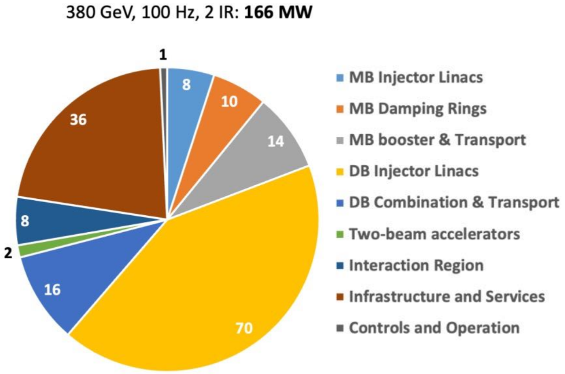


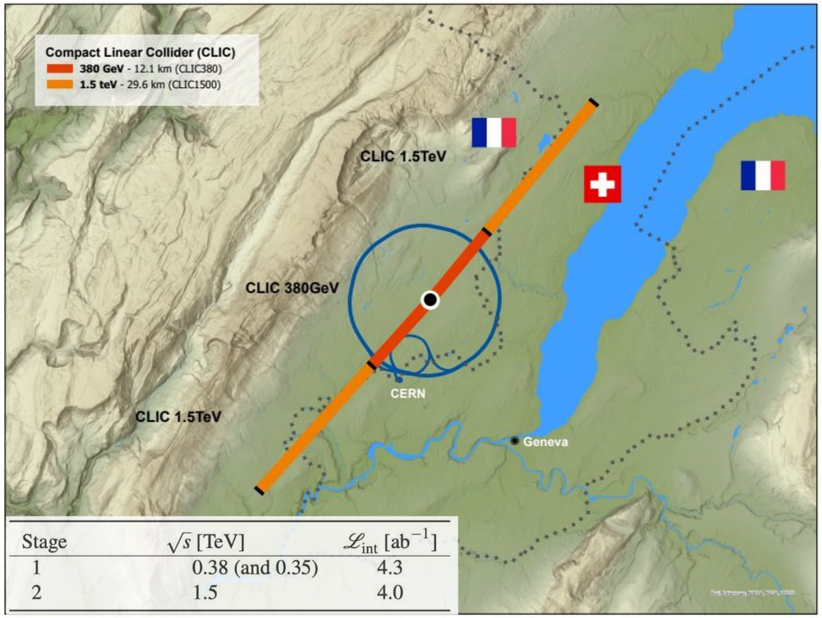
Double-Higgs prod.: e^+e^-→$HH\nu_e\nu_e$

- Measure tri-linear self coupling
- Needs high **$\sqrt{s} \gtrsim 1.5$ TeV**

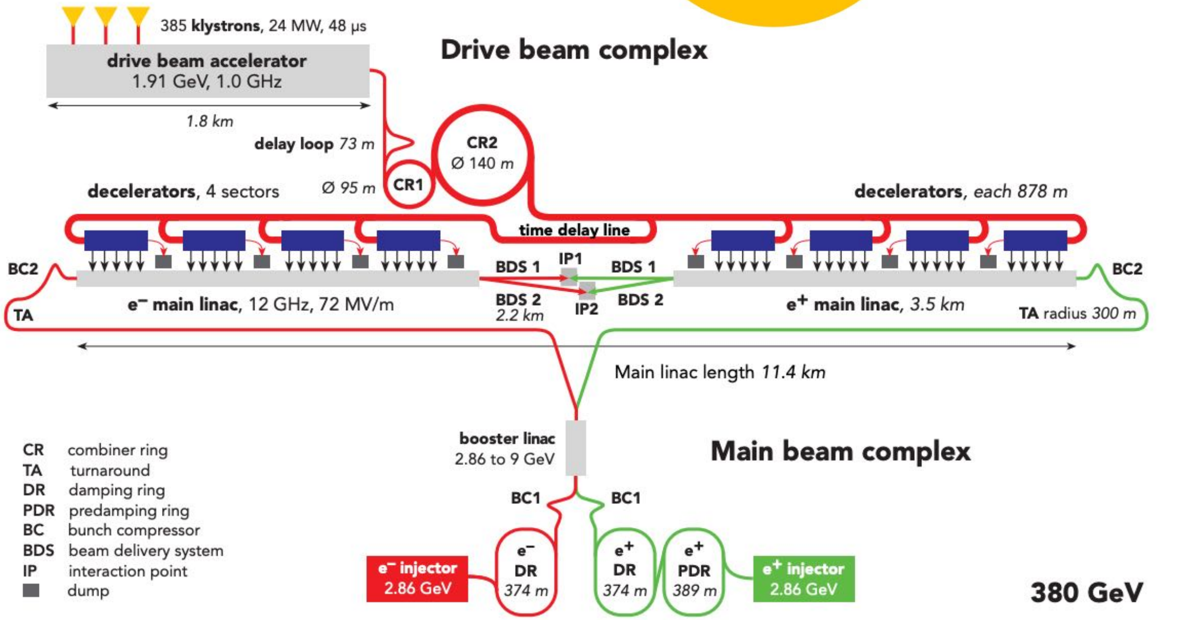
CLIC staged implementation

- New 2025 staging baseline optimised for luminosity performance, cost and power:
  - **380 GeV**: 12.1 km tunnel, 100 Hz operation, P=166 MW, L_{tot} = 4.5 x 10^{34} cm^{-2} s^{-1}
  - **1.5 TeV**: 29.6 km tunnel, 50 Hz operation, P=282 MW, L_{tot} ~ 5.6 x 10^{34} cm^{-2} s^{-1}
  - **2 interaction points**, flexible sharing of luminosity
  - **Single drive beam** for both stages (feasible up to 2 TeV)
  - **3x higher luminosity / power**, compared to 2018 design (0.82 TWh/y @380 GeV; 1.4 TWh/y @1.5 TeV)





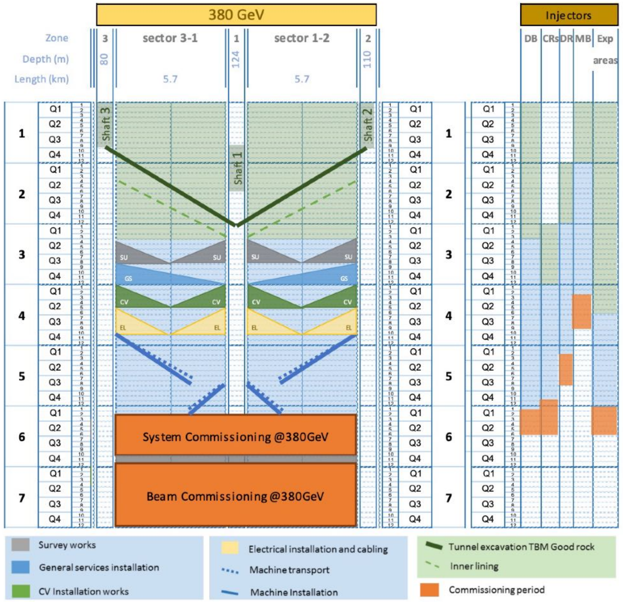
Stage	$\sqrt{s}$ [TeV]	$\mathscr{L}_{int}$ [ab^{-1}]
1	0.38 (and 0.35)	4.3
2	1.5	4.0



https://indico.cern.ch/event/1439855/contributions/6461475/

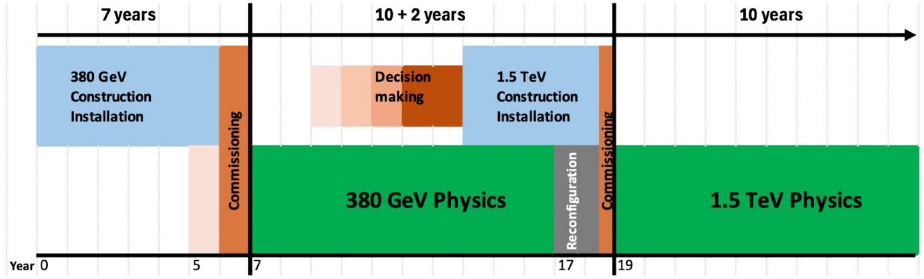
CLIC schedule and cost

Construction schedule for 380 GeV stage

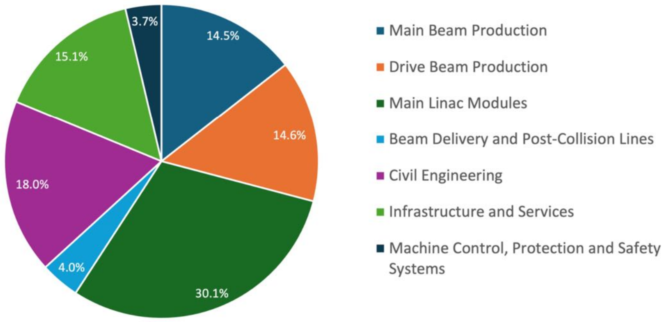


- First stage can be constructed in **7 years**, starting ~2034-35
    - Cost of 380 GeV stage: **7.2 BCHF**
    - Alternative 250 GeV 1st stage: 6.5 BCHF
    - Alternative 550 GeV 1st stage: 9.4 BCHF
- Construction of 2nd stage with minimal interference (2y gap)
    - Cost of upgrade to 1.5 TeV: **7.1 BCHF**
- Cost of detector (CLICdet design): **~400 MCHF**
- Physics program covers ~10 years per stage, accumulating **≳4 ab^{-1}** per stage
    - Operation cost @ 380 GeV: **137 MCHF / y + ~650 FTEy / y**
    - Energy cost: **66 MCHF / y** @ 380 GeV (**112 MCHF /y** @ 1.5 TeV)

Construction and operation schedule for 2-stages

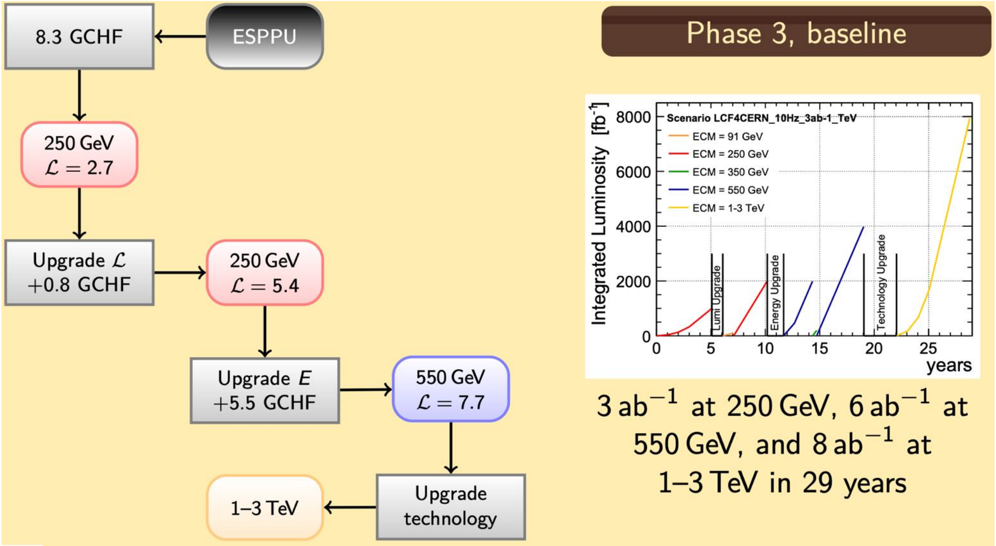


Construction cost share for 380 GeV



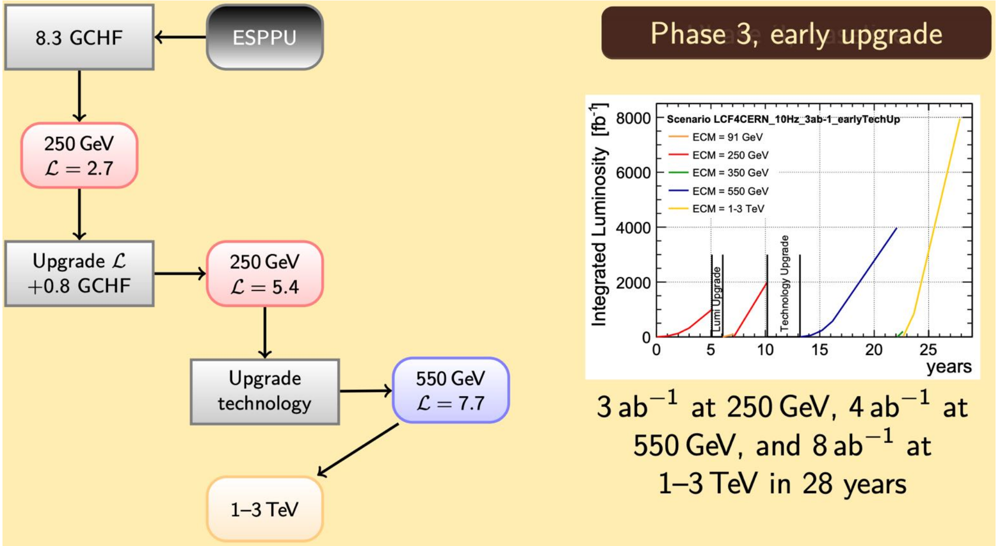
LCF @ CERN

- CLIC underground civil-engineering footprint is also **compatible** with **alternative acceleration technologies**
- Strategy submission “Linear Collider Facility @ CERN (LCVision)” discusses several options with **SCRF** stages
  - Pros: first stage(s) based on already **industrialized** SCRF technology
  - Cons: high **cost** of initial stages (250 GeV: **9.1 BCHF**; 550 GeV: **+5.5 BCHF**), **long down times**



Phase 3, baseline

3 ab^{-1} at 250 GeV, 6 ab^{-1} at 550 GeV, and 8 ab^{-1} at 1–3 TeV in 29 years



Phase 3, early upgrade

3 ab^{-1} at 250 GeV, 4 ab^{-1} at 550 GeV, and 8 ab^{-1} at 1–3 TeV in 28 years

P. Kloppenburg
https://indico.cern.ch/event/1527581/contributions/6497901/

→ Such alternative options show the **versatility** of the Linear Collider concept
→ LCVision initiative helps to **engage** the world-wide ILC community in a CERN-based project
→ However: **CLIC** technology remains **preferred Linear Collider option** for CERN in terms of energy reach, feasibility and cost

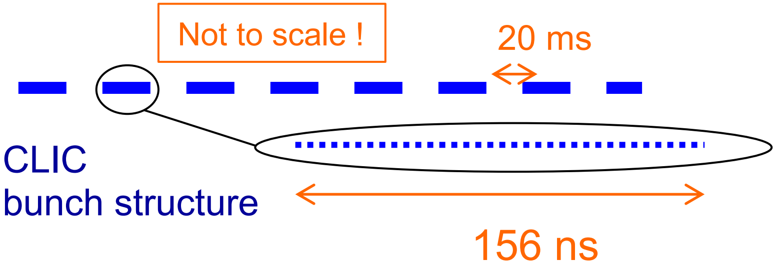
Experimental conditions at CLIC

- CLIC operates with bunch trains, 50 Hz repetition rate

→ Low duty cycle

→ Trigger-less readout between trains

→ Allows for power-pulsed operation of detector, to reduce average power consumption

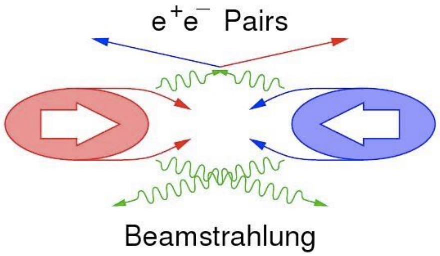


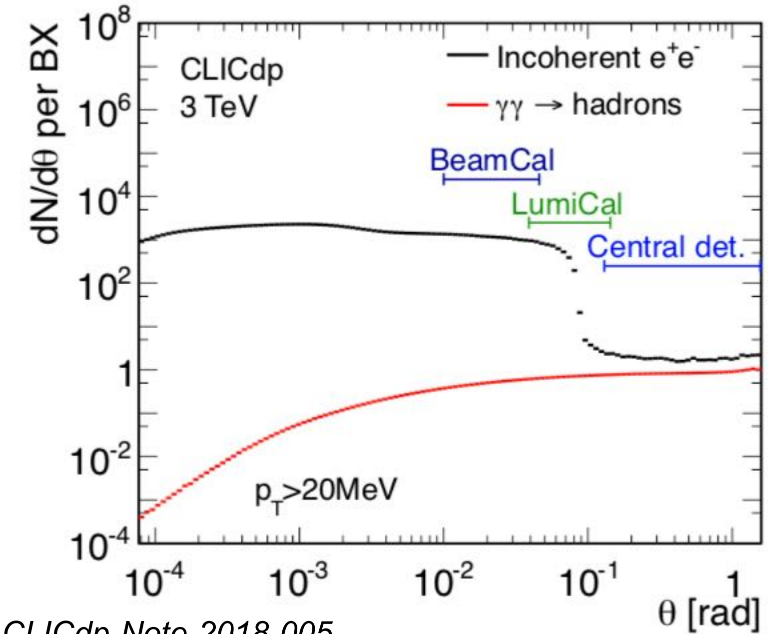
Very small bunches:
40 nm (x) x 1 nm (y) x 44 µm (z)
(at 3 TeV)

- Collisions within 156 ns bunch trains
- High E-fields lead to Beamstrahlung

→ High rates of beam-induced background particles

→ Drives detector design (layout, granularity, timing)





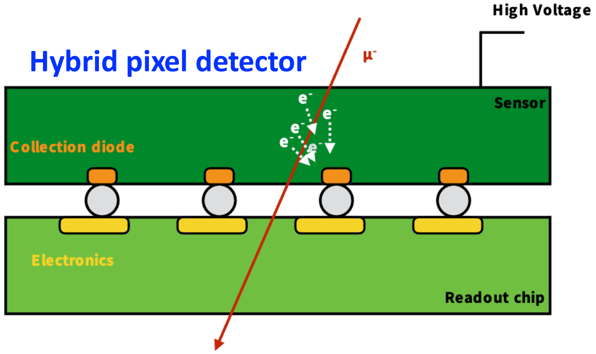
CLICdp-Note-2018-005

Main backgrounds in detector

- **Incoherent e+e- pairs**
  - 19k particles / bunch train at 3 TeV
  - Constrains beam pipe radius, granularity
- $\gamma\,\gamma$ →hadrons events
  - 17k particles / bunch train at 3 TeV
  - Constrains granularity, layout, impacts physics

High instantaneous hit rates (up to 6 GHz/cm^2), however: very low readout rate (50 Hz)

Hybrid pixel detectors



Hybrid pixel detectors

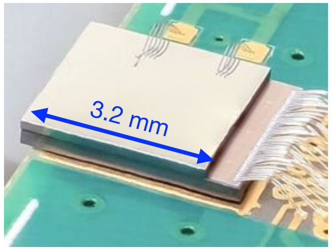
- Target applications: CLIC vertex detector, track-timing layers
- Separate interconnected sensor and readout ASIC layers

→ Factorise R&D on sensors and readout ASICs

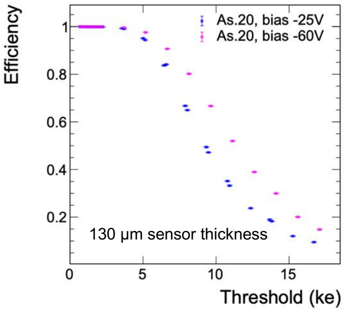
- Develop new sensor concepts, e.g.:
  - Thin sensors (50 µm) with large fill factor (active edge)
  - Active / passive CMOS sensors
  - Sensors with enhanced lateral drift (ELAD) for optimal position resolution
  - Sensors with charge amplification (LGAD) for picosecond timing
- Profit from advanced industry technologies for highest ASIC performance (rate, timing)
- Profit from synergy with (HL)-LHC developments, medical imaging, gaseous detector r/o (GridPix)
- Refine and develop new interconnect technologies
- Challenges: material budget, interconnect: cost, minimum pitch

Test-beam studies for 65 nm CLICpix2 with thin active-edge sensors (25 µm pitch)

CLICpix2 hybrid assembly

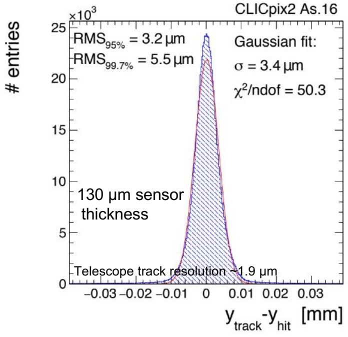


Efficiency

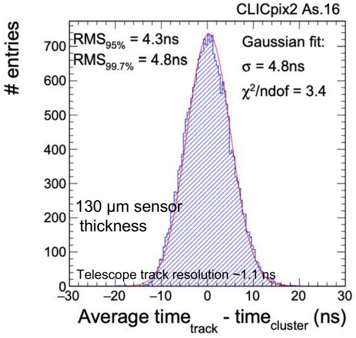


CERN-THESIS-2020-338

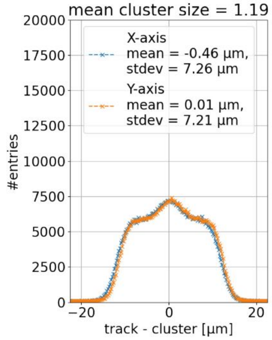
Spatial residuals



Timing residuals



Spatial residuals for 50 um thick sensor



arXiv:2210.02132

- Efficiency, spatial and timing resolution targets are achieved, but not yet simultaneously with material budget target
  → need advanced sensors / smaller pitch (→ 28 nm ASICs, also considered for HL-LHC)

Fine-pitch hybridization

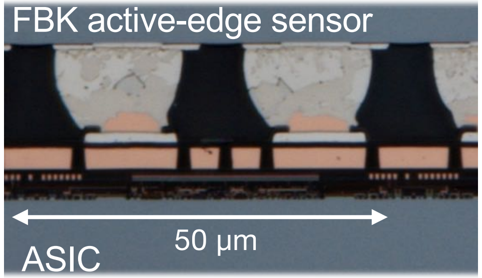
- Sensor/ASIC interconnect is one of the main challenges for hybrid pixel-detectors:
  - Cost / complexity, material budget, minimum pitch, single-die processing during R&D
- Different interconnect technologies are under study for future-collider detectors

Single-die bump-bonding process developed by IZM:

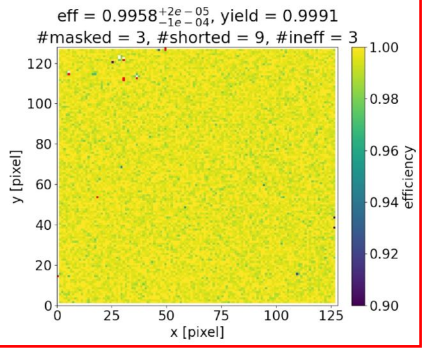
- pitch 25 µm, sensor thickness down to 50 µm
- Support-wafer processing of CLICpix2 ASICs from MPW for UBM and SnAg bump deposition
- Excellent interconnect yield >99.7% observed in laboratory and test-beam measurements

https://arxiv.org/abs/2210.02132

25 µm bump bonding @ IZM



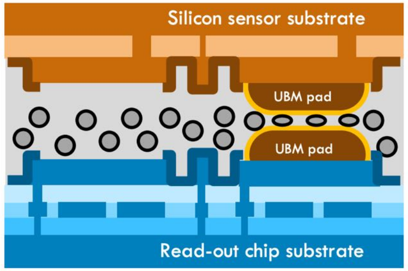
TB pixel effic. 50 µm CLICpix2 ass.



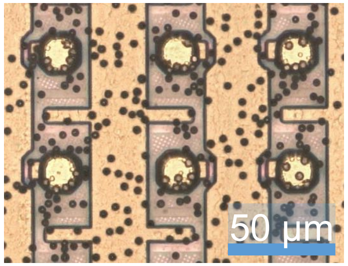
Hybridisation with **Anisotropic Conductive Films (ACF):**

- Adhesive epoxy film with embedded conductive micro-particles, electrical connection through thermo-mechanical compression
- Ongoing development / optimization of two single-die in-house processes:
  - Chemical Electroless Nickel Immersion Gold (ENIG) deposition for Under Bump Metallization (UBM)
    → uniformity, thickness, edge effects
  - Semi-automatic flip-chip bonding with ACF layer
    → ACF material (particle diameter and density), epoxy thickness, bonding profile
- Proof-of-principle results for Timepix3 hybrid assemblies
  → high interconnect yield in regions with good UBM
  → ongoing optimization of UBM process for single dies
- ACF also under study for module integration
  → 'easier' use case (large-pitch interconnect)
- Also tests with paste (ACP) and non-conductive (NCP)

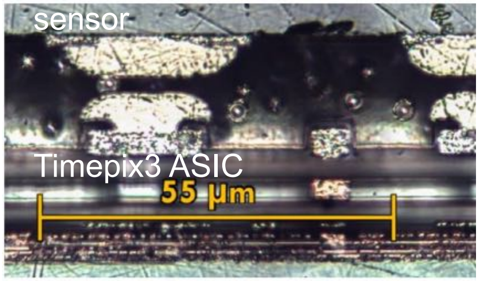
ACF bonding w/ conductive micro-particles



ACF on Timepix3

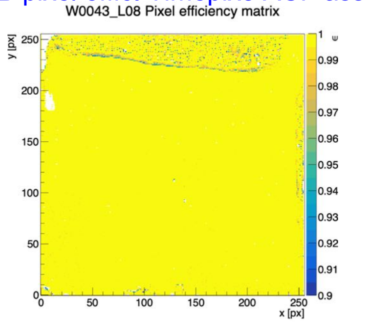


55 um ACF interconnect



https://arxiv.org/abs/2210.13046

TB pixel effic. Timepix3 ACF ass.



ACF for module integration

ACF module integration

Larger bonding pads: 80 µm – few mm diam.

→ Similar to industrial ACF usage

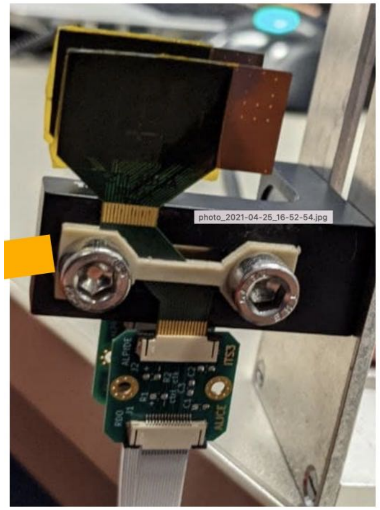
→ Good interconnect results

→ Topology / uniformity of UBM important

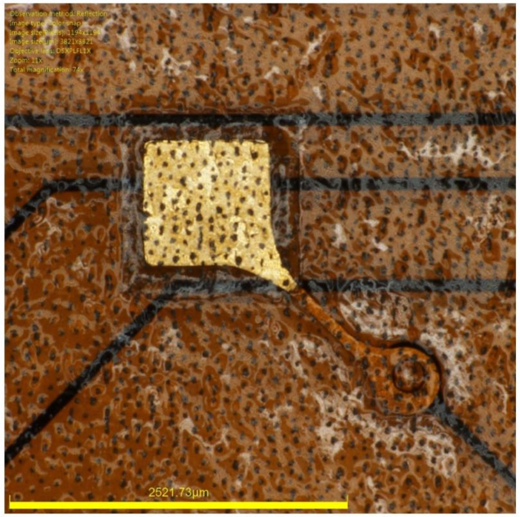
Various proof-of-concept projects:

- Beam tests of ALPIDE ACF modules
- Bonding tests with MALTA silicon bridges
- Tests with FCAL LUXE pad sensors

ALPIDE ACF module in DESY TB

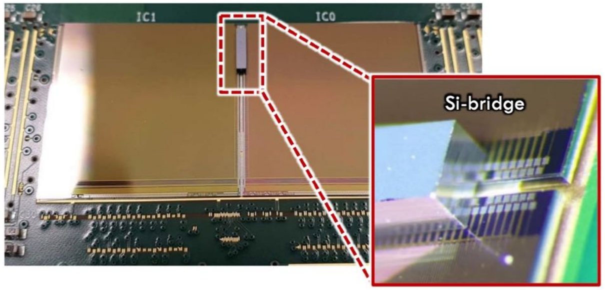


ACF on LUXE pad



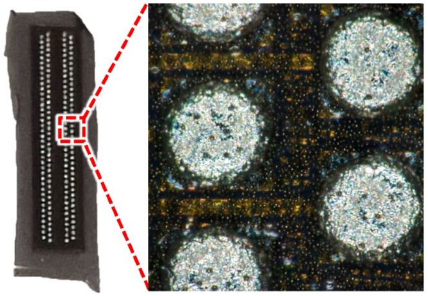
MALTA module building with silicon bridge and ACF bonding

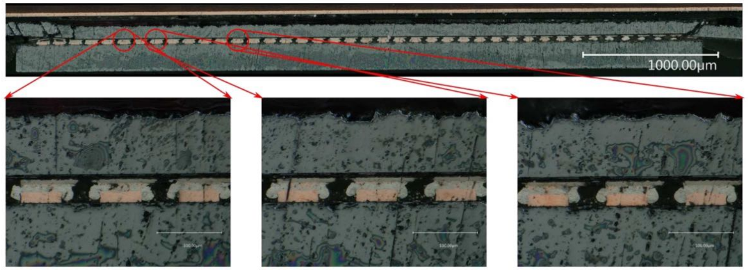
MALTA double module with Si-bridge chip (images credit: Florian Dachs)



Si-bridge with ACF

ACF over Si-bridge pads





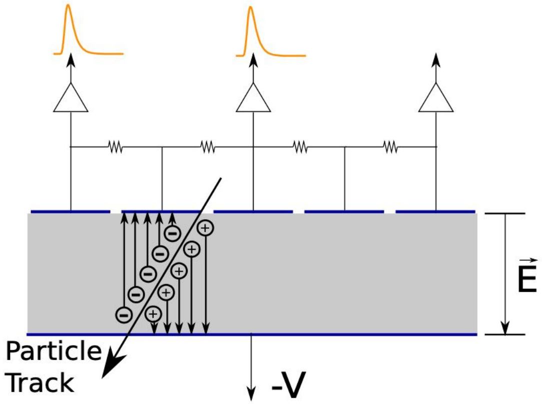
Cross section for 5kg of pressure.

M. Mager, F. Dachs, Y. Benhammou

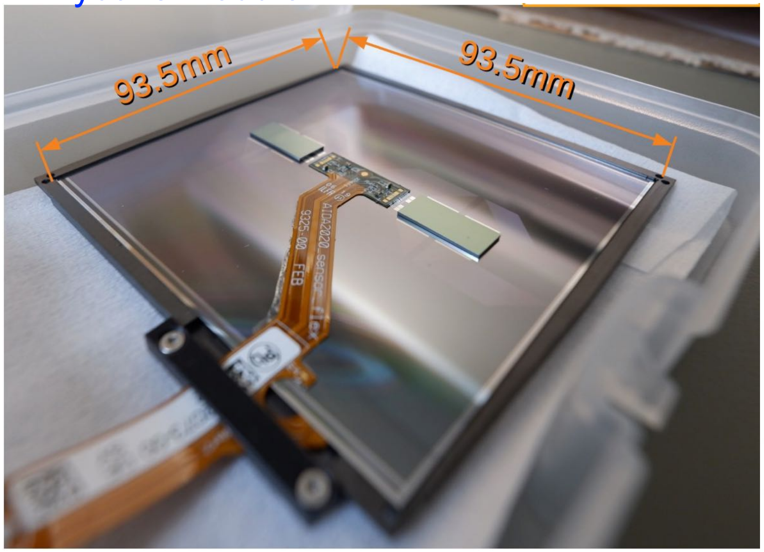
Hybrid strip detectors

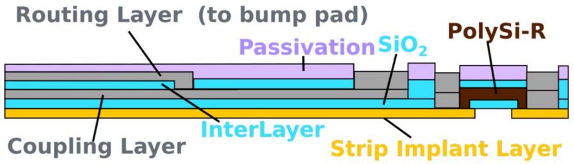
Hybrid strip detectors:

- Baseline for LCF trackers (also suitable for CLIC outer layers)
- Well-established technology (e.g. HL-LHC)
    - low material + power (sparse readout)
    - large and fast signals (dE/dx)
    - high spatial resolution (charge interpolation) in R/phi direction
    - Advanced sensor concepts (e.g. stitched passive CMOS strip sensors)
    - Challenges: not for high occupancy regions; complex interconnect



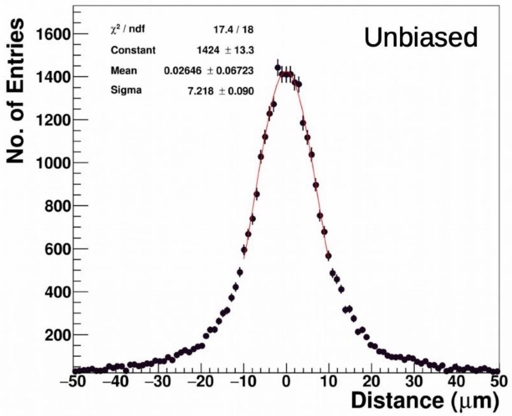
Lycoris module



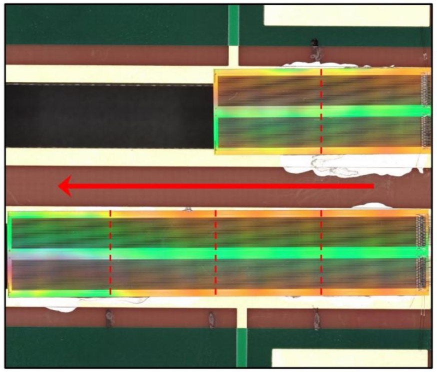


https://indico.cern.ch/event/995633/contributions/4259345

- Lycoris development DESY / SLAC:
    - 320 µm thick SiD sensors, 25 µm strip pitch, 50 µm r/o pitch
    - KPiX r/o ASIC bump-bonded on-sensor → high fill factor
    - 7 µm single-point resolution achieved in test beam
    - Test-case: beam telescope for PCMAG@DESY



Stitched passive CMOS sensors



Freiburg, DESY, Bonn

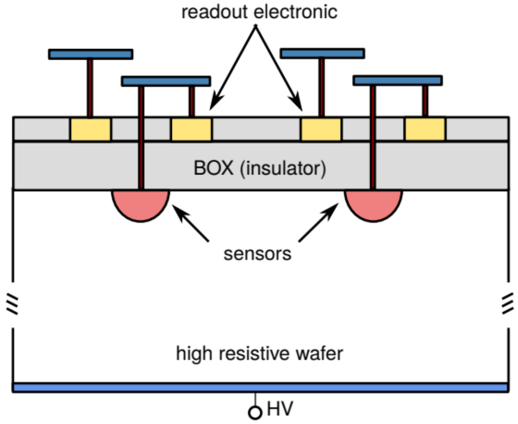
https://indico.cern.ch/event/995633/contributions/4259384/attachments/2209268/3738710/Passive%20CMOS%20Strip%20Sensors.pdf

Silicon-on-Insulator (SOI) / 3D integration

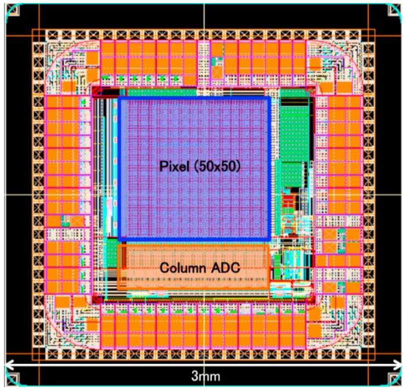
- Silicon-On-Insulator (SOI): r/o electronics on thin low-resistivity electronics wafer, separated from high-resistivity sensor wafer by buried insulation oxide layer

- Thin + fast (fully depleted) ”monolithic” sensors
- Challenge: specialized + complex production process (wafer bonding)
- Various developments targeting LC vertex and tracking detectors, e.g.:
  - SOFIST V1 in 200 nm LAPIS SOI
    20x20 μm^2 pitch, 200 μm thickness → σ_{SP}~1.4 μm
  - Cracow SOI test chip in 200 nm LAPIS SOI process
    30x30 μm^2 pitch, 500 μm thickness → σ_{SP}~1.5 μm
  - CPV4 SOI-3D LAPIS SOItest chip (IHEP)
  - IPHC LAPIS SOI test chip (with KEK)
  - 3D developments @ IPHC (with TJ, T-Micro)
- Precision timing not yet demonstrated

SOI pixel detector

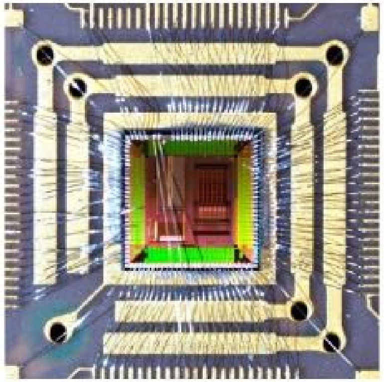


SOFIST v1



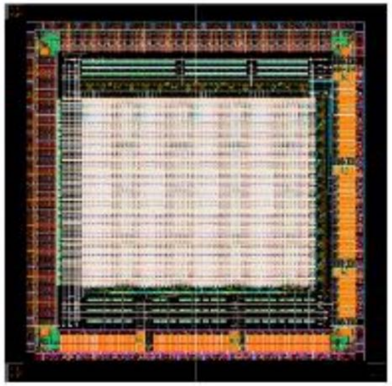
https://doi.org/10.1016/j.nima.2018.06.075

Cracow SOI test chip



Nucl. Instrum. Methods Phys. Res., A 988 (2021) 164897

CPV4 SOI-3D



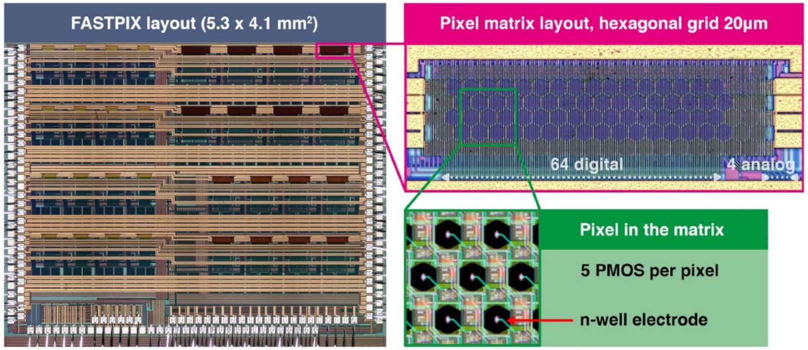
IPHC double-tier 3D TJ 180

https://indico.cern.ch/event/995633/contributions/4259377/attachments/2208714/3738410/LCWS2021_BESSON_vf.pdf

ATTRACT FASTPIX

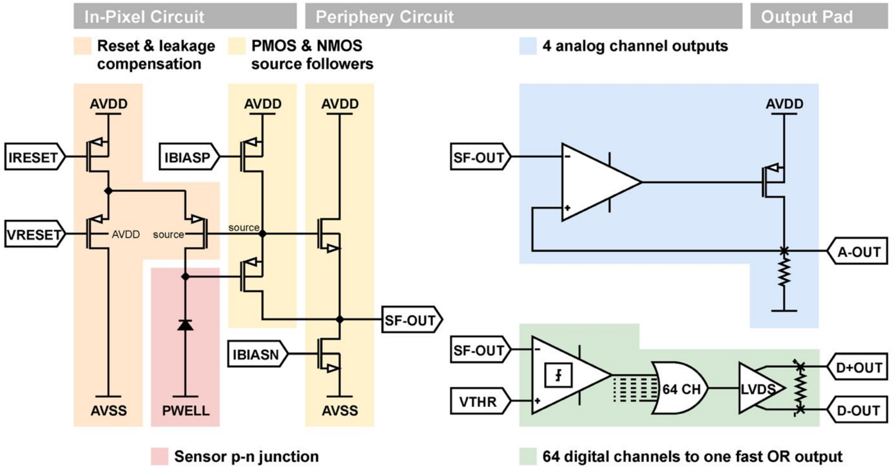
FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process
- 32 mini matrices of hexagonal pixels (8.66 to 20 µm pitch)
- 4 analogue outputs + 4x16 pixels with ToT/ToA
- Various sensor designs and process options
- Position and ToT encoding via delay lines (asynchr. r/o)



On-chip readout circuit

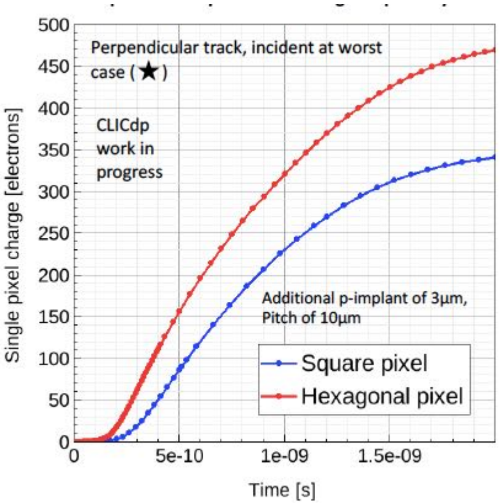
W. Snoeys, T. Kugathasan

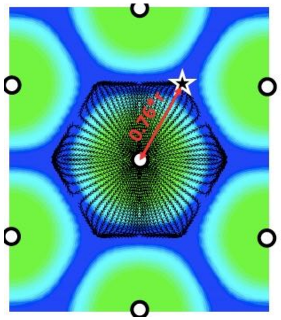


Simulated chip parameters:

Sensor capacitance		1 fF
Equivalent Noise Charge		11 e⁻
Jitter (for Q_{in} = 1000 e⁻)		20 ps
Power	In pixel source follower	18 µW
	Periphery discriminator	150 µW
	Analog monitoring buffer	20 mW

3D TCAD Simulation





T. Kugathasan et al: Monolithic CMOS sensors for sub-nanosecond timing, Hiroshima 2019

- Optimised for precise sensor timing in 3D TCAD simulation studies
- Hexagonal pixel layout:
  - Improved charge collection at pixel edges
  - Reduced number of neighbouring pixels → Less charge sharing

Caribou DAQ

Versatile data acquisition system based on programmable hardware

https://gitlab.cern.ch/Caribou

System-on-Chip (SoC) board

- Embedded CPU for DAQ, user interface, operating system (Linux)
- Field programmable gate array (FPGA) for detector control and data processing

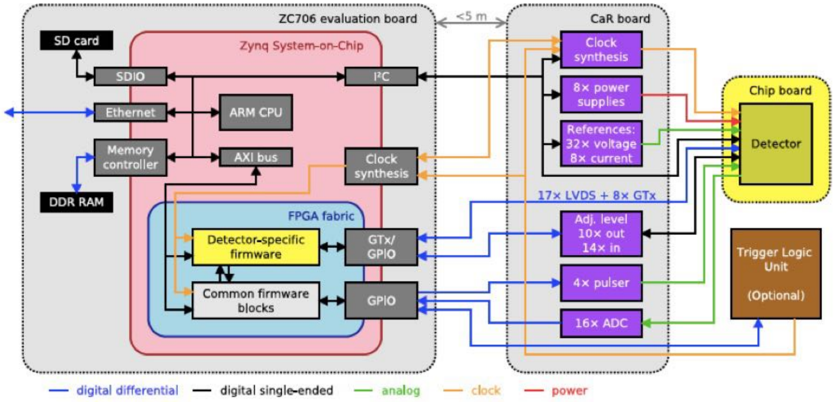
Control and Readout (CaR) interface board

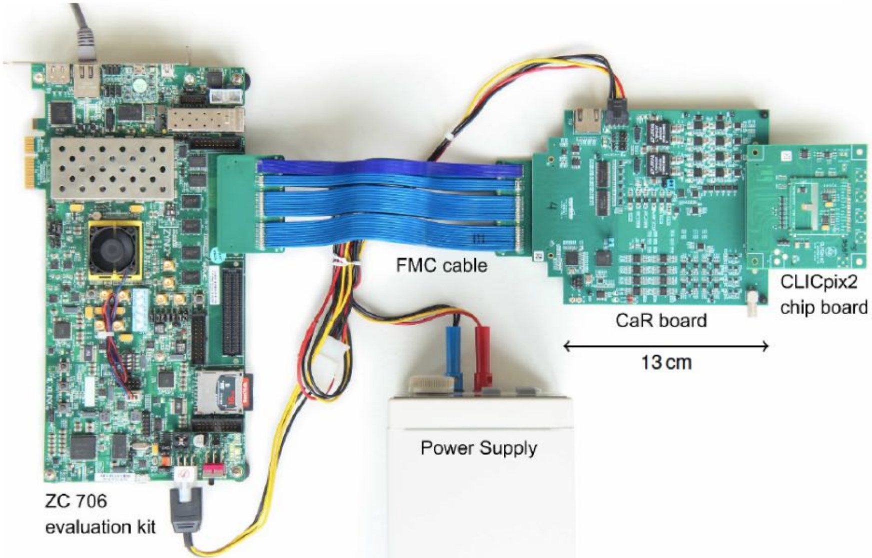
- Physical interface from SoC board to detector chip
- Voltage regulators, ADCs, pulse/clock generator

Application-specific detector carrier board

- Only detector chip and passiv components

- Successfully used for ATLASPix, ATLASPix2, ATLASPix3, CLICpix2/C3PD, H35Demo/FEI4, RD50-MPW1

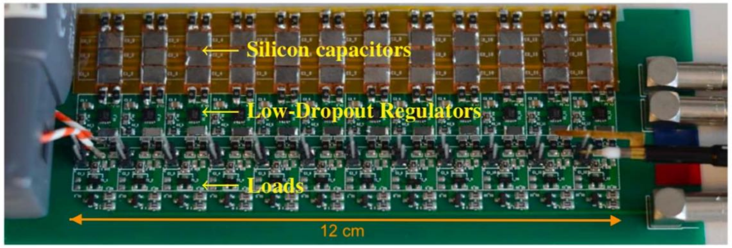




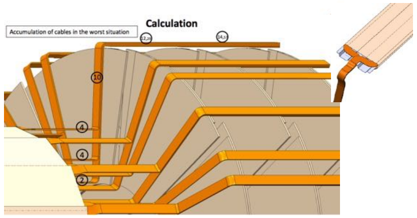
https://iopscience.iop.org/article/10.1088/1748-0221/12/01/P01008

Silicon detector integration

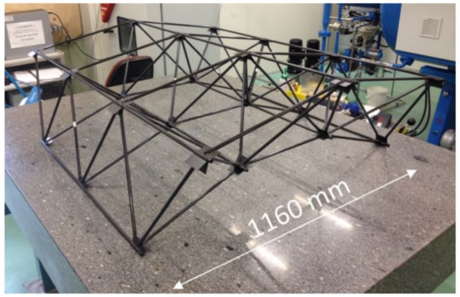
Power-pulsing mockup



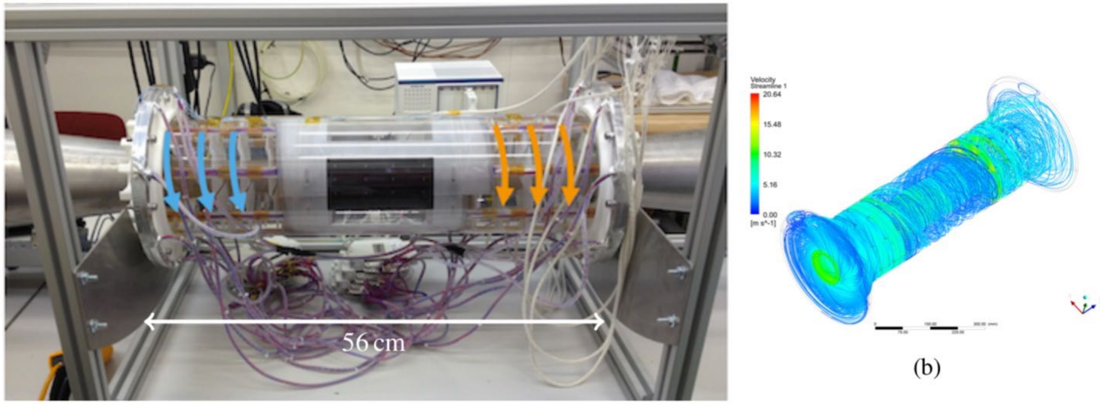
Vertex-detector services



Outer barrel tracker support structure

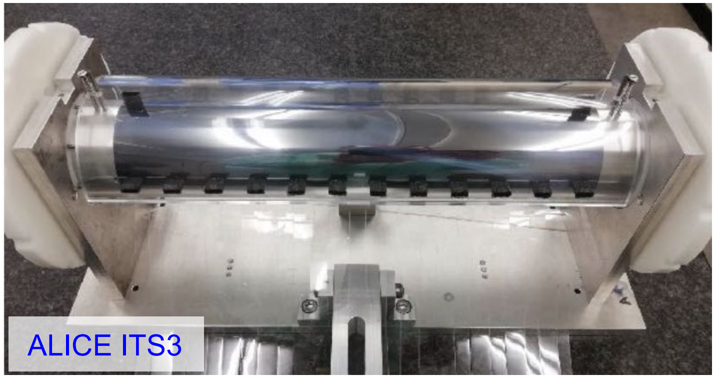


Air-flow cooling mockup and simulation



(b)

Bent wafer-scale dummy sensor on foam support



- Engineering studies based on calculations, simulations, prototyping
  → confirm feasibility of detector concepts + provide input for realistic performance simulation
- Profit from recent developments in approved projects (Belle II, ALICE ITS3, CMB@FAIR)
- However: not all critical Higgs-Factory requirements are fulfilled by these developments (e.g. barrel/endcap geometries, combination of low material budget and precise timing)
- More focused effort required, but depends also on choice of project (linear vs. circular)