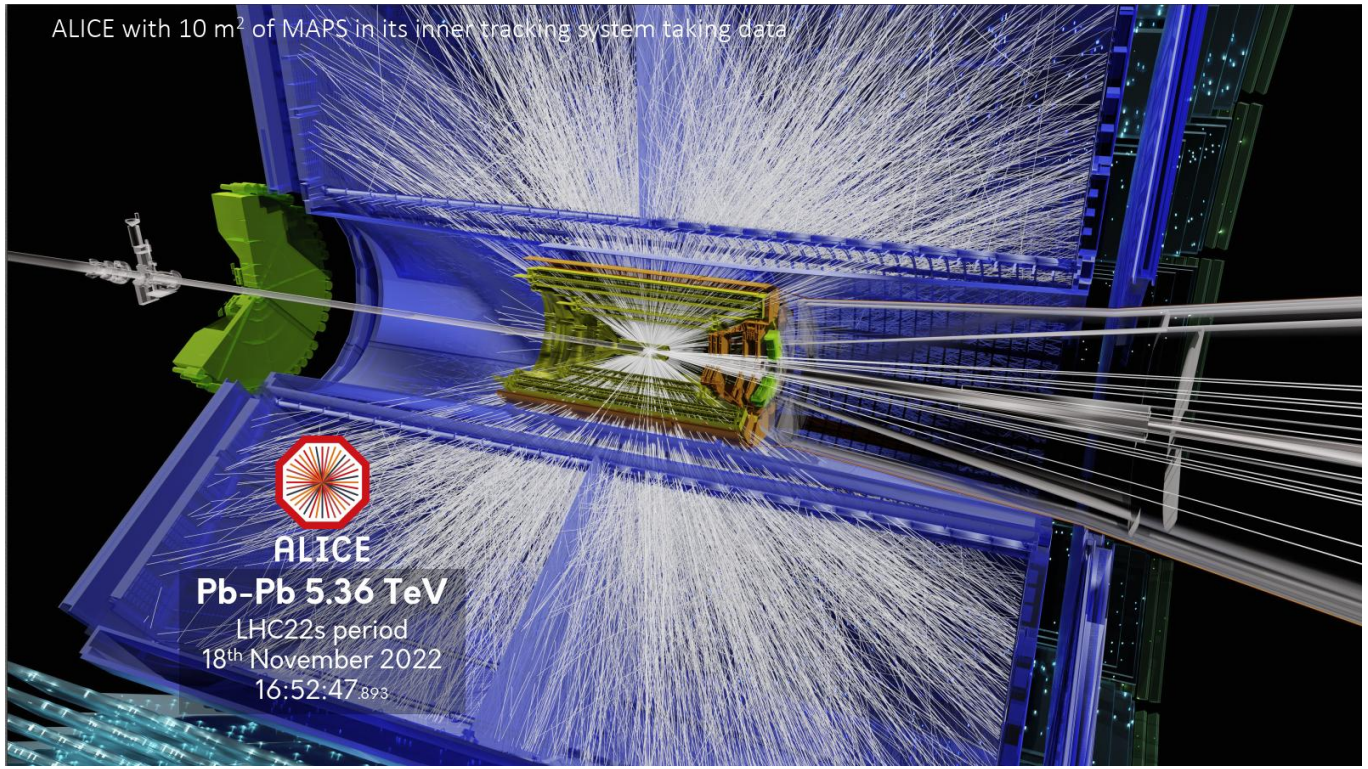
Monolithic active pixel sensors based on TPSCo 65 nm imaging technology: an overview of results and future challenges

Giacomo Ripamonti

The work presented here covers the activities of the CERN EP R&D WP1.2 team and benefited from massive contributions from the ALICE and monolithic CMOS sensor communities

Monolithic active pixel sensors

Monolithic active pixel sensors (MAPS) are crucial for current and future High Energy Physics detectors, due to their minimal material budget, low power consumption and low cost per unit area.



ALICE Inner Tracking System 2 (ITS2) is the first detector based on MAPS deployed at CERN.

The ALPIDE CMOS sensor for the ITS2 was implemented in the TowerJazz 180 nm imaging CMOS technology.

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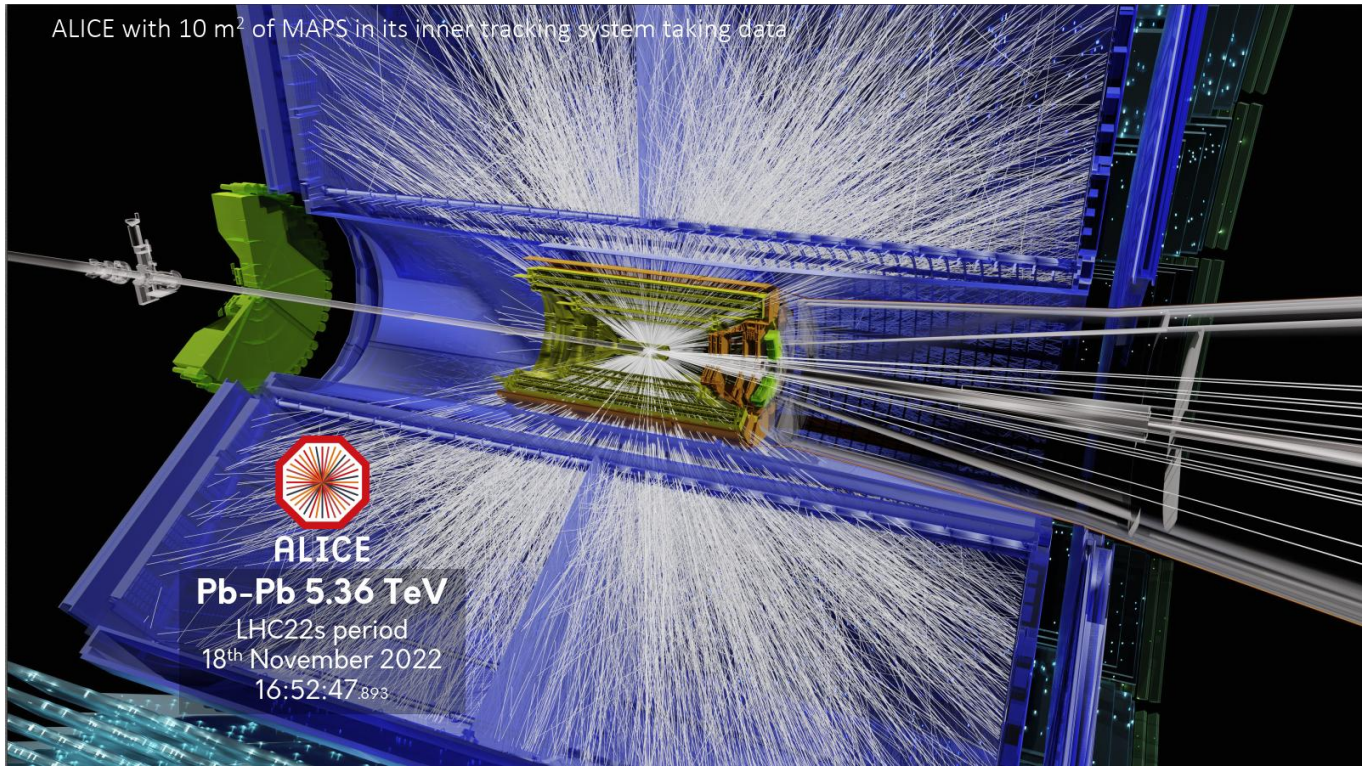

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More details on ITS2 in Jiyoung's talk:

J. Kim, "ALICE ITS2: Performance and Operational Experience"

R&D for monolithic active pixel sensors

CERN EP R&D WP 1.2 targets the development of monolithic CMOS sensors for future HEP detectors in sub-100 nm technologies to achieve smaller pixel pitch, higher data rate, increased radiation tolerance and fabrication of wafer-scale sensors on 300 mm wafers.

The first technology retained is the TPSCo 65 nm, and significant development in this technology was carried out in collaboration with the ALICE experiment for the upgrade of its vertex detector, ITS3.

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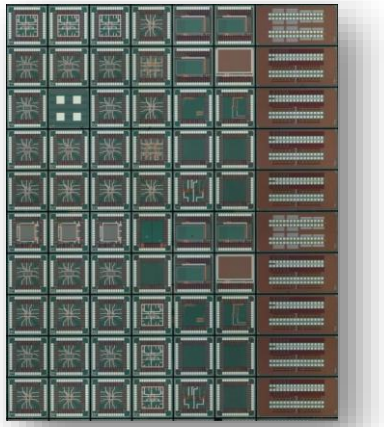
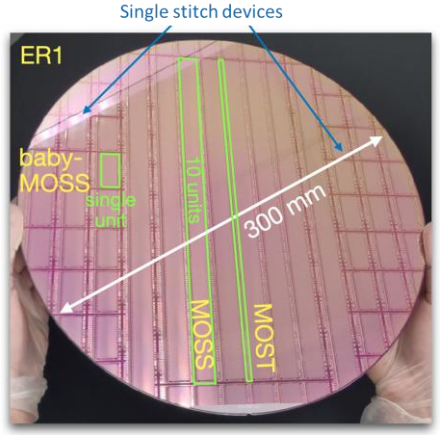
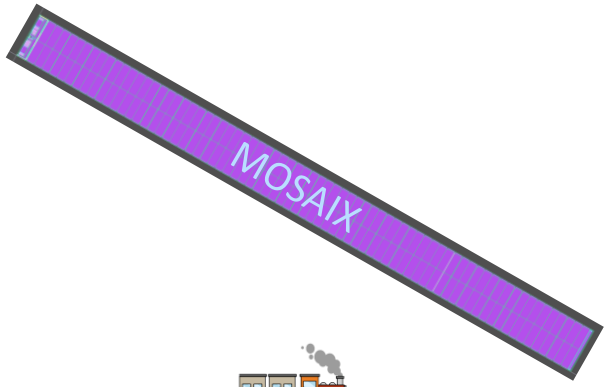
Main goals and activities:

- Design of wafer-scale stitched sensor (application in ITS3)
- Investigate new concepts for CMOS sensors:
  - Porting of hybrid pixel detector architecture into monolithic (Hybrid-to-Monolithic, H2M)
- Performance optimization for future applications
  - Fast timing
  - Low power
  - Radiation tolerance
- Provide support and access to TPSCo 65 nm imaging technology

Projects timeline (TPSCo 65 nm)







MPR2

Shared engineering run

WP 1.2 “rail”

ALICE “rail”

MLR1 (Multy-Layer Reticle, Dec 2020):

Learn about the technology, characterize pixels, transistors and building blocks

ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors

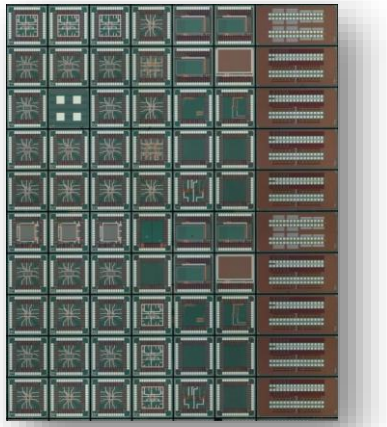
ER2 (Q2 2025):

Full-scale stitched sensor prototype for ALICE ITS3

ER3 (2026):

Stitched sensor production for ITS3 (ALICE-specific)

Projects timeline (TPSCo 65 nm)



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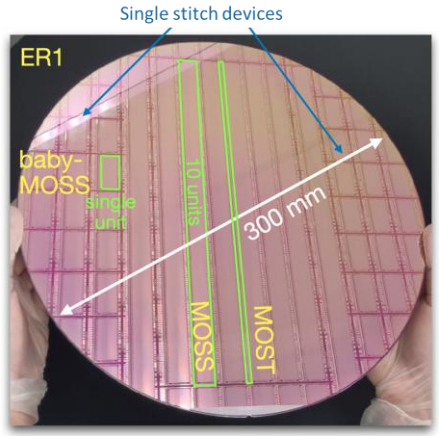
Learn about the technology, characterize pixels, transistors and building blocks

1.5 x 1.5 mm^2 test chips

>50 chiplets from: DESY, IPHC, RAL, NIKHEF, CPPM, Yonsei, CERN



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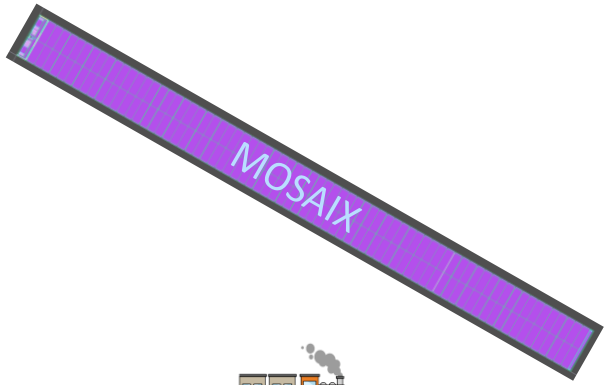

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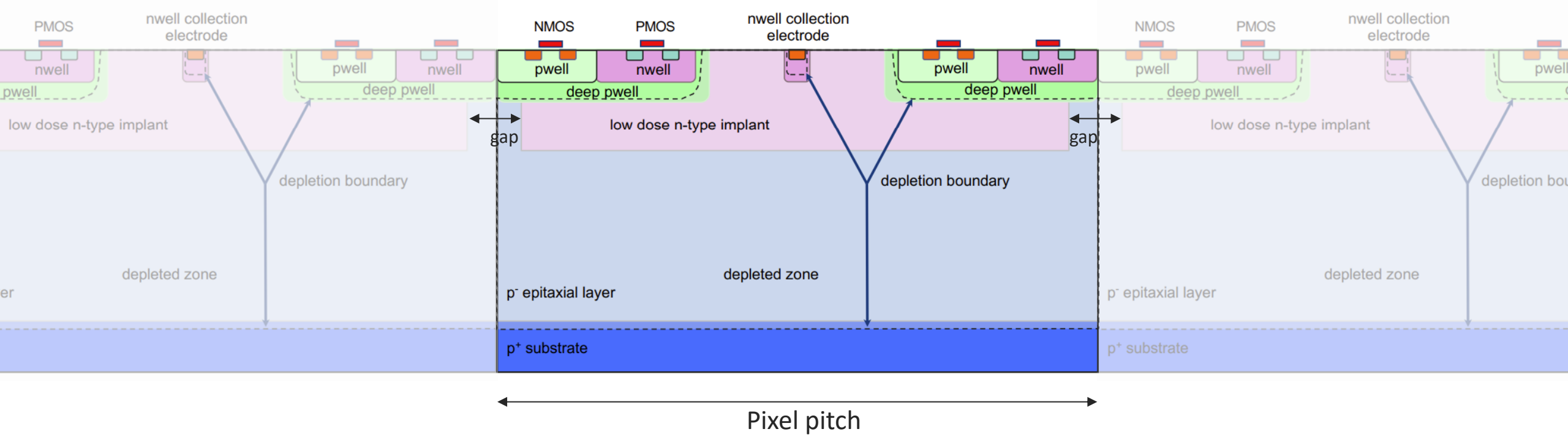
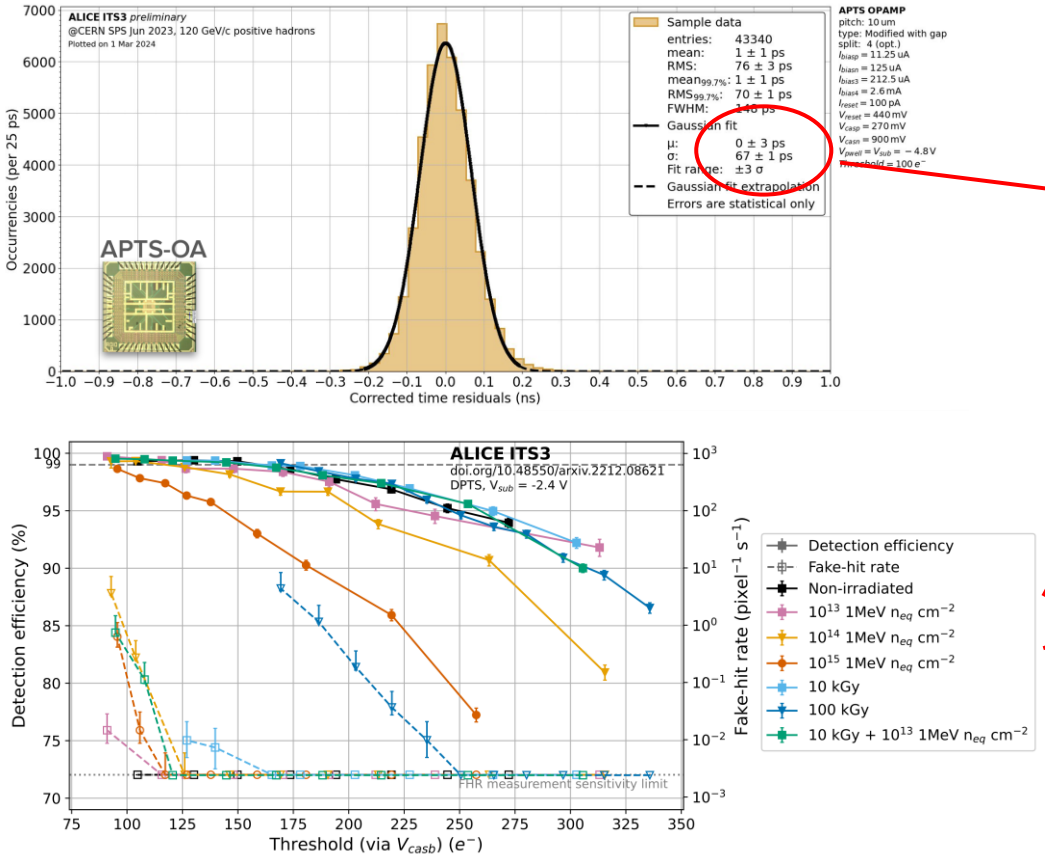
Sensor cross section

Sensor development in TPSCo 65 nm built on experience with TowerJazz 180 nm



MLR1: learning on sensor, front-end and readout



Lessons learned from MLR1:

- < 100 ps timing precision (sensor + front-end only) [2]
- Fully efficient sensor, analog front end, digital readout chain with 15 x 15 µm^2 pixel [3]
- Transistor total ionizing dose tolerance and SEU in line with other 65 nm technologies
- Proof-of-principle that we can reach ~ 99 % detection efficiency at $10^{15}\ 1MeV\ neq\ cm^{-2}$ at room temperature

[1] “Characterization of analogue Monolithic Active Pixel Sensor test structures implemented in a 65 nm CMOS imaging process”. In: Nucl. Instr. and Meth. A 1070 (2025), 169896. doi: 10.1016/j.nima.2024.169896.

[2] “Time performance of Analog Pixel Test Structures with in-chip operational amplifier implemented in 65 nm CMOS imaging process”, In: Nucl. Instr. and Meth. A 1070 (2025), 170034. doi: 10.1016/j.nima.2024.170034.

[3] “Digital pixel test structures implemented in a 65 nm CMOS process” , In: Nucl. Instr. and Meth. A 1070 (2025), 168589. doi: 10.1016/j.nima.2024.168589.

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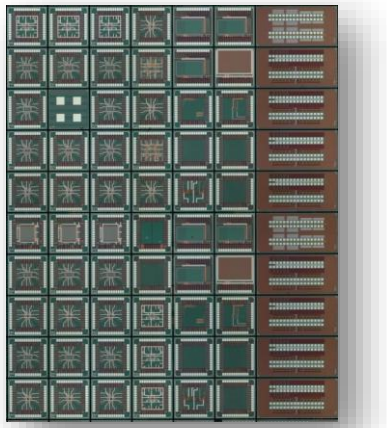

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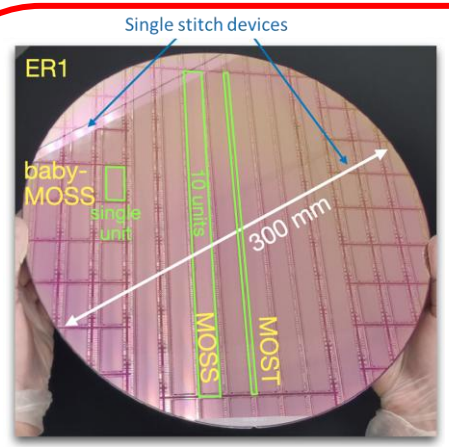


ER1 (Engineering Run, Dec. 2022):

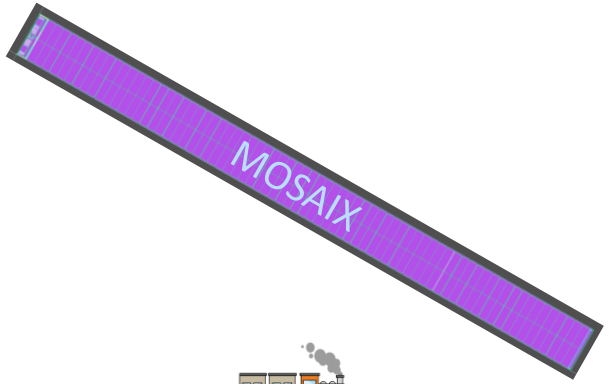
Prove we can design wafer-scale stitched sensors

MOSS (1.4 x 25.9 cm)

MOST (0.25 x 25.9 cm)

Hybrid-To-Monolithic (H2M)

51 chiplets from: DESY, IPHC, RAL, NIKHEF, SLAC, INFN, CERN



ER2 (Q2 2025):

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MPR2

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WP 1.2 "rail"

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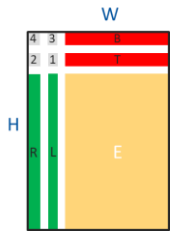
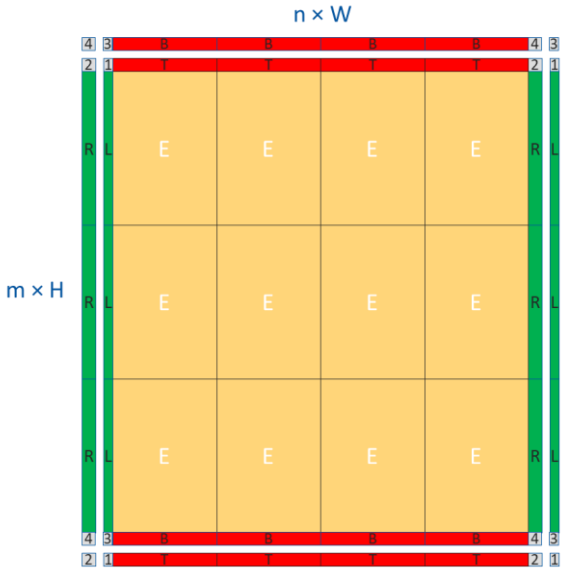
ER1: learning stitching and handling procedures

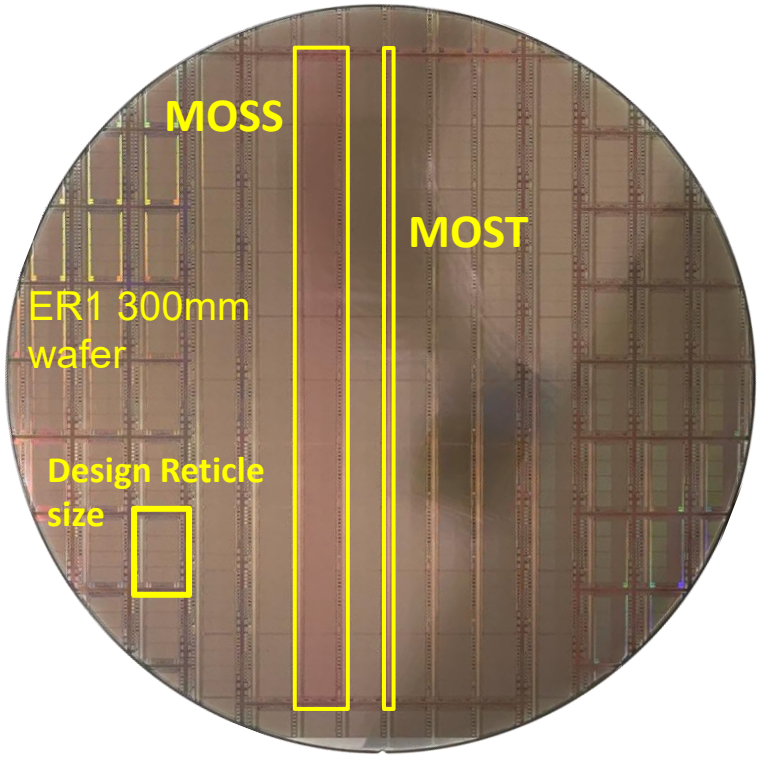
- Two wafer-scale stitched sensor chips
  - MOSS (Monolithic Stitched Sensor)
  - MOST (Monolithic Stitched Sensor with Timing)

Design Reticle
(typ. 2x3 cm)



Stitched circuit on wafer





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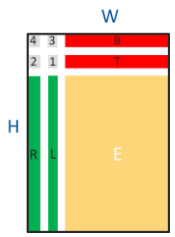
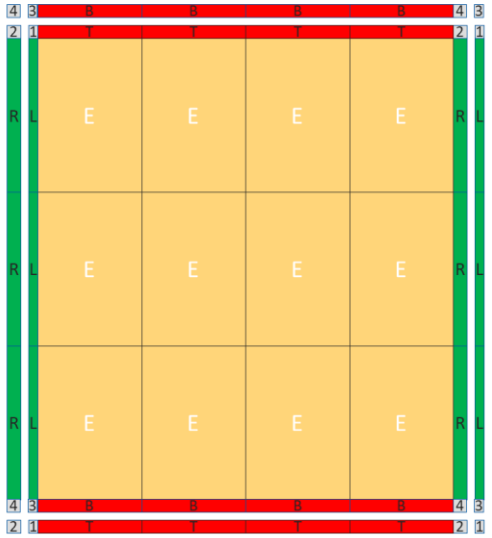
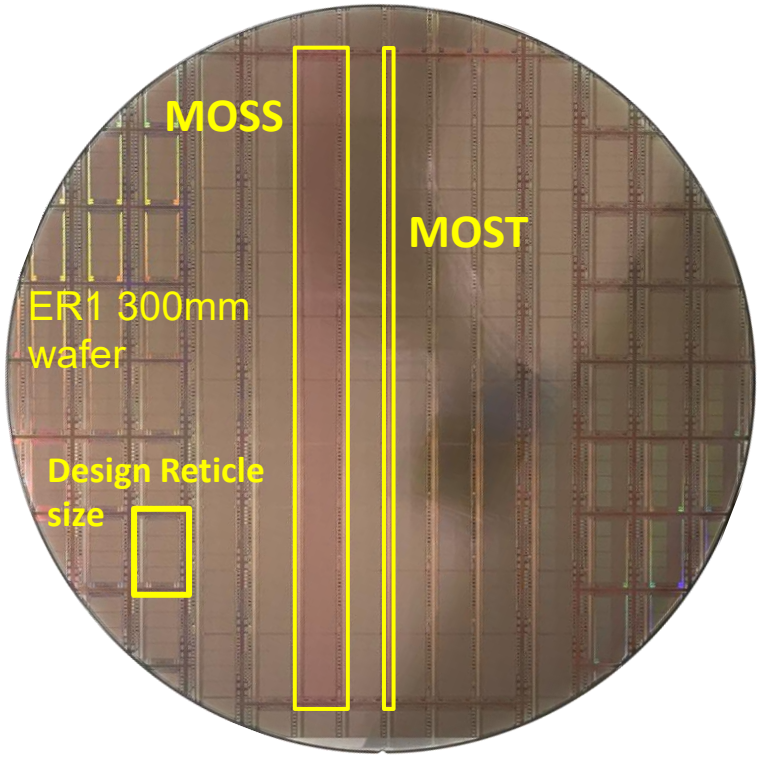
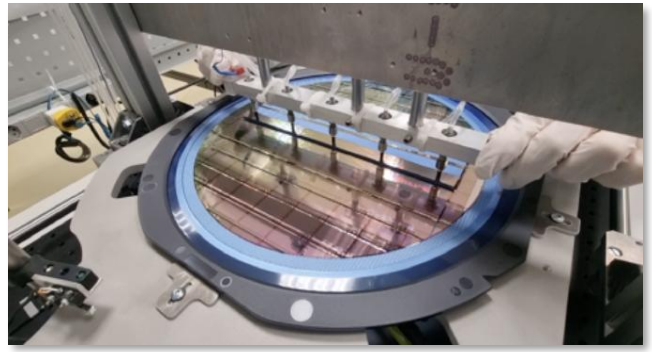


Stitched circuit on wafer
n × W
m × H





- Lots of learning on chip handling
- Several small test chips (1.5 mm × 1.5 mm)
  - H2M, PLL, pixel prototypes, fast serial links, SEU test chips, …

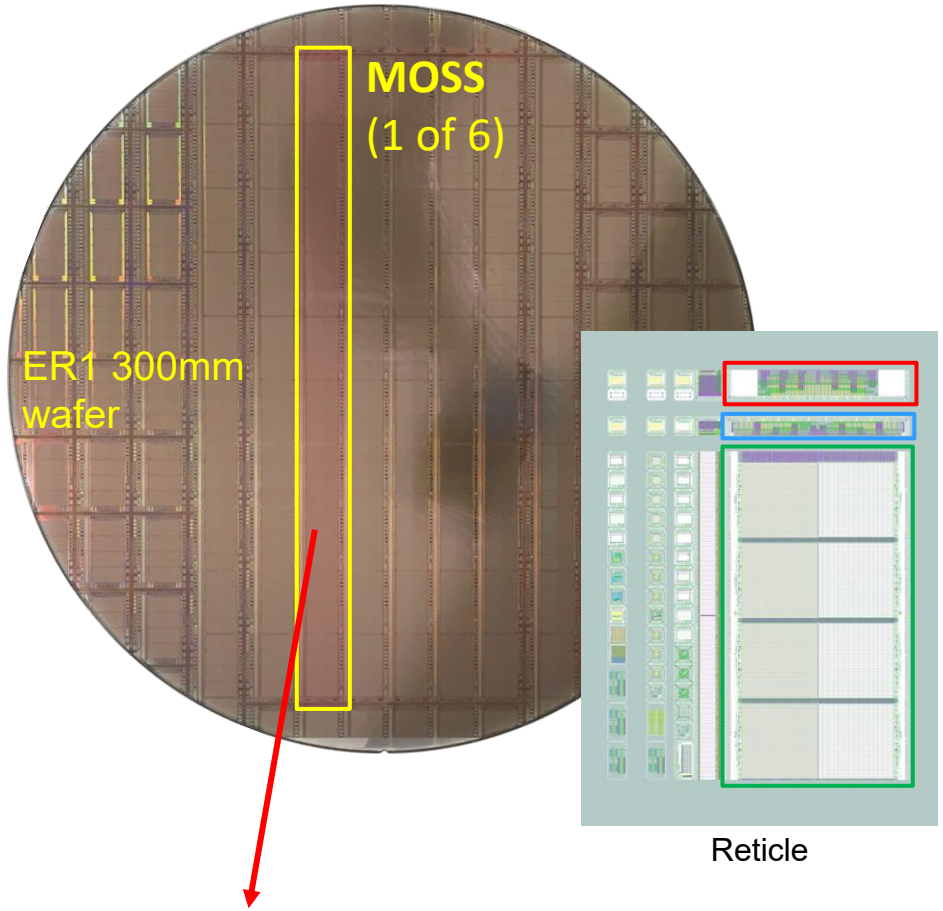


MOSS picking

MOSS (Monolithic Stitched Sensor)

"Full-size" prototype for ALICE ITS3
14 mm × 259 mm, 6.72 Mpixels
Conservative design and layout, study yield and uniformity

- MOSS building blocks:
  - Repeated Sensor Unit (hosting pixel matrices, each RSU can be powered, controlled and read-out independently or from the Left Endcap)
  - Left Endcap (allows to provide power, control and read data from the short edge, as required by ITS3)
  - Right Endcap (allows to provide power from the short edge)
- Two pixel pitches (22.5 µm and 18 µm) to study the effects of layout density



MOSS tests

Testing of MOSS carried out entirely by the ALICE community.

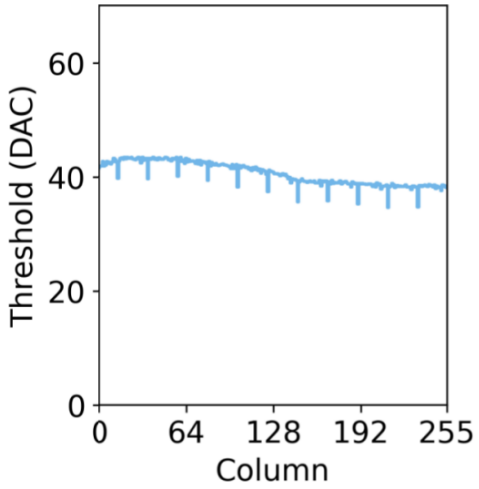
MOSS design has proven to be fully functional. Some short circuits observed related to a new, project-specific metal stack offered by the foundry, understood and addressed in a collaborative effort with the foundry, not expected in future runs.

Test beam results: ITS3 requirements in terms of efficiency and fake-hit rate met, also post-irradiation (radiation load estimated for ITS3 is ~ 400 krad, ~ 4 x 10^{12} 1 MeV n_{eq}/cm^2).

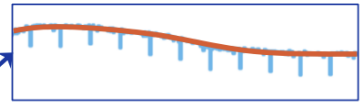
More details in Livia's talk:
L. Terlizzi, "ALICE Inner Tracking System 3 overview: from MOSS and MOST to the full-size MOSAIX sensor prototype "

MOSS – Learnings on matrix uniformity and couplings

Pixel threshold measured using on-pixel pulsing (charge injected by applying a voltage step to a capacitor connected to the pixel input)

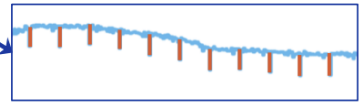


Two anomalies can be clearly distinguished



#1 Left to right smooth decrease (~2 DAC codes)

Voltage drop in the pulsing voltage explains this [5]



#2 Several downward spikes (~2-3 DAC codes)

A $\sim 3\ aF$ coupling from a digital signal to the pixel input happening in the highlighted columns explains the pattern [5]

Lots of learning from the test campaign of MOSS that have guided the design of its successor.

[5] S. Emiliani et al. “Investigation of non-idealities of pulsing circuitry in the ALICEITS3 MOSS monolithic sensor”. In: Journal of Instrumentation 19.12 (Dec. 2024), p. C12021. doi: 10.1088/1748-0221/19/12/C12021

MOST (Monolithic Stitched Sensor with Timing)

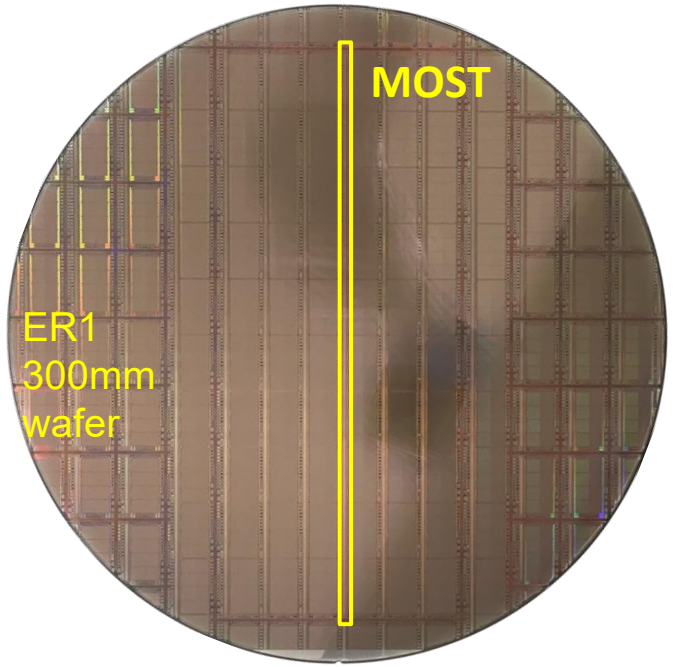
MOST other stitched sensor on ER1

- 259 x 2.5 mm
- 18 micron pixel pitch

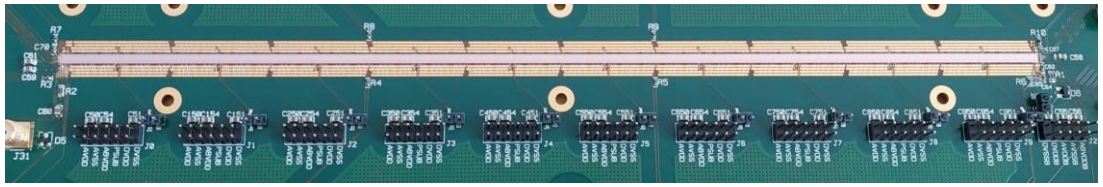
Main differences with MOSS

- Powering: global power distribution with power switches to switch off faulty parts, very densely designed circuit
- Asynchronous, hit-driven readout for timing information + low power consumption
- High-speed data transmission on chip
- Reverse bias is applied to the sensor via the front-end

Significant testing effort, also at NIKHEF, more details in [6]

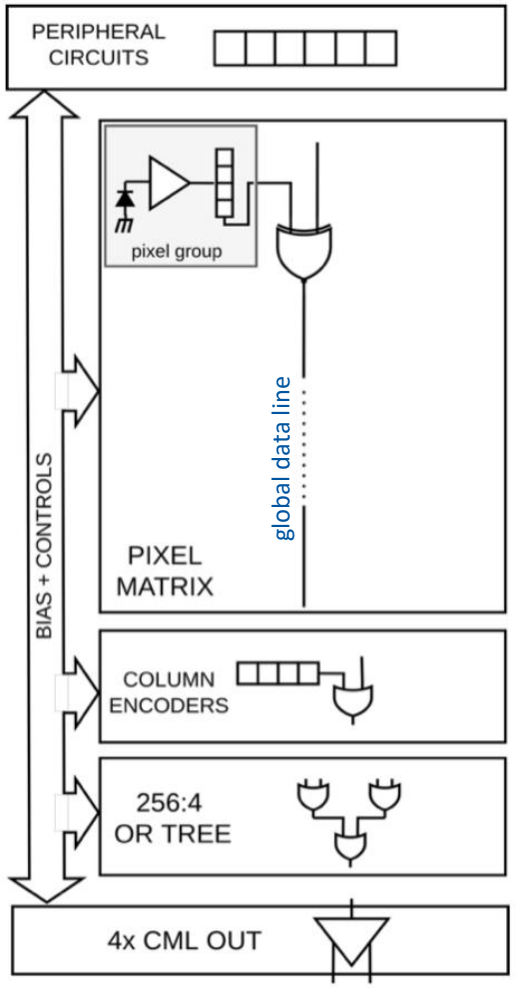


MOST on carrier board



[6] M. Selina. “Exploring ALICE ITS3 MOST: Early Results on Power Segmentation and Asynchronous Readout for Timing in a Monolithic Stitched Sensor”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024), https://arxiv.org/pdf/2504.13696

MOST: asynchronous readout



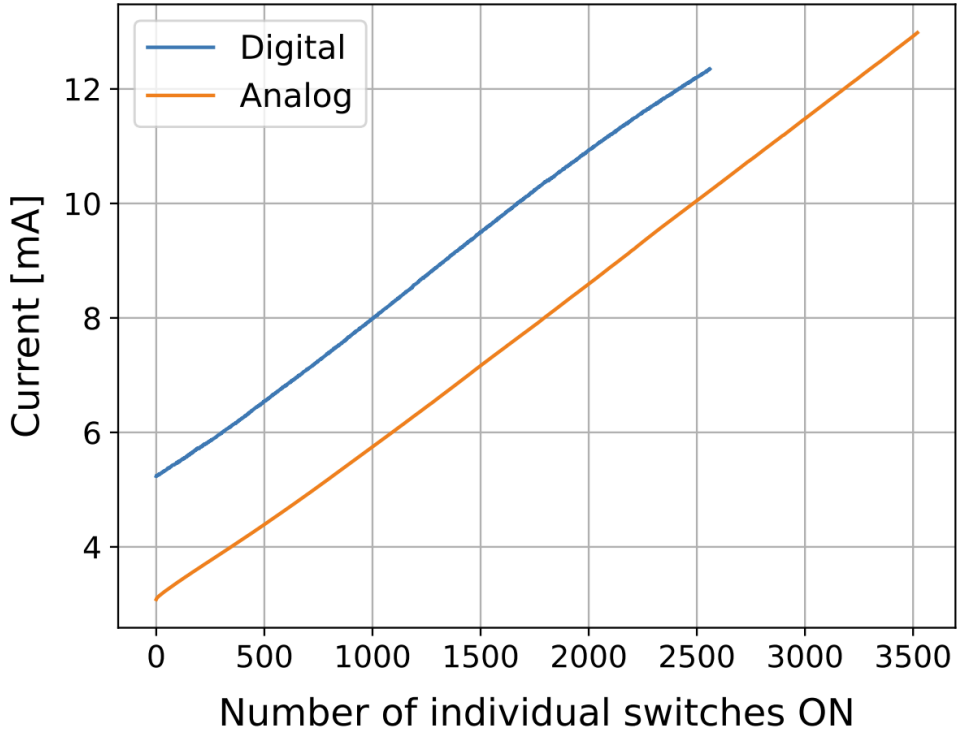
- Groups of 4 pixels
- As soon as a pixel is hit, its address is shipped through a global data line to the column encoders
- The column encoders append the column address, and the data are shipped out through a CML driver

The asynchronous readout of MOST allows to study to what degree the timing is preserved in the long-distance transmission

MOST: yield & powering

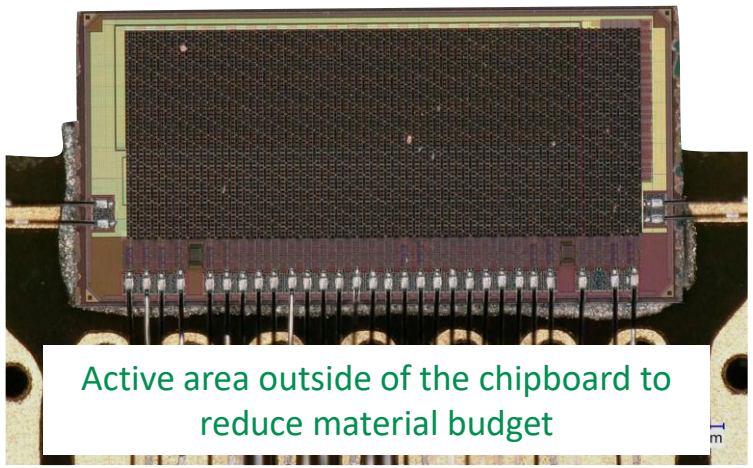
- If MOST can be powered (functional global power network), fully functional
  - In that case pixel yield better than 99.98 %, despite the highly-dense layout. This result paves the way for high-density, large-area designs

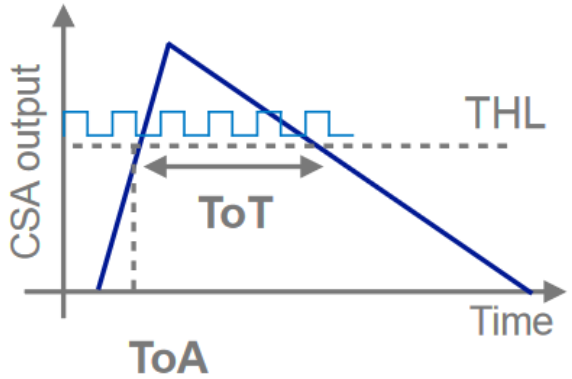
MOST current consumption vs. powered pixel groups (powered through power switches)



H2M (Hybrid-to-Monolithic)

- Technology demonstrator designed by WP 1.2, DESY and IFAE
- Ports a **hybrid pixel detector architecture into a monolithic chip**





- **Pixel pitch: 35 µm in 64x16 pixel matrix**
- **Total thickness:** ~ 50 µm (epi ~10 µm)

- 4 Non-simultaneous acquisition modes
  - 8 bit **ToT**,
  - 8 bit **ToA** (100 MHz clock - 10 ns binning),
  - **counting** (#number of hits above threshold),
  - **triggered**.
- Readout: 40 MHz clock, frame-based without zero-suppression.

[7] S. Ruiz Daza at al. “The H2M Monolithic Active Pixel Sensor - characterizing non-uniform in-pixel response in a 65 nm CMOS imaging technology”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024), https://arxiv.org/abs/2502.06573

H2M - Global performance results

- **Various thicknesses** were tested
  - Single-die backside thinning
  - **No performance degradation**

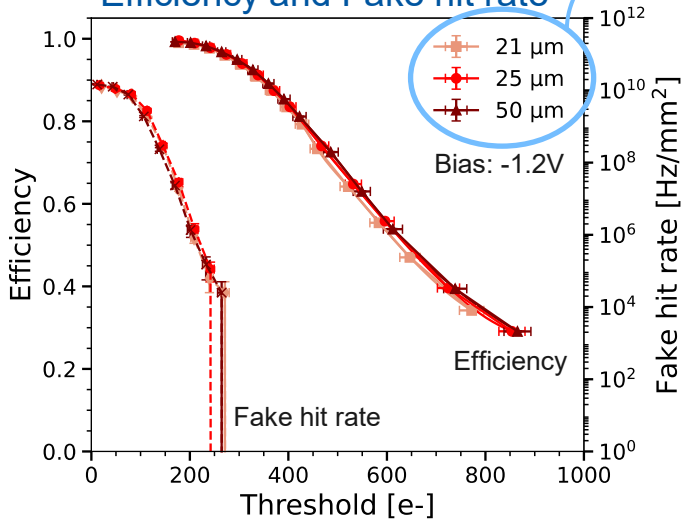
- Chip can be operated with full efficiency. Some work needed to improve the fake hit rate

- **Thin epitaxial layer** and **large pitch**
  → Mostly single-pixel clusters
  → Spatial resolution **($\sim$pitch/$\sqrt{12}$)** **dominated by the large pitch** of 35 µm

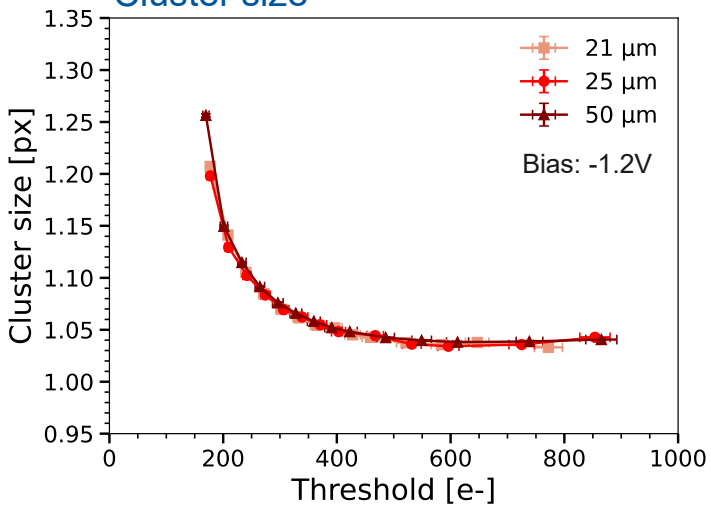
- Time resolution **limited by non-uniformity of charge collection**

Total chip thickness

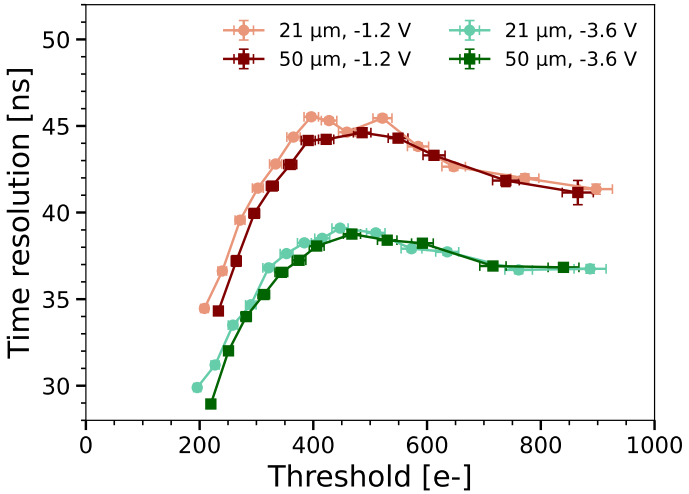
Efficiency and Fake hit rate



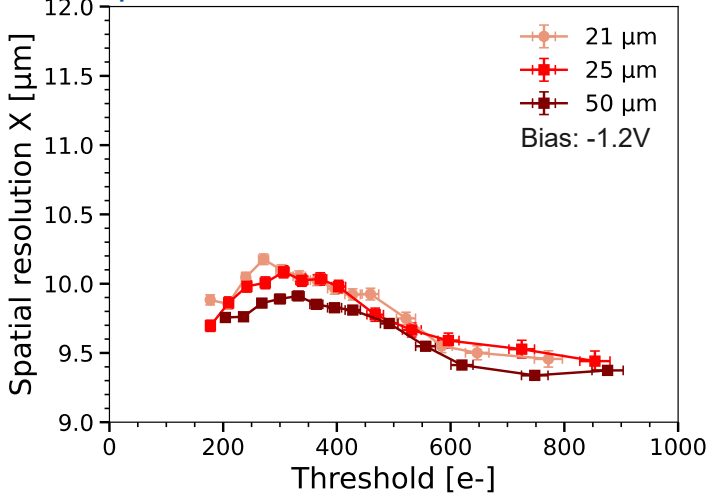
Cluster size



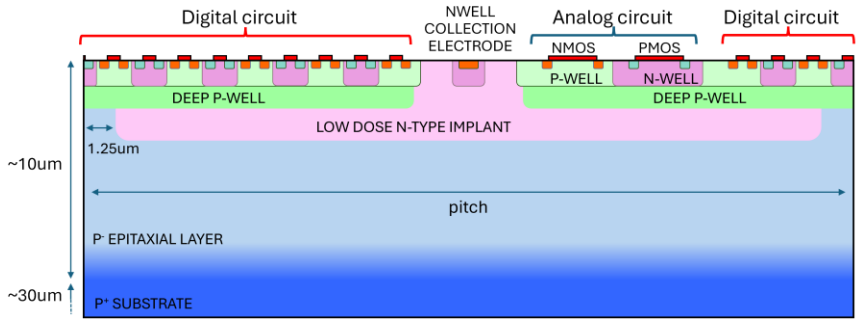
Time resolution



Spatial resolution

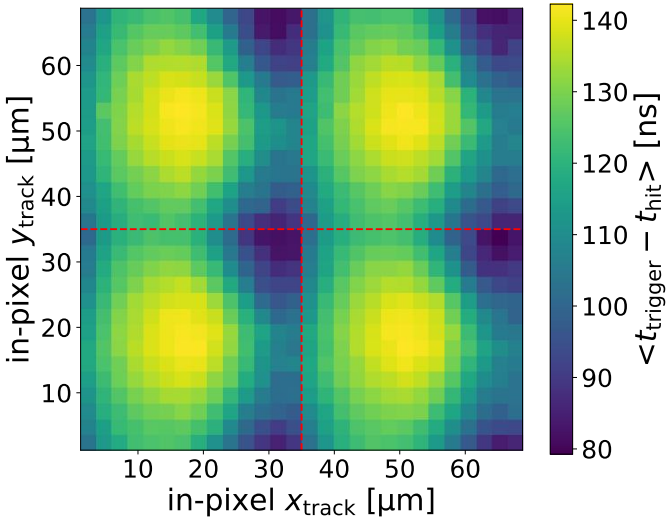


H2M - Non-uniform in-pixel response

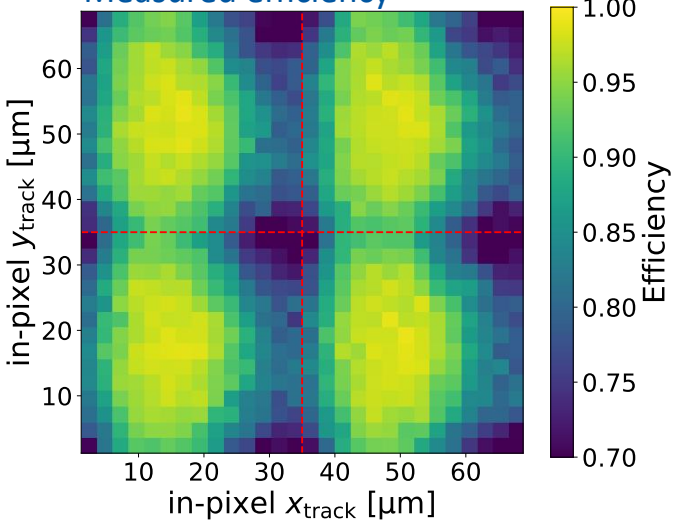


- Related to the size and location of the n-wells of the circuitry, leading to localized low-field regions with slower charge collection
- Mitigated with optimized operating parameters (larger sensor bias, lower threshold, lower reset current)
- Confirmed in simulation (TCAD + Monte Carlo + Spice) [8]

Measured time residual

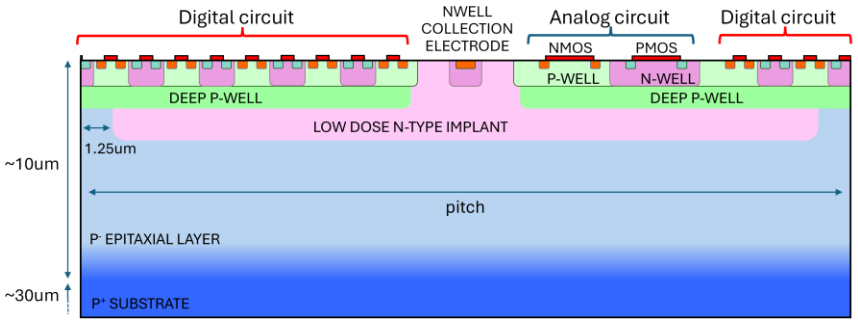


Measured efficiency



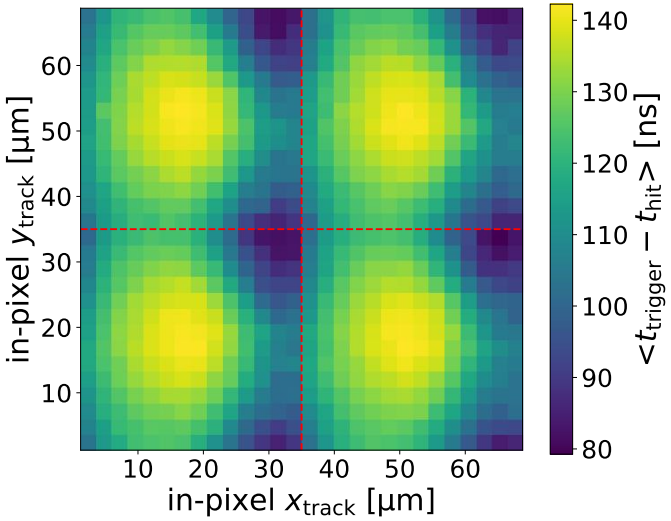
[8] C. Lemoine et al. “Impact of the circuit layout on the charge collection in a monolithic pixel sensor”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024), https://arxiv.org/abs/2503.21853

H2M - Non-uniform in-pixel response

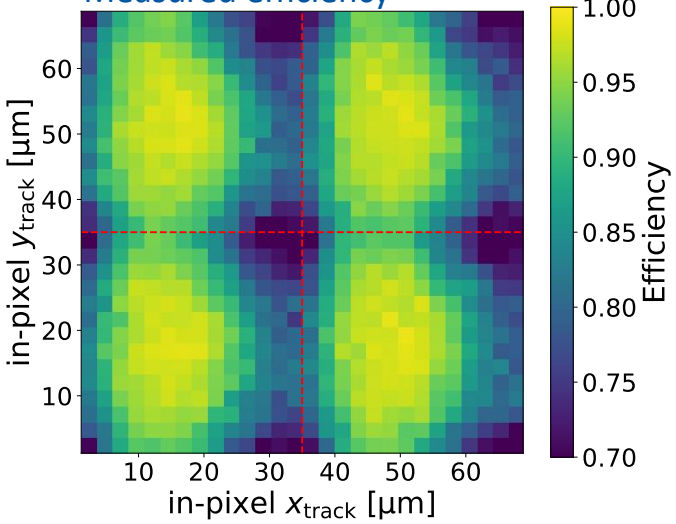


- Related to the size and location of the n-wells of the circuitry, leading to localized low-field regions with slower charge collection
- Mitigated with optimized operating parameters (larger sensor bias, lower threshold, lower reset current)
- Confirmed in simulation (TCAD + Monte Carlo + Spice) [8]

Measured time residual



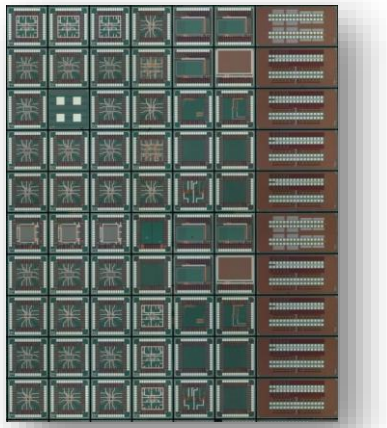
Measured efficiency



- This effect led to useful learnings on the challenges to design “large” efficient pixels
- New simulation strategies have been devised to understand the issue: crucial tool for future developments

[8] C. Lemoine et al. “Impact of the circuit layout on the charge collection in a monolithic pixel sensor”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024), https://arxiv.org/abs/2503.21853

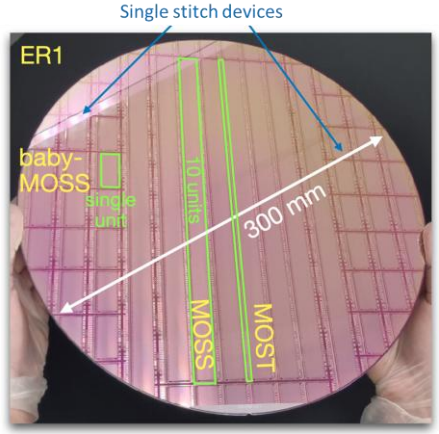
Projects timeline (TPSCo 65 nm)



MLR1 (Multy-Layer Reticle, Dec 2020):

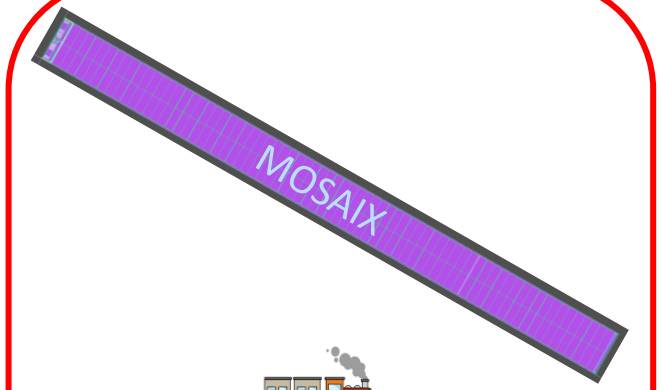
1.5 x 1.5 mm^2 test chips

Learn about the technology, characterize pixels, transistors and building blocks



ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors



ER2 (Q2 2025):

Full-scale stitched sensor prototype for ITS3

MOSAIX (1.9 x 26.6 cm)

~30 chiplets from: IPHC, SLAC, CPPM, BNL, INFN, Universität Heidelberg, CERN

MPR2

Shared engineering run

WP 1.2 "rail"

ALICE "rail"

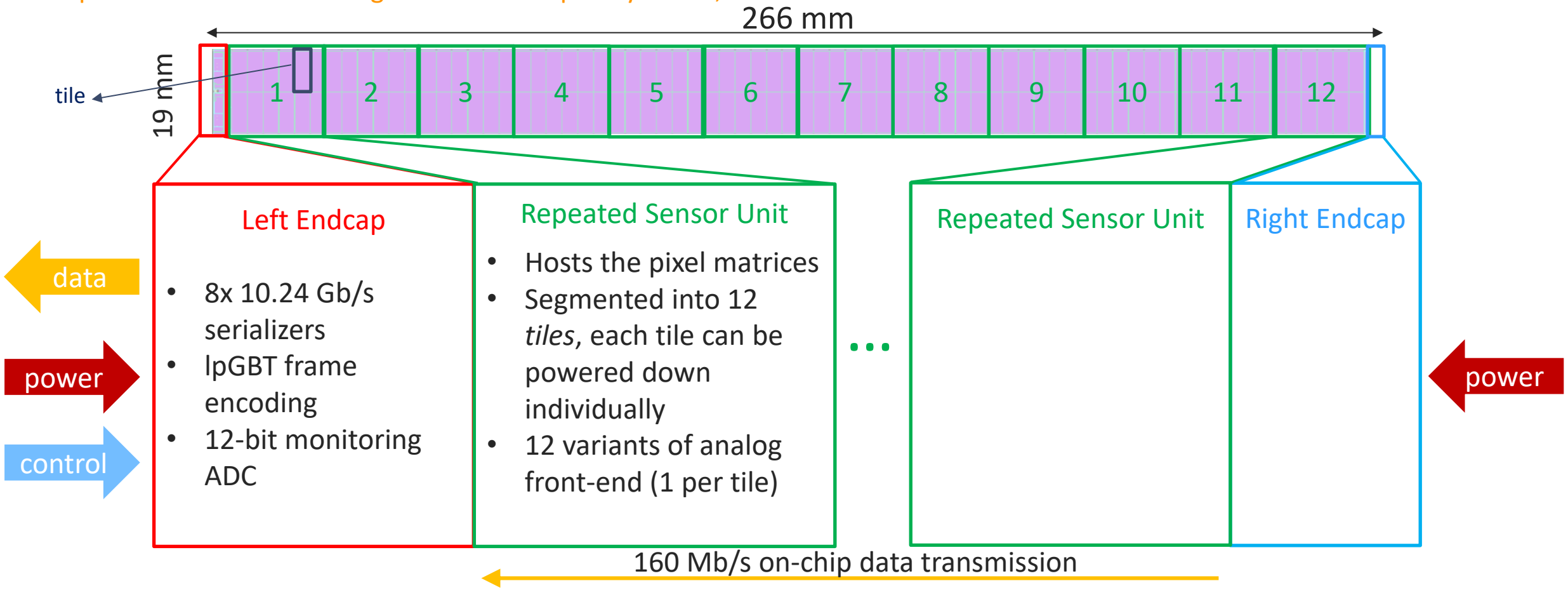
ER3 (2026):

Stitched sensor production for ITS3 (ALICE-specific)

MOSAIX (MOnolithic Stitched Active pIXel)

MOSAIX is the full-size, full-functionality, stitched sensor prototype for ALICE ITS3. 22.8 x 20.8 µm pixels, 9.97 Mpixels. MOSAIX inherits some of its features from MOSS (synchronous read-out, conservative layout) and MOST (power segmentation, data transmission on chip), but it includes many more complex functionalities.

Unprecedented level of integration and complexity in HEP, ~ 3 bn transistors



[9] P. Vicente Leitao. “Development of the MOSAIX chip for the ALICE ITS3 upgrade”. In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).

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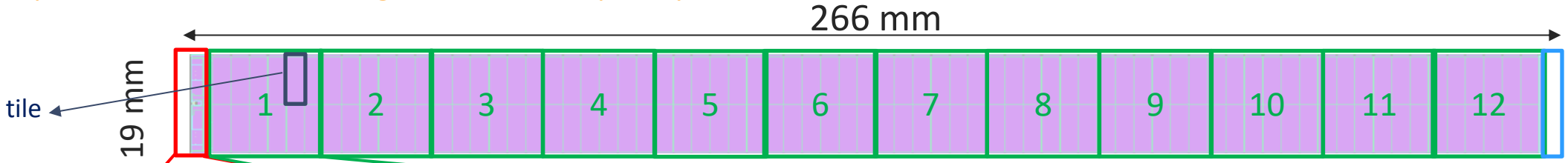


data

power

control

Left Endcap

- 8x 10.24 Gb/s serializers
- lpGBT frame encoding
- 12-bit monitoring ADC

Repeated Sensor Unit

- Hosts the pixel matrices
- Segmented into 12 *tiles*, each tile can be powered down individually
- 12 variants of analog front-end (1 per tile)

More details in Jelena's talk:

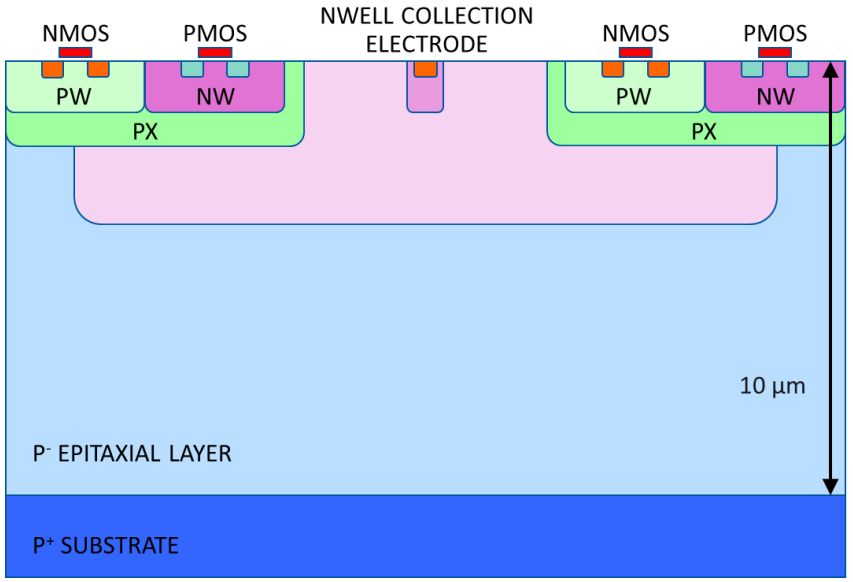
J. Lalic, "ALICE ITS3 MOSAIX stitched wafer-scale sensor – Implementation challenges and solutions"

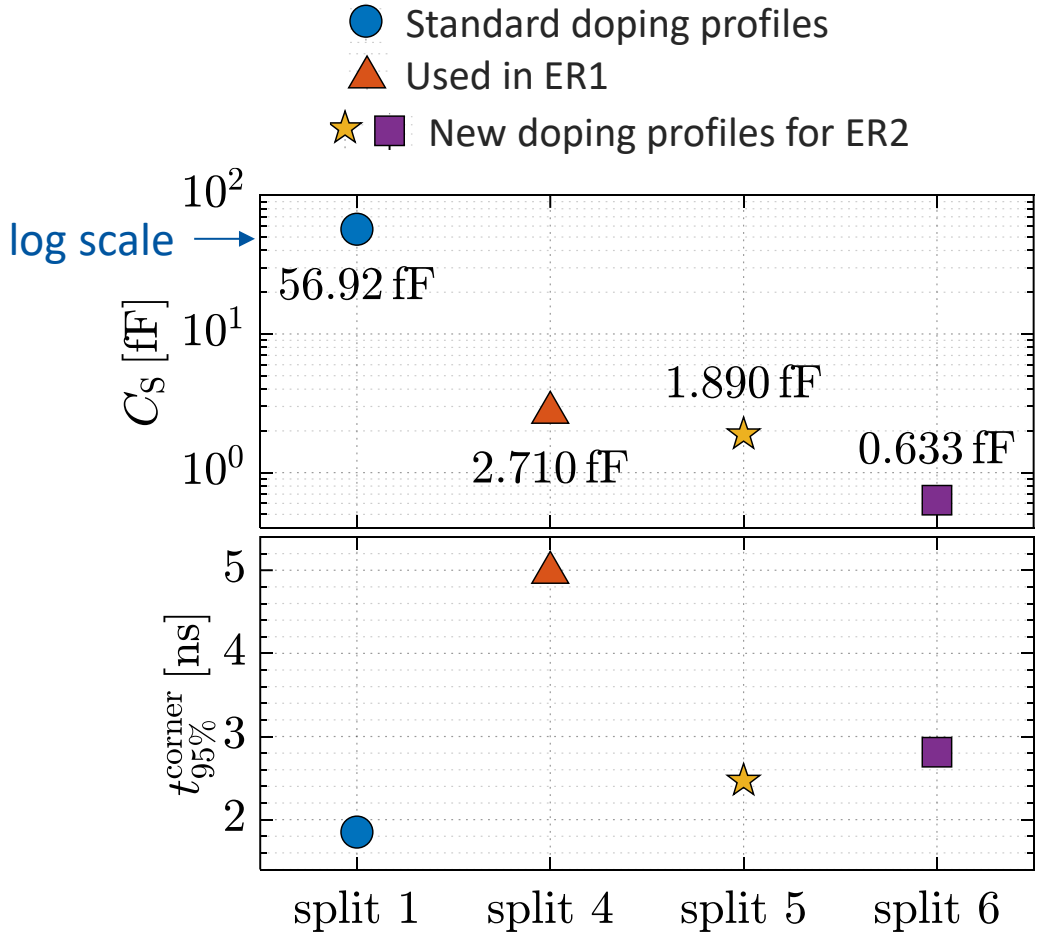
[9] P. Vicente Leitao. "Development of the MOSAIX chip for the ALICE ITS3 upgrade". In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).

Sensor optimization for MOSAIX

For HEP applications, the sensor is optimized (by modifying its doping profiles) working in close collaboration with the foundry.

<u>Goal:</u> minimize sensor capacitance C_S, minimize collection time $t_{95\%}^{corner}$





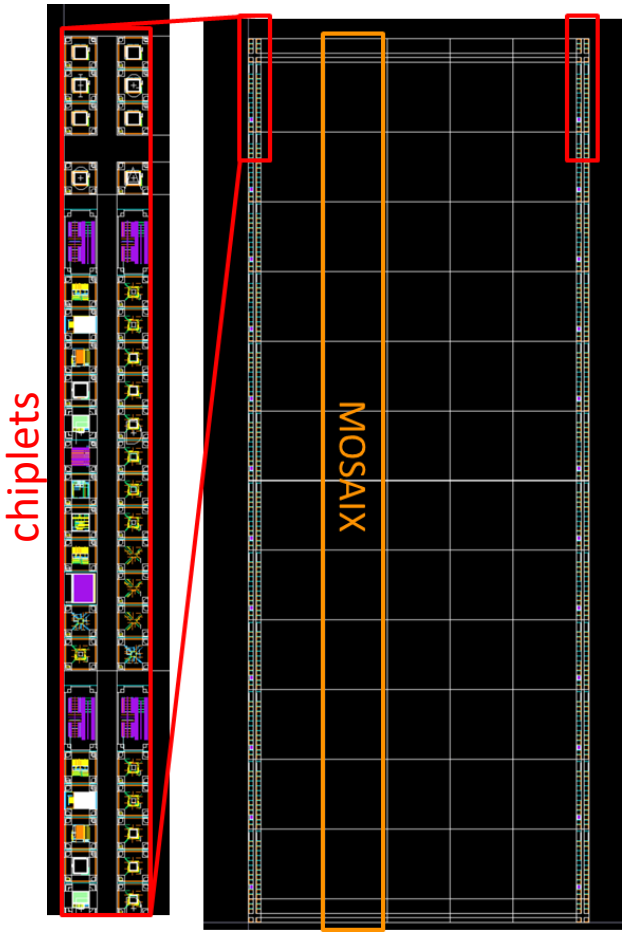
An additional sensor split for developments beyond ITS3 is also included in ER2

[10] G. Borghello. “Optimization of monolithic pixel sensors for high energy physics applications using 3D TCAD simulations”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024).

ER2: status and plans towards ER3

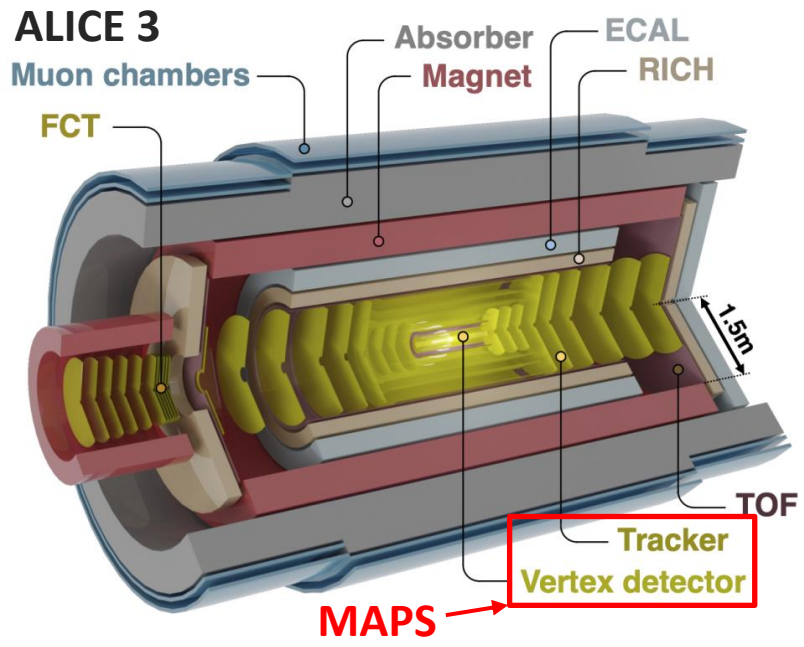
- ER2 (including MOSAIX and ~30 chiplets from IPHC, SLAC, CPPM, BNL, INFN, Universität Heidelberg, CERN) submitted in July 2025
- Chiplets will be used to test circuitry and sensor optimization
- The testing campaign on MOSAIX will identify the best sensor (3 variants) + front-end (12 variants) combination
- The final version of MOSAIX is foreseen to be submitted in 2026 (ER3)

Chip placement on wafer (ER2)

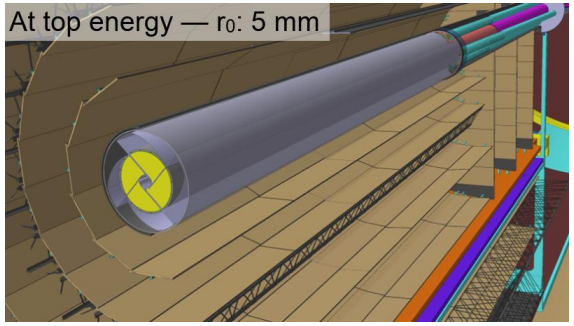


Challenges for detectors beyond ITS3

Monolithic active pixel sensors are foreseen to be used in future HEP detectors (ALICE3, FCC-ee detectors, …).



Vertex detector: r_0 = 5 mm for innermost layer

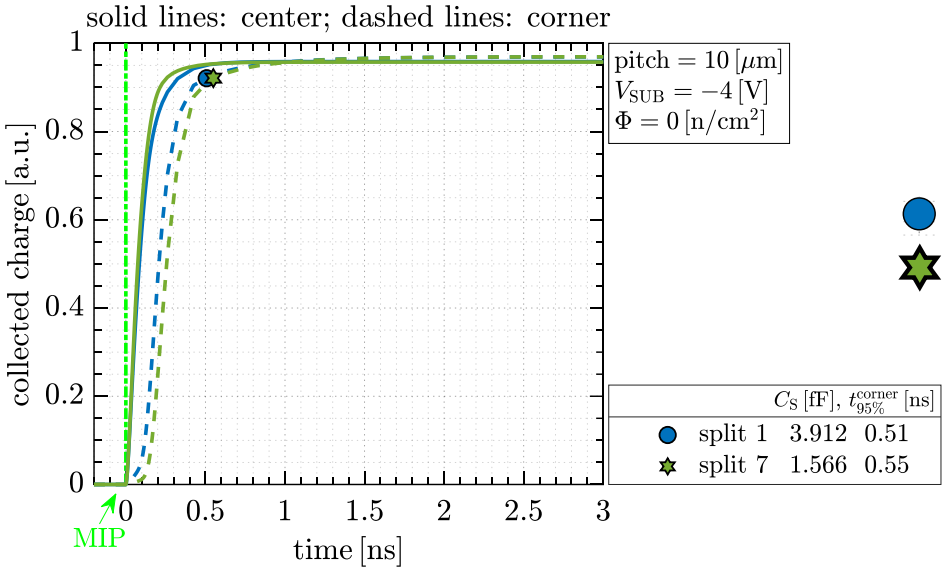


R&D for future MAPS driven by the requirements of the inner layers of ALICE3:

- Pixel pitch of 10 µm (pixel area < ¼ compared to MOSAIX)
- Total power consumption < 70 mW/cm^2 (compared to 40 mW/cm^2 in MOSAIX with a more than 4 times larger, 20.8 µm x 22.8 µm pixel)
- ≈ 1 MHz/mm^2 particle hit rate
- Time resolution < 100 ns RMS
- Radiation tolerance: 1e16 1 MeV n_{eq}/cm^2 + 300 Mrad (4e12 1 MeV n_{eq}/cm^2 + 400 krad for MOSAIX)
- Further minimization of dead area

Developments towards ALICE3

- A sensor optimized for 10 µm pitch to address the ALICE3 vertex detector needs has been designed and prototyped in ER2



- Standard doping profiles
- Optimized doping profiles targeting application in vertex detector of ALICE3

- Front-end circuits that achieve improved speed for the same power compared to MOSAIX and fit in a 10 µm x 5 µm area including the collection electrode are in development

- Readout architectures that minimize the power consumption are being studied

- Further minimization of the dead area needed: effort to design a periphery-less sensor with biasing and read-out circuitry embedded in the pixel matrix

Support for TPSCo 65 nm imaging technology

WP 1.2 provides access and support to TPSCo 65 nm

Design

- PDK (Physical Design Kit) for analog designs, DDK (Digital Design Kit) for digital designs, implementation flow, design rules (DRC/LVS decks from the foundry, customized/extended at CERN)
- Libraries for digital design, padring, sensor layout …
- Special design rules for special layers needed for sensor/pixel matrix
- Review of chiplets and suggestions for improvement/corrections

Interface with the foundry

- Technical and commercial, see also admin

Admin

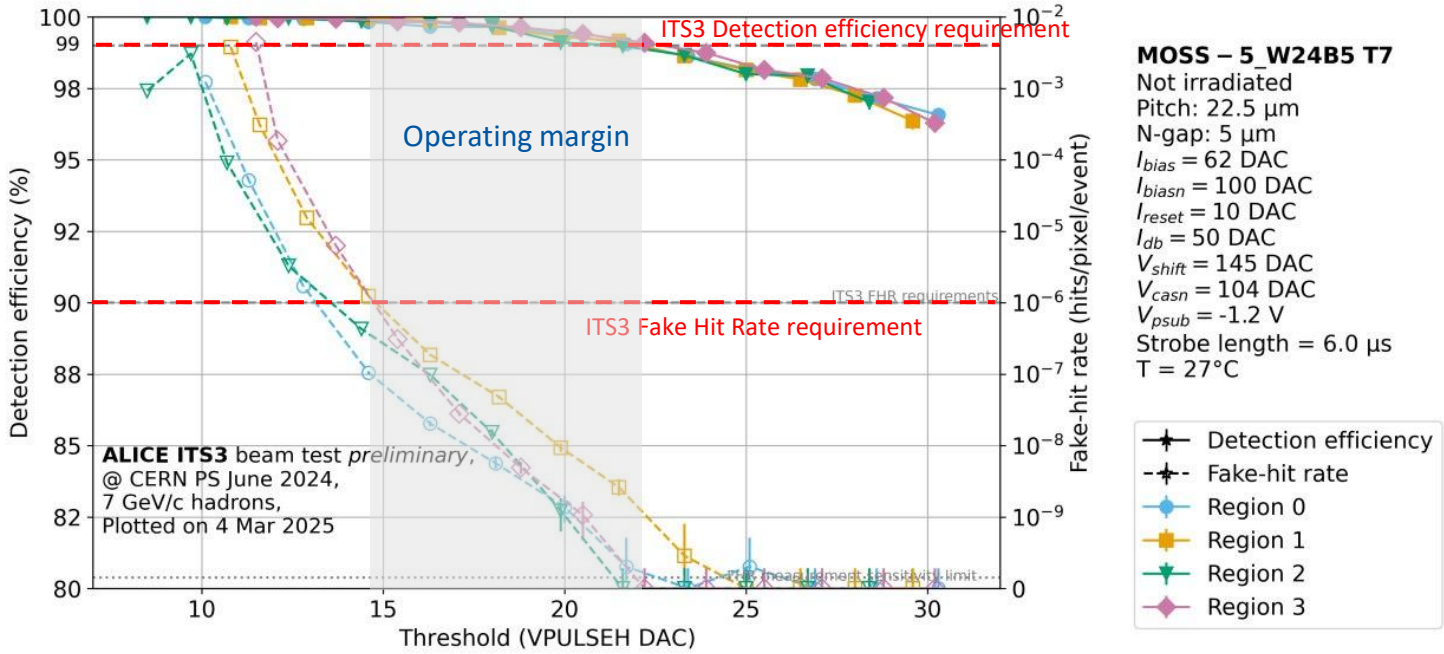
- Procurement, offers, etc
- NDA, export declarations, compliance letters, etc
- Need more work on design sharing

Take home messages

- WP 1.2 in synergy with the ALICE experiment demonstrated the feasibility of stitched monolithic CMOS sensors for HEP applications (MOSS, MOST)
- The design of the MOSAIX stitched sensor prototype for the new ALICE vertex detector (ITS3) has been finalized. It features unprecedented integration and complexity in the HEP community.
- The H2M project demonstrated the feasibility of porting hybrid pixel detector architecture into a monolithic chip. It also successfully demonstrated the sensor functionality for thicknesses < 50 µm and highlighted the challenges of designing “large” pixels
- R&D activities for detectors beyond ITS3 are being ramped up, driven by requirements of vertex detector of ALICE3
- WP 1.2 provides access and support to the TPSCo 65 nm imaging technology. WP 1.2 is starting the organization of MPR2 (Multi-Project Run, TPSCo 65 nm), gathering interest from HEP institutes and preparing the administrative framework.
- Link with experiments foreseeing large detectors is important, as foundries are ultimately interested in volume

Backup

MOSS – test beam results



Before irradiation: good operating margin.

After irradiation: satisfactory operating margin at the radiation load estimated for ITS3 (~ 400 krad, ~ 4 x 10^{12} 1 MeV n_{eq}/cm^2, see [4]).

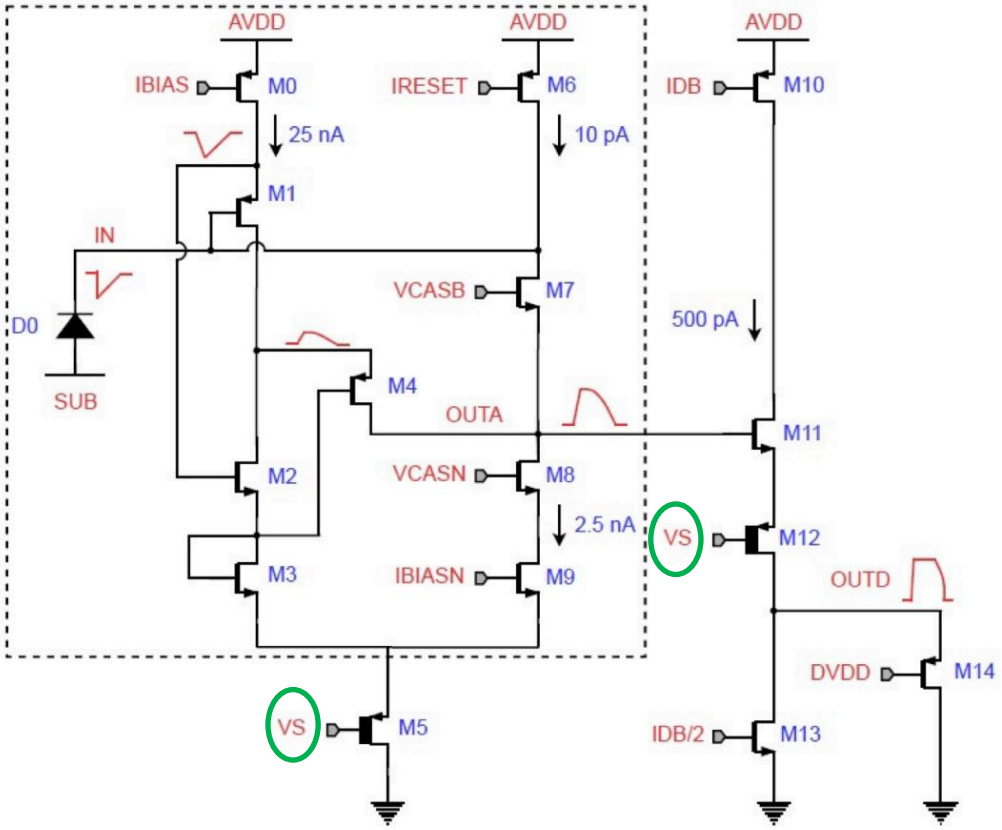
[4] L. Terlizzi. “Characterization of silicon Monolithic Stitched Sensors (MOSS) for the ALICE ITS3 for the LHC Run 4”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024).

MOST: front end and reverse substrate bias

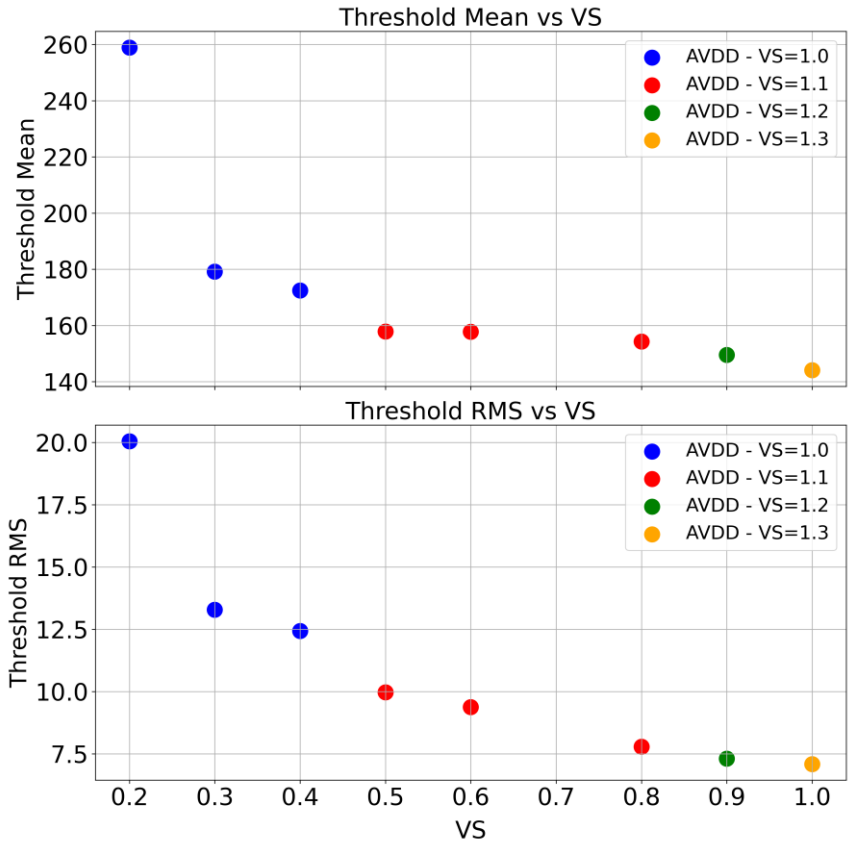
A larger VS increases the reverse bias of the sensor: the circuit ground can be tied to the substrate, greatly simplifying the design.

Increasing VS may require a larger AVDD, leading to larger power consumption.

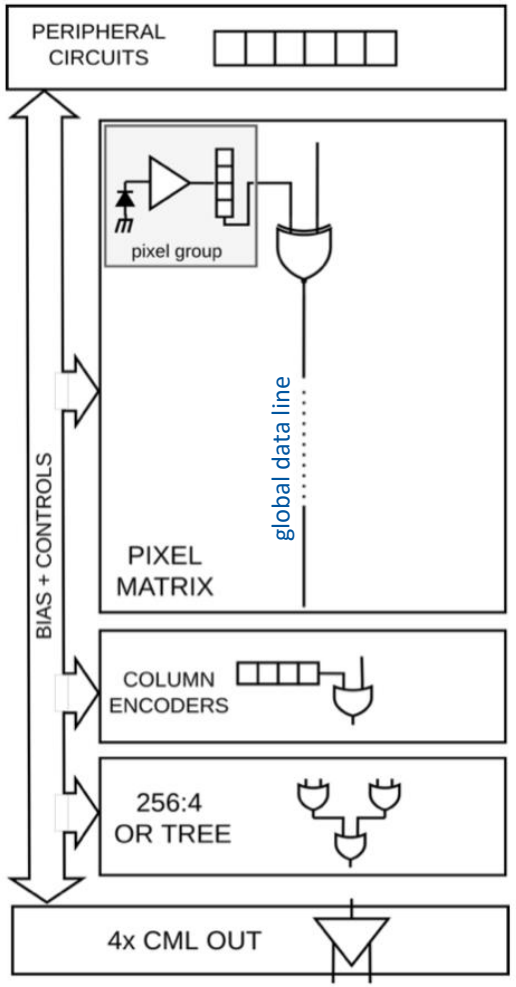
Front-end schematic



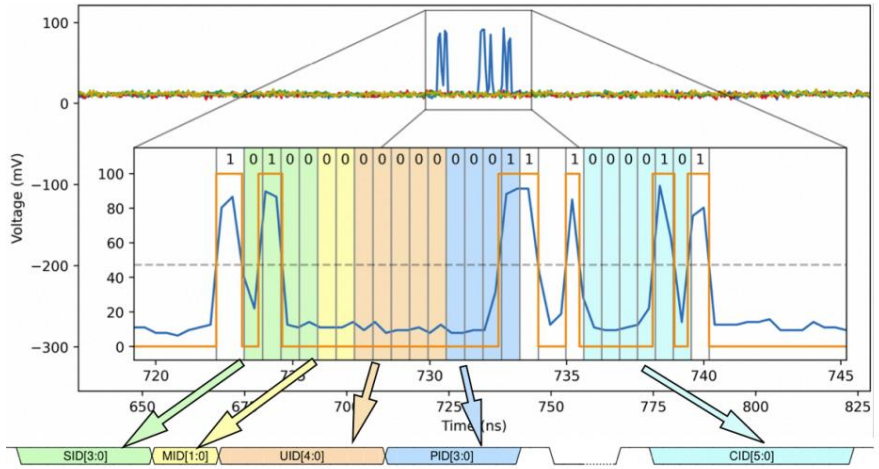
Increasing VS reduces the threshold and the threshold mismatch



MOST: asynchronous readout



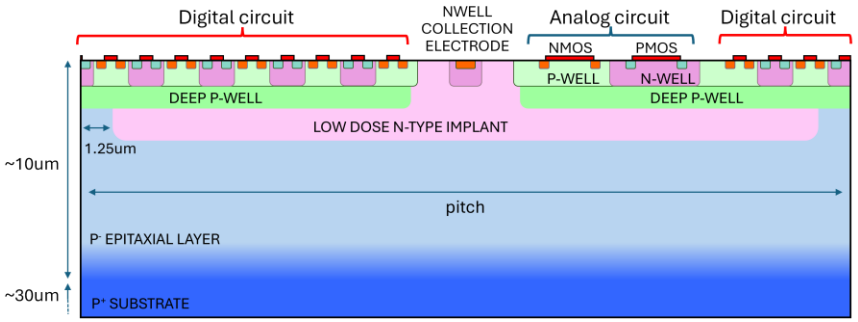
- Groups of 4 pixels
- As soon as a pixel is hit, its address is shipped through a global data line to the column encoders (asynchronous, the aim is to preserve timing information)
- The column encoders append the column address, and the data are shipped out through a CML driver

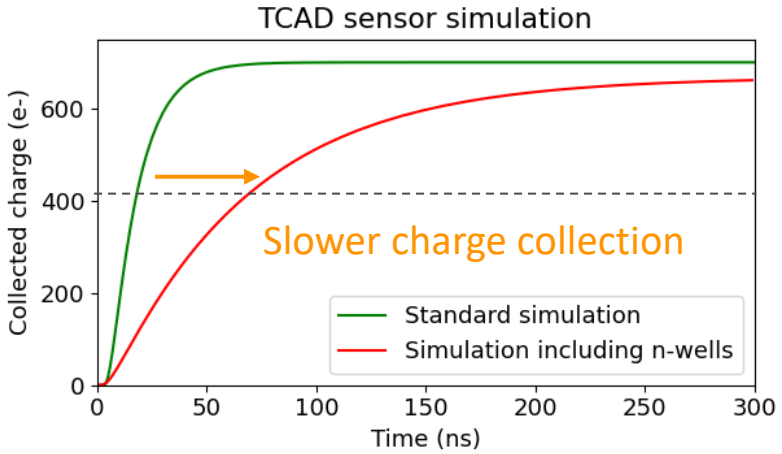


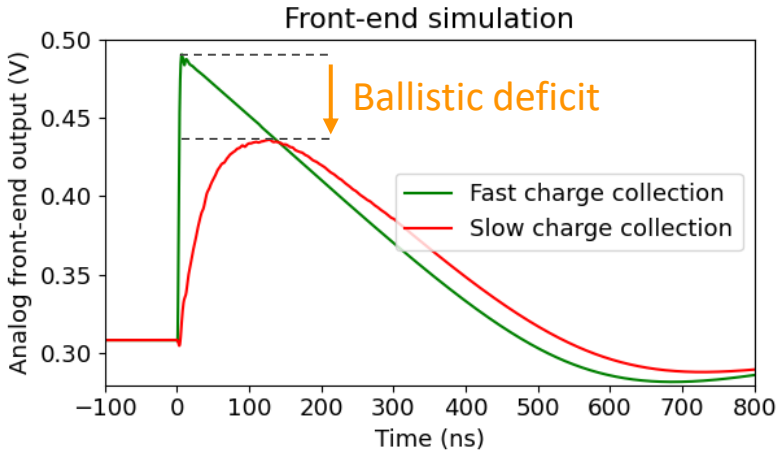
SID: Stitched Unit address, **MID**: Matrix ID, **UID**: Unit ID, **PID**: Pixel ID, **CID**, Column ID

The asynchronous readout of MOST allows to study to what degree the timing is preserved in the long-distance transmission

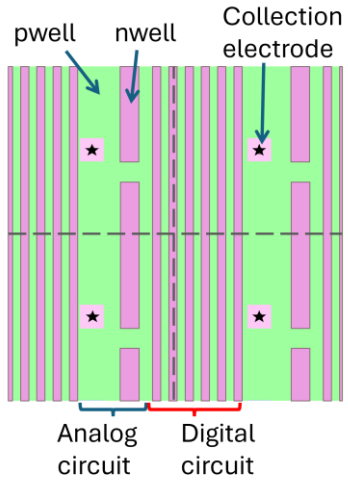
H2M - Non-uniform in-pixel response

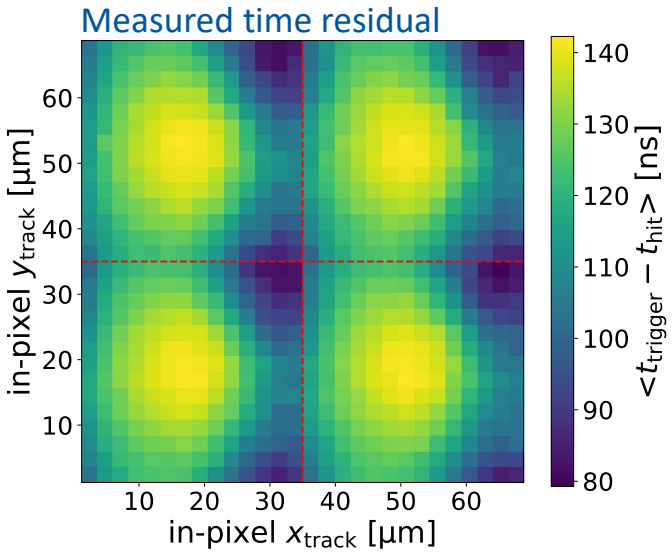


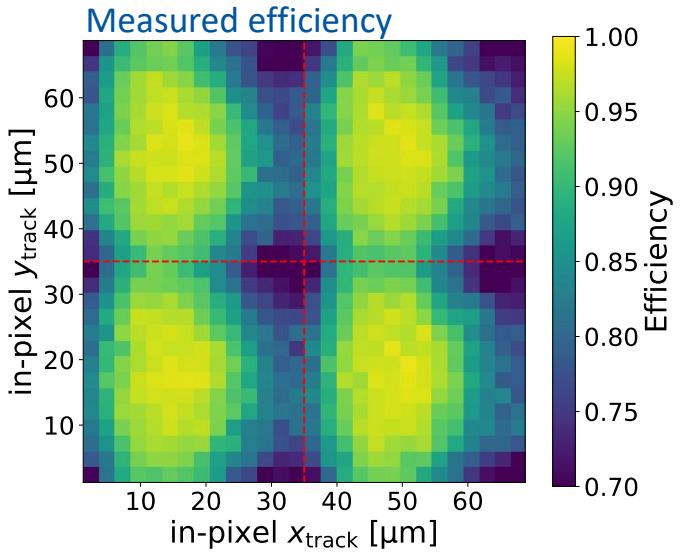




- Related to the size and location of the n-wells of the circuitry, leading to localized low-field regions with slower charge collection
- Mitigated with optimized operating parameters (bias, threshold, …)
- Confirmed in simulation

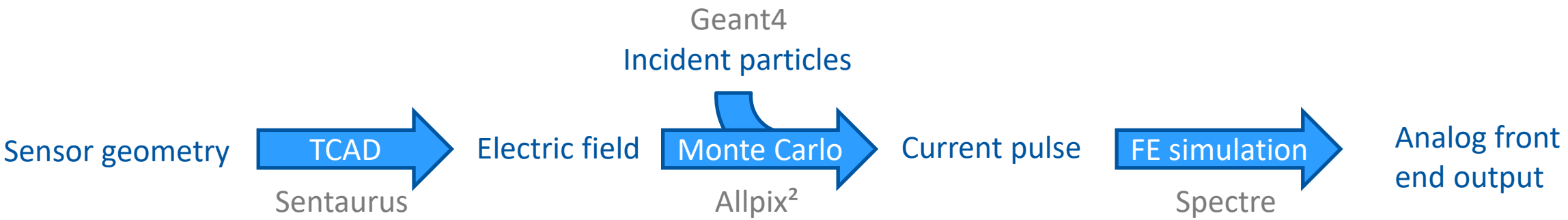




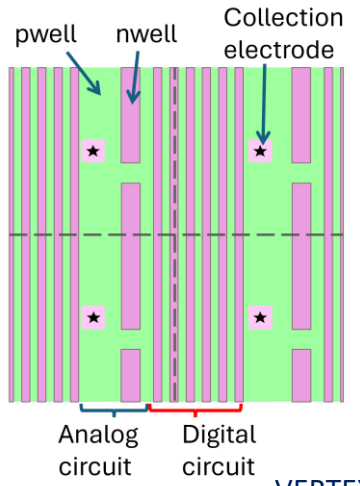


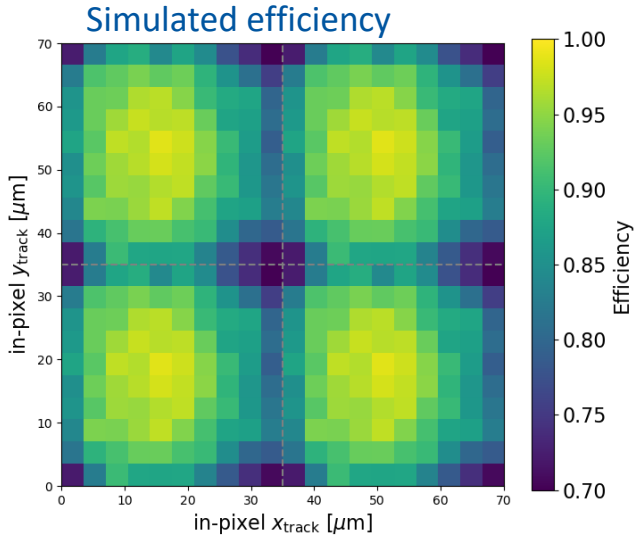
[8] C. Lemoine et al. “Impact of the circuit layout on the charge collection in a monolithic pixel sensor”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024), https://arxiv.org/abs/2503.21853

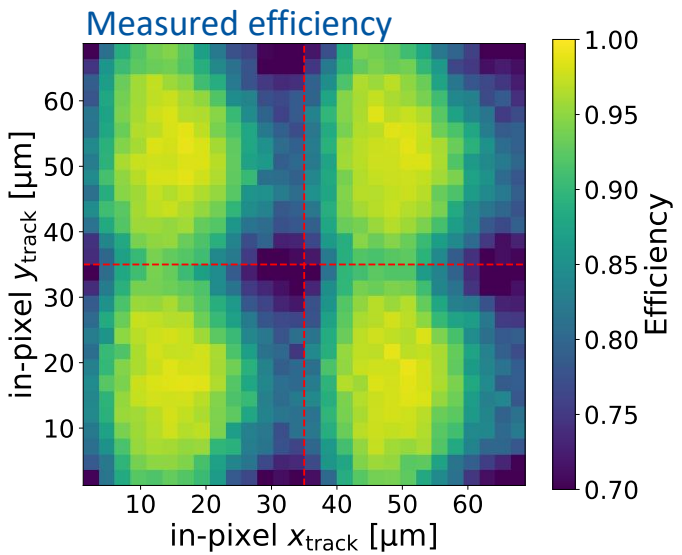
H2M - Simulation



- Simulation exploited to **understand and reproduce** the non uniform pixel response.
- Qualitative matching with measurements.
- Enable **simulation at design stage**, potentially avoiding future issues



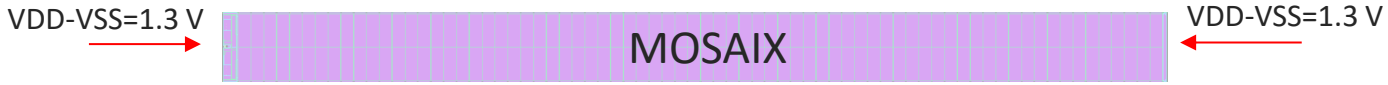




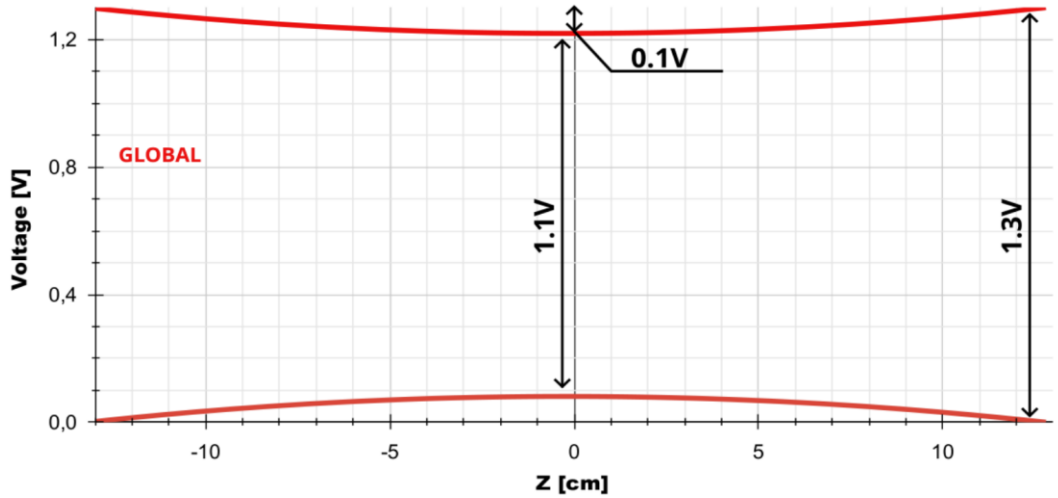
MOSAIX: on-chip power distribution

Power is supplied only from the short edges of MOSAIX in ITS3, and an acceptable on-chip supply voltage drop could not be achieved with the metals used for MLR1 and ER1 runs.

A custom metal stack has been provided by the foundry, including an additional thick metal layer and the replacement of two metal layers with thicker ones.



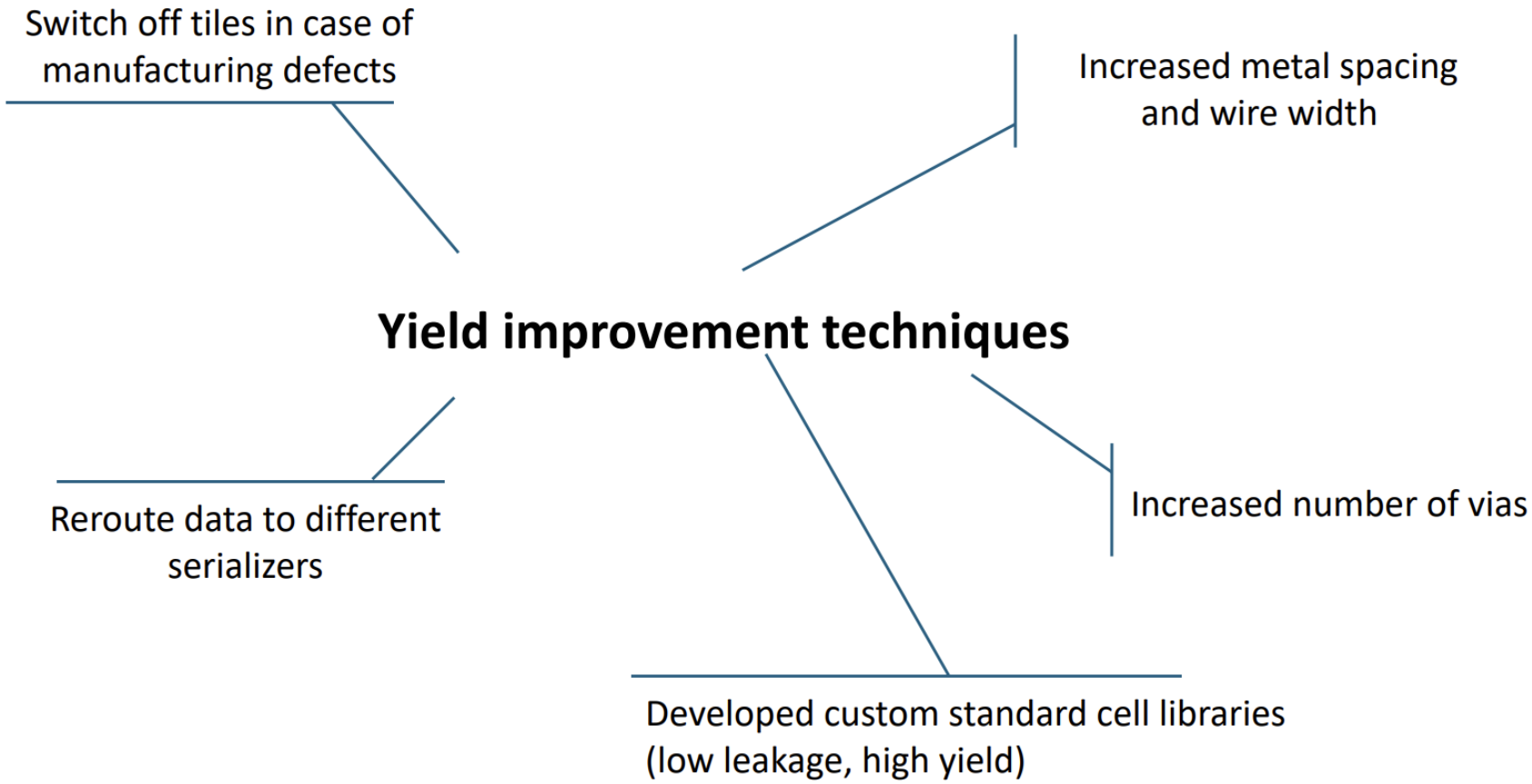
Simulated worst-case supply voltage drops with new metal stack, real power grid of MOSAIX [7]



[11] S. Bugiel. “Power distribution over the wafer-scale monolithic pixel detector - MOSAIX for ALICE ITS3”. In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).

MOSAIX: design for yield

Techniques have been extensively used to achieve high manufacturing yield and deal with defects.



[9] P. Vicente Leitao. “Development of the MOSAIX chip for the ALICE ITS3 upgrade”. In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).
[11] S. Bugiel. “Power distribution over the wafer-scale monolithic pixel detector - MOSAIX for ALICE ITS3”. In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).