# Front-End Chip R&D for HL-LHC era Pixel detectors - latest results and lessons learned

Vertex 2025 - Knoxville, 26.08.25

VERTEX25

Timon Heim - LBNL

# What drives Front-End Chip design?

BERKELEY LAB

**Performance**
(More pixels, smaller pixels, faster readout …)

**Low Mass**
(Lower Power, thinner cables, less passives, …)

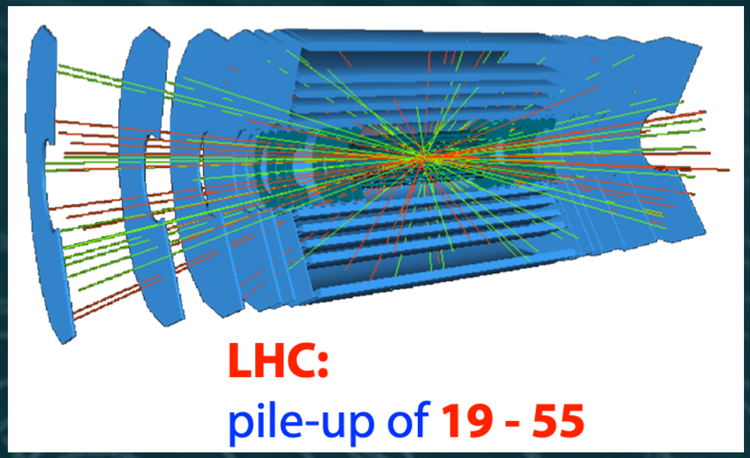
Design Specs

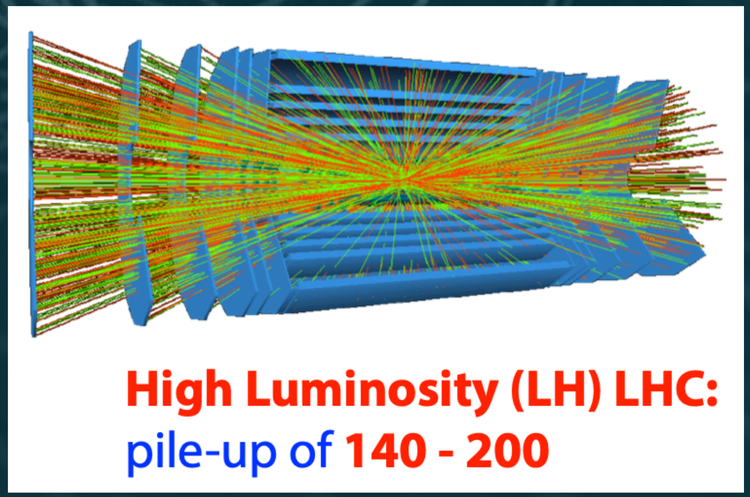
**Radiation Tolerance**
(Higher radiation tolerance, SEE tolerance, higher temperature operation, …)

Need to balance multiple opposing specification drivers!

# HL-LHC Requirements

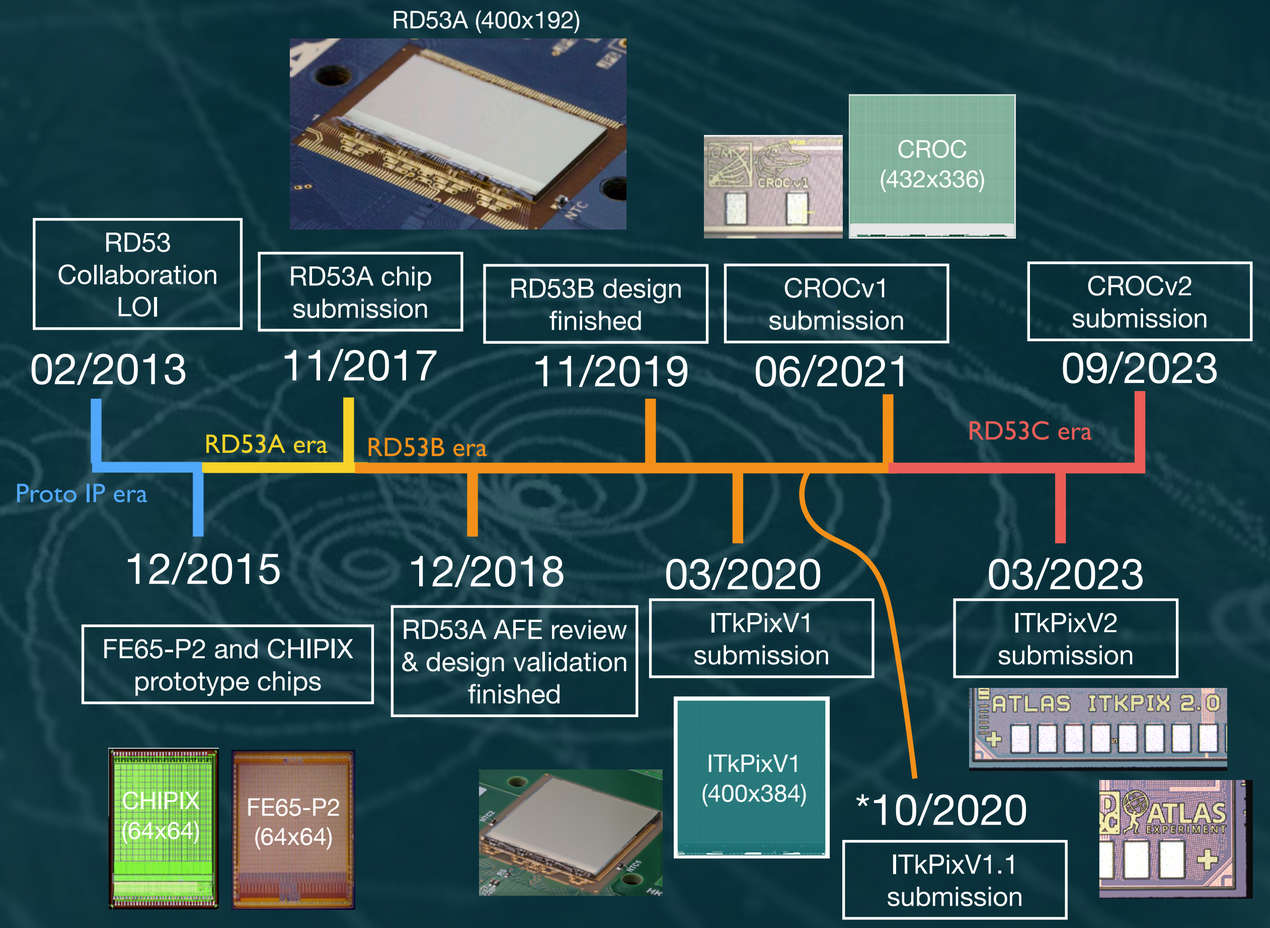
- From the detector R&D point of view:
  - More collisions -> 5x more particles & radiation damage
    - Higher occupancy demands higher granularity
  - Want more data -> 5x higher trigger rate
  - Increase acceptance -> tracking coverage up to $\eta < 4$
  - Maintain or improve on tracking performance from Run 1/2/3



# RD53 Timeline

- Prototype era:
  - Test IPs in independent MPW ASIC submissions
  - Small scale Pixel prototype chips
- RD53A era:
  - Half-size demonstrator chip
  - Realistic biasing and power distribution of full size chip
  - Tests 3 different analog front-ends
- RD53B era:
  - ATLAS/CMS full-size pre-production chip
  - All production chip features, but lacking some SEE hardening
- RD53C era:
  - ATLAS/CMS full-size production chip
  - Heavily improved verification procedures



# ITkPix in a Nutshell

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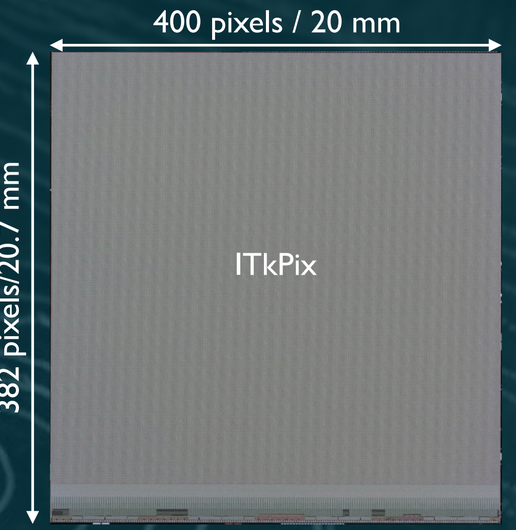
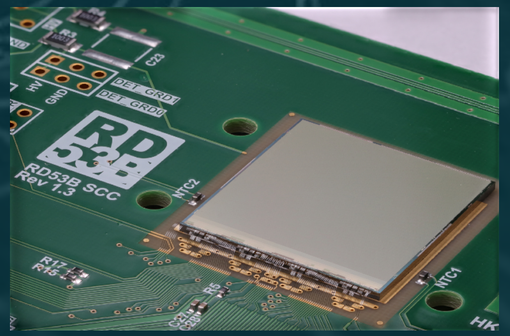
- Performance:
  - Main design specs derived from ATLAS/CMS innermost layer particle fluence 3GHz/cm2
  - Need to achieve main performance specs while not exceeding 1W/cm2 power
- Radiation tolerance:
  - 65nm technology inherent radiation hardness does a lot of the heavy lifting
  - Nevertheless had to do a lot of tweaking in design to achieve desired TID and SEE tolerance
- Low mass:
  - Major mass contributions from power and data services
    - Novel serial powering made power service's contribution nearly negligible
    - In ATLAS data services could not be reduces (no on-detector optical conversion due to radiation damage)

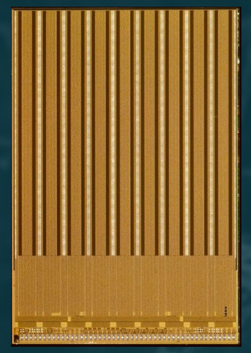
| Parameter | Value |
|---|---|
| Technology | 65nm |
| Max. hit rate | 3 GHz/cm2 |
| Trigger Rate | 1MHz |
| Trigger Latency | 12.5us |
| Pixel size (chip) | 50um x 50um |
| Pixel array | 400x384 |
| Chip dimension | 20mm x 21mm |
| Detector Capacitance | <100fF |
| Detector Leakage | <10nA |
| Min. threshold | <1000e |
| Radiation Tolerance | 1Grad @ -10C |
| SEE Tolerance | <100Hz/chip |
| Power | <1W/cm2 |
| Readout data rate | 1-4 links @ 1.28Gbps |
| Temp. Range | -40C to +40C |



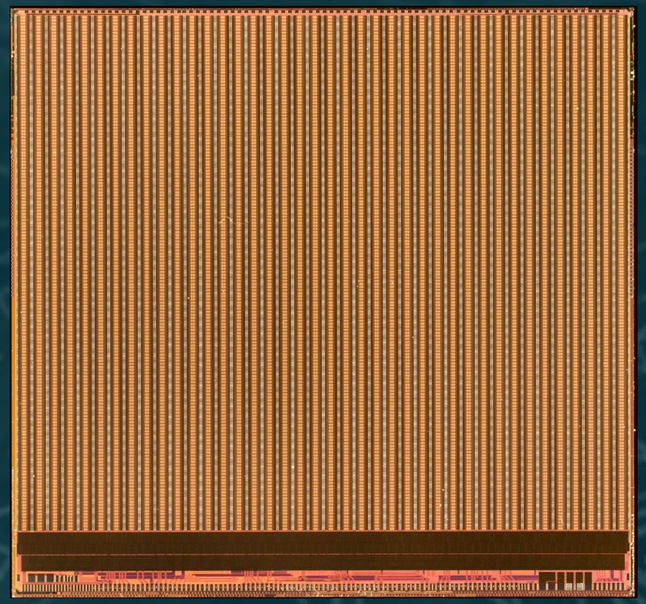



# A brief ATLAS Pixel History

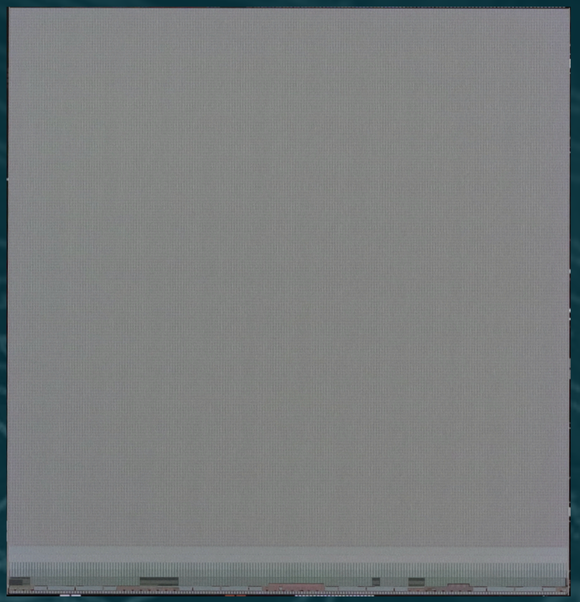
FE-I3 (2003)



FE-I4 (2011)



ITkPix (RD53) (2023)



FE-I3:
- 250nm CMOS (7.6 mm x 10.8 mm)
- 2,880 pixel (400 um x 50 um)
- 3.5 M Transistors
- 100 MRad TID tolerance
- 200 MHz/cm2 hit rate
- 40 uW per pixel
- 40 Mbps data output

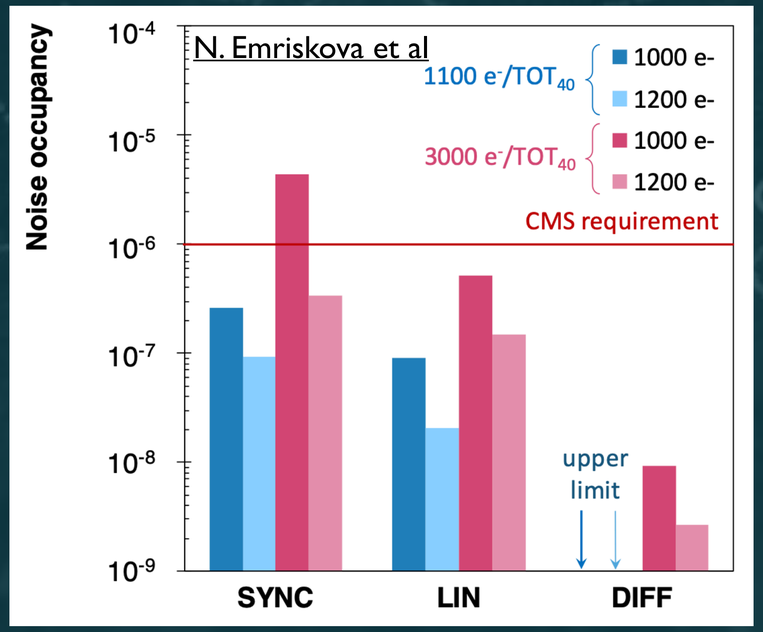
FE-I4:
- 130nm CMOS (20 mm x 20 mm)
- 26,880 pixel (250 um x 50 um)
- 80 M Transistors
- 250 MRad TID tolerance
- 400 MHz/cm2 hit rate
- 15 uW per pixel
- 160 Mbps data output

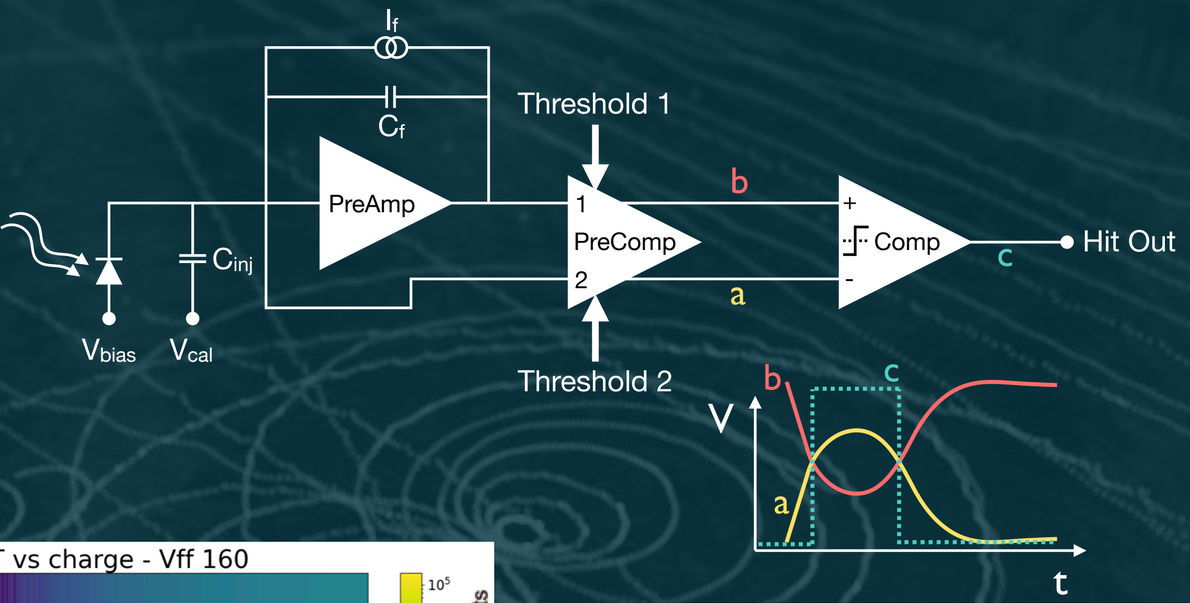
ITkPix:
- 65nm CMOS (20 mm x 21 mm)
- 153,600 pixel (50 um x 50 um)
- 1000 M Transistors
- 1 GRad TID tolerance
- 3 GHz/cm2 hit rate
- 12 uW per pixel
- 5.12 Gbps data output

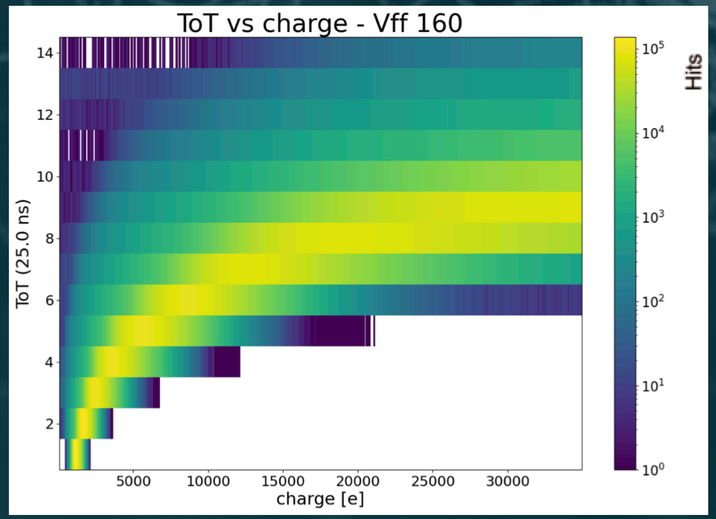
# Analog Front-End

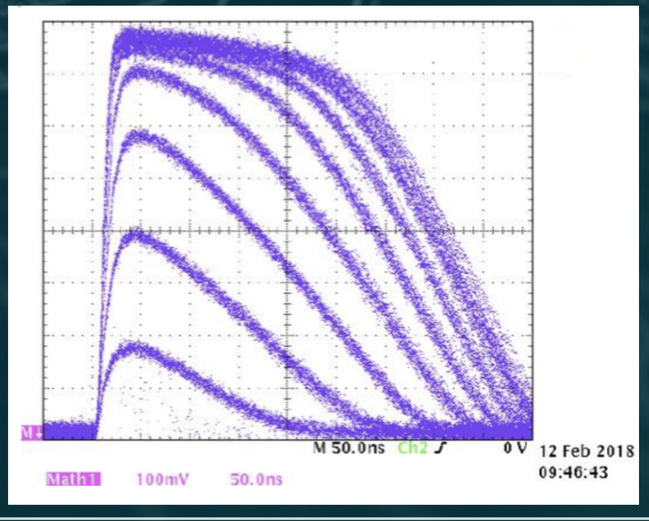
## Differential Analog Front-End:

- Optimized for low-power & low-noise operation
- Tested alongside Linear and Synchronous Front-End during RD53A era
- Non-traditional and somewhat complex, raised concerns with radiation hardness
- Highly non-linear response
- ATLAS chose differential and CMS chose linear front-end for production chip

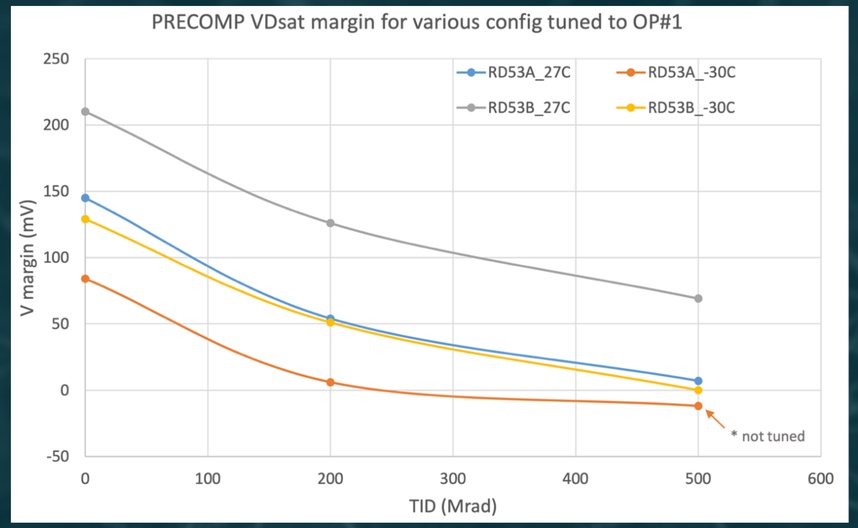


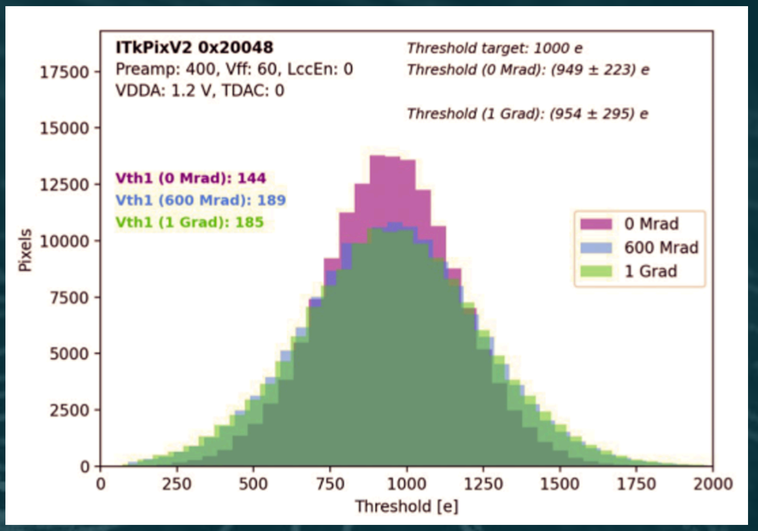



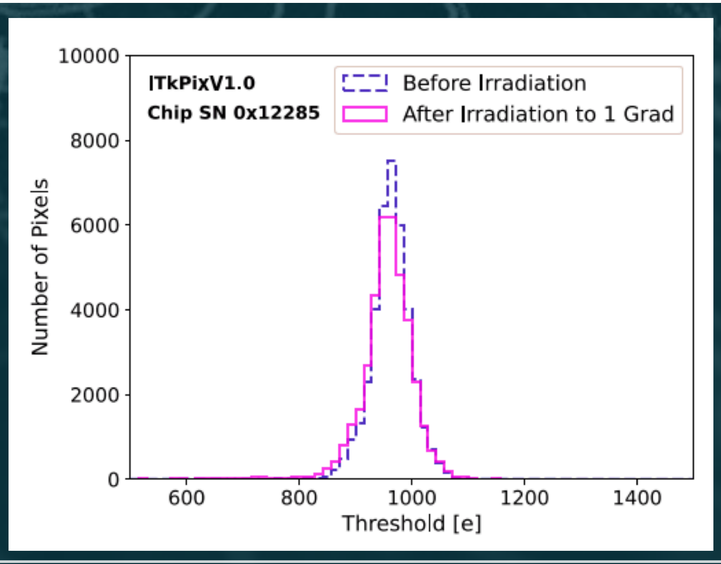



# Differential Front-End Radiation Tolerance



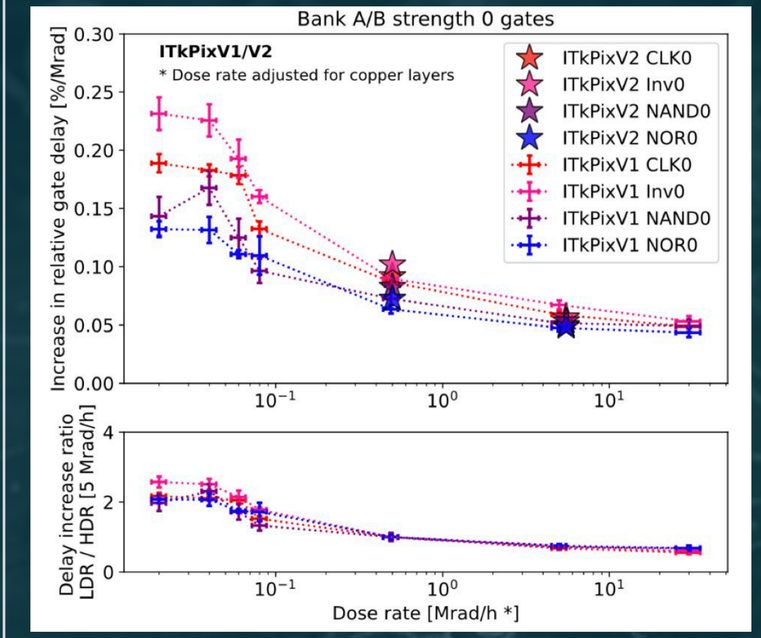



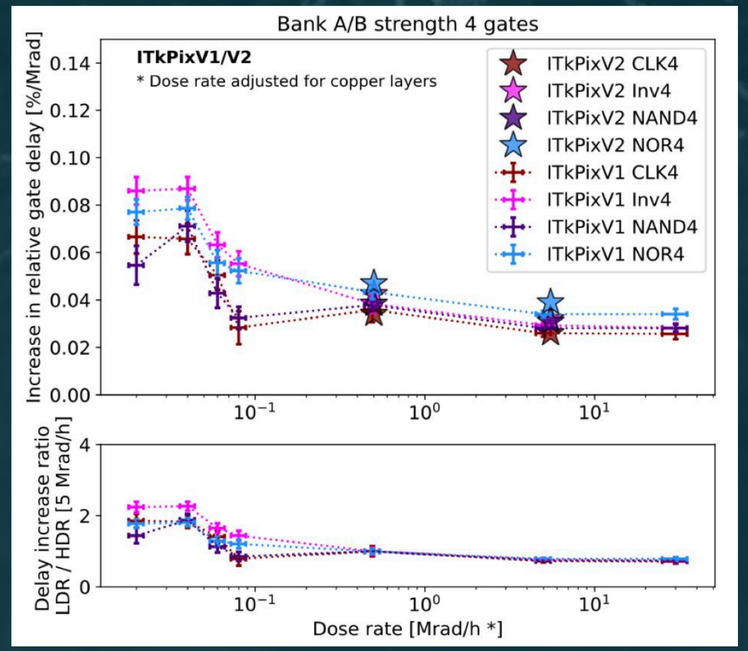



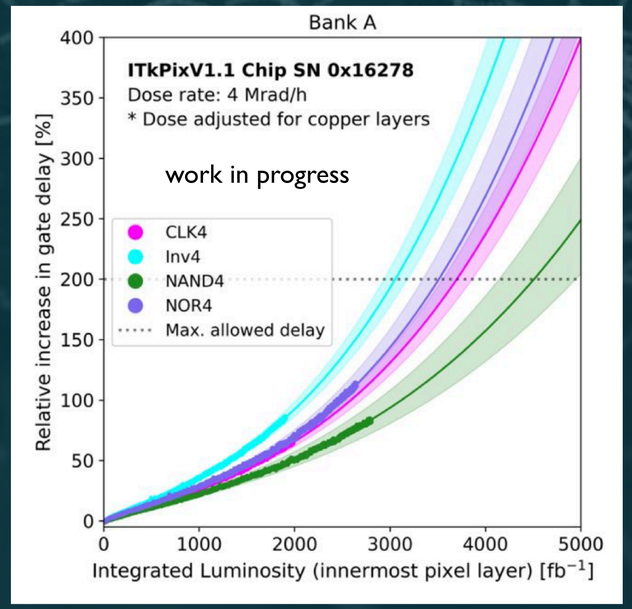

- Differential FE performance measurements in RD53A complicated by FE output erroneously not being buffered close to FE and comparator output being loaded with varying and large parasitic capacitance
- Hidden under this issue discovered problem with pre-comparator voltage margin when operating cold and irradiated
- Where confident in how to fix the issue as behavior was well reproduced in simulation, never the less ATLAS took some risk choosing the front-end for their pre-production chip
- Lesson learned: IMO focus on one design choice and more chances for design iteration are better than large variety of options

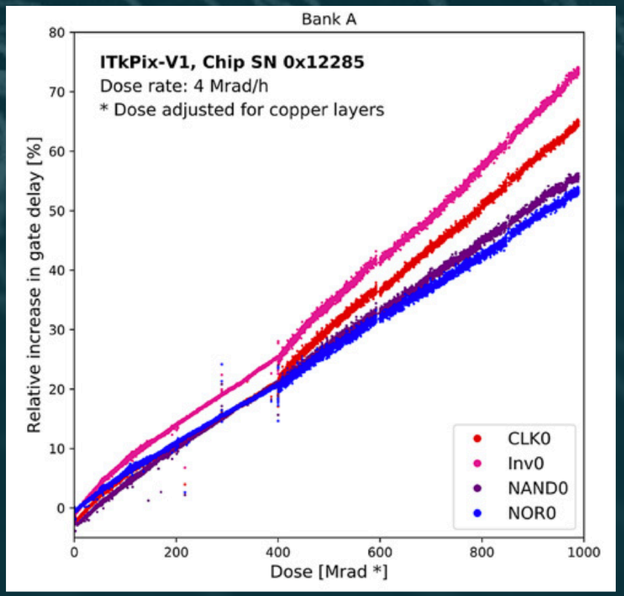
# Digital Radiation Tolerance

- On-chip ring oscillators are critical tool to evaluate radiation hardness of digital circuitry
- Strength (~size) 4 gates used in pixel matrix to balance circuit density with radiation tolerance
- Have to consider low dose rate damage amplification
- Extrapolation from high dose rate irradiations indicates sufficient tolerance (>1Grad)
- Perhaps even rad hard enough for 2.5a$^{-1}$b?



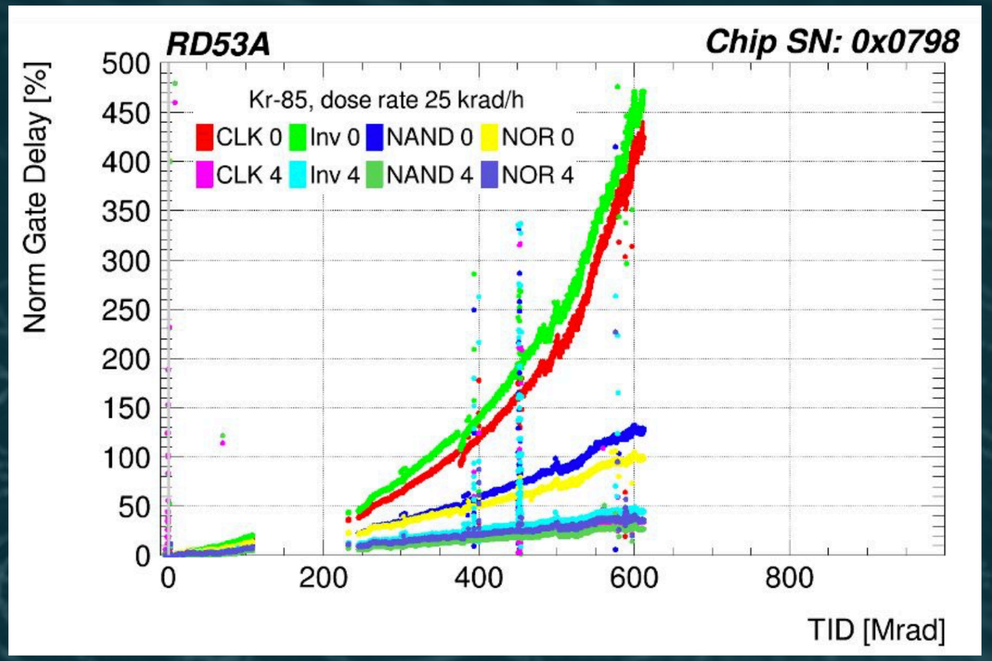



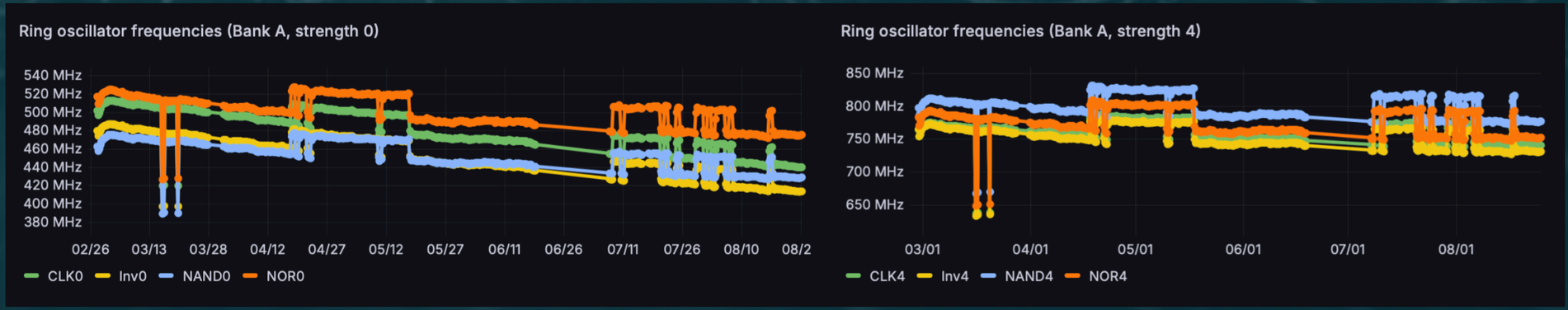



# Low Dose Rate Irradiations

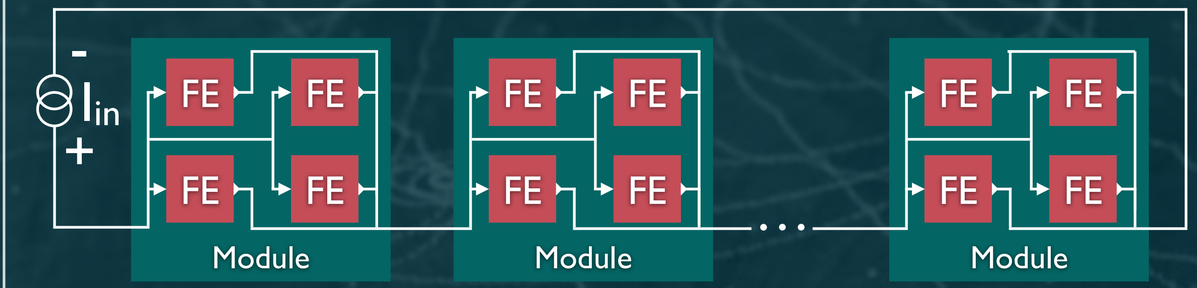
- Have to extrapolate high-dose rate results to low-dose rate damage based on , typically based on short term O(10Mrad) low dose rate irradiations
- Cannot predict non-linear evolution of damage -> Need long-term low dose rate irradiations to do so -> ~5 years of continuous irradiation
- Need active cooling to -10C and active readout to keep transistors switching -> non-trivial high reliability setup needed
- Established low dose rate irradiation system at LBNL (SLIPPER) using Kr85 source
- RD53A (using Strength 0 gates) started failing around 600Mrad (after 3 years of operation) matching expectation from simulation of gate delay
- Finally started SlipperV2 with ITkPixV2 in beginning of 2025



# Powering Options

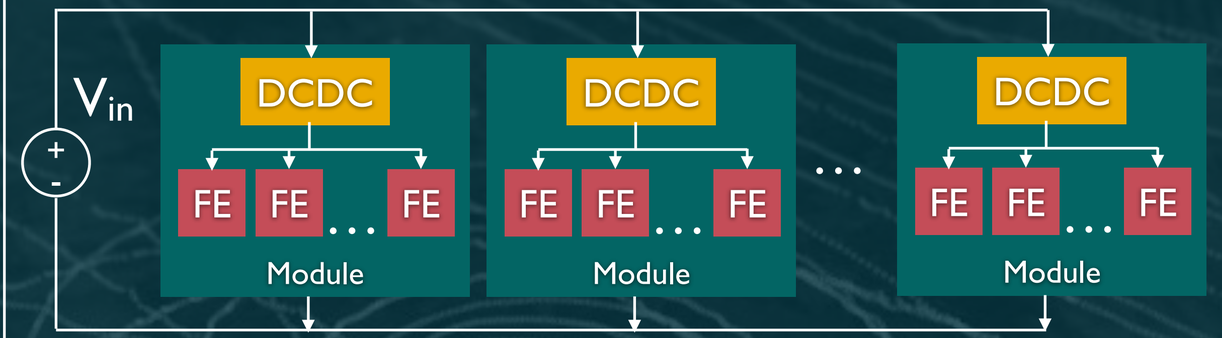
## Serial Powering




Pro:
- Compact on-chip regulator design
- Robust against most common failures
- Redundancy against most severe failure
- Efficiency improves the longer the SP chain
- “Simple”
- Inherently radiation hard
- Proven to be exceptionally robust against noise

Con:
- System behavior defined during design → Need excellent knowledge of FE under operational conditions
- Regulator optimization coupled with FE chip design
- Realistic* testing requires full SP chain (N Modules)

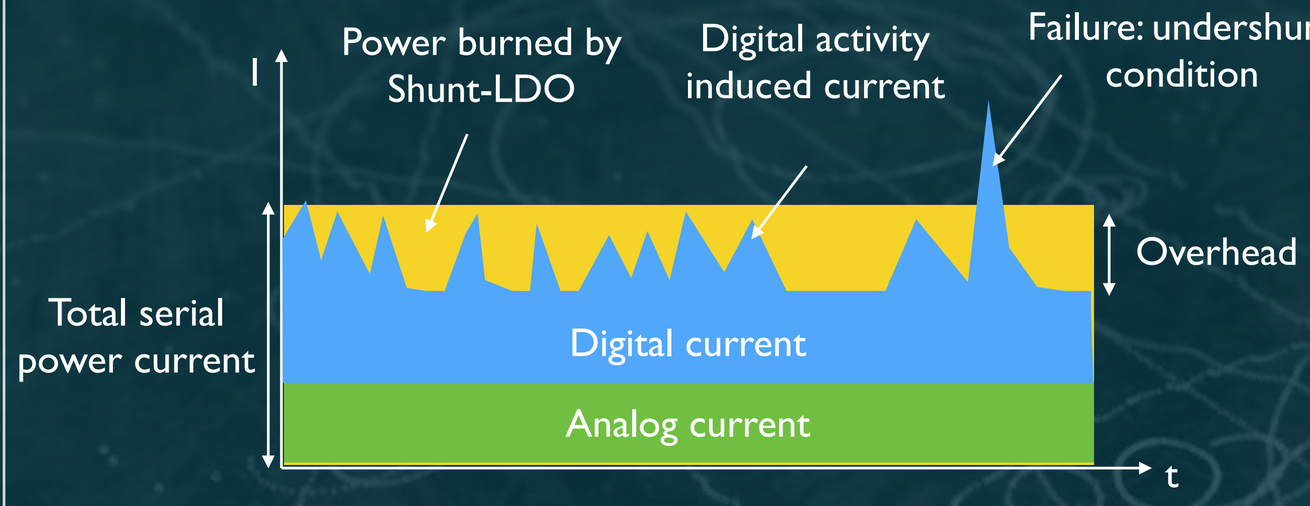
## DCDC Conversion

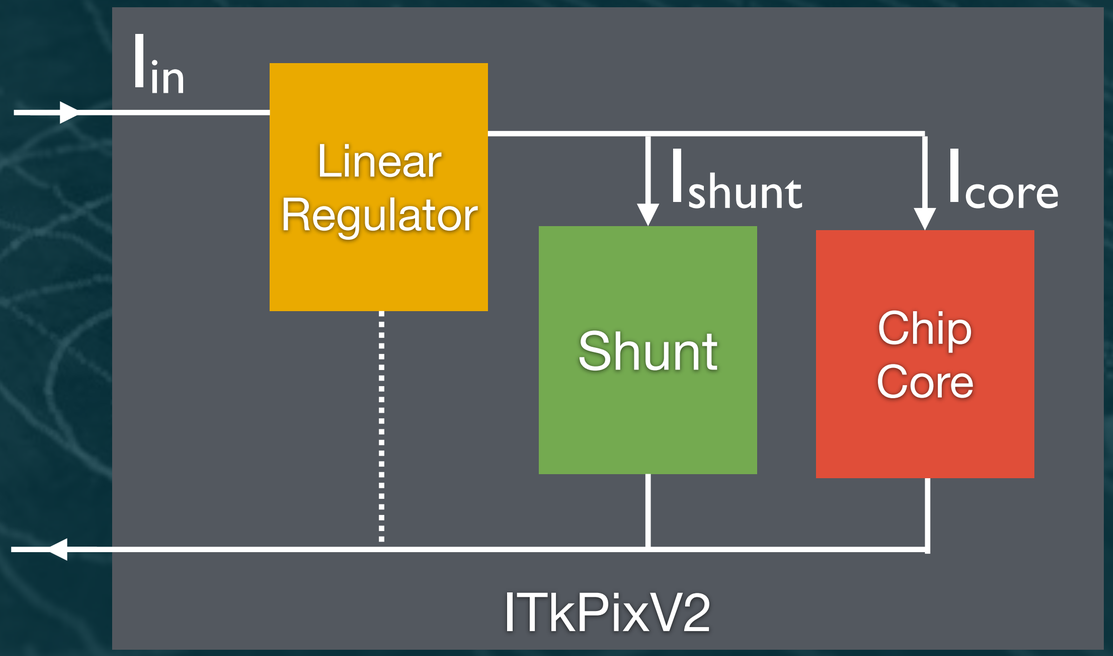



Pro:
- Well understood and widely used regulator design
- Efficiency independent of no. of modules
- Can be optimized independently of other components (or even developed independently e.g. CERN bPOL12V)

Con:
- DCDC converter cannot be manufactured in FE chip technology (high voltage switches)
- EMI from switch mode converter can induce noise in detector
- Requires bulky inductor
- Shielding increases mass
- Single point of failure

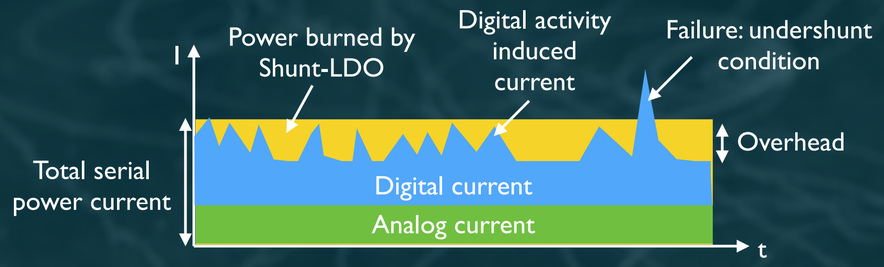
# Serial Power Regulator in a Nut-shell



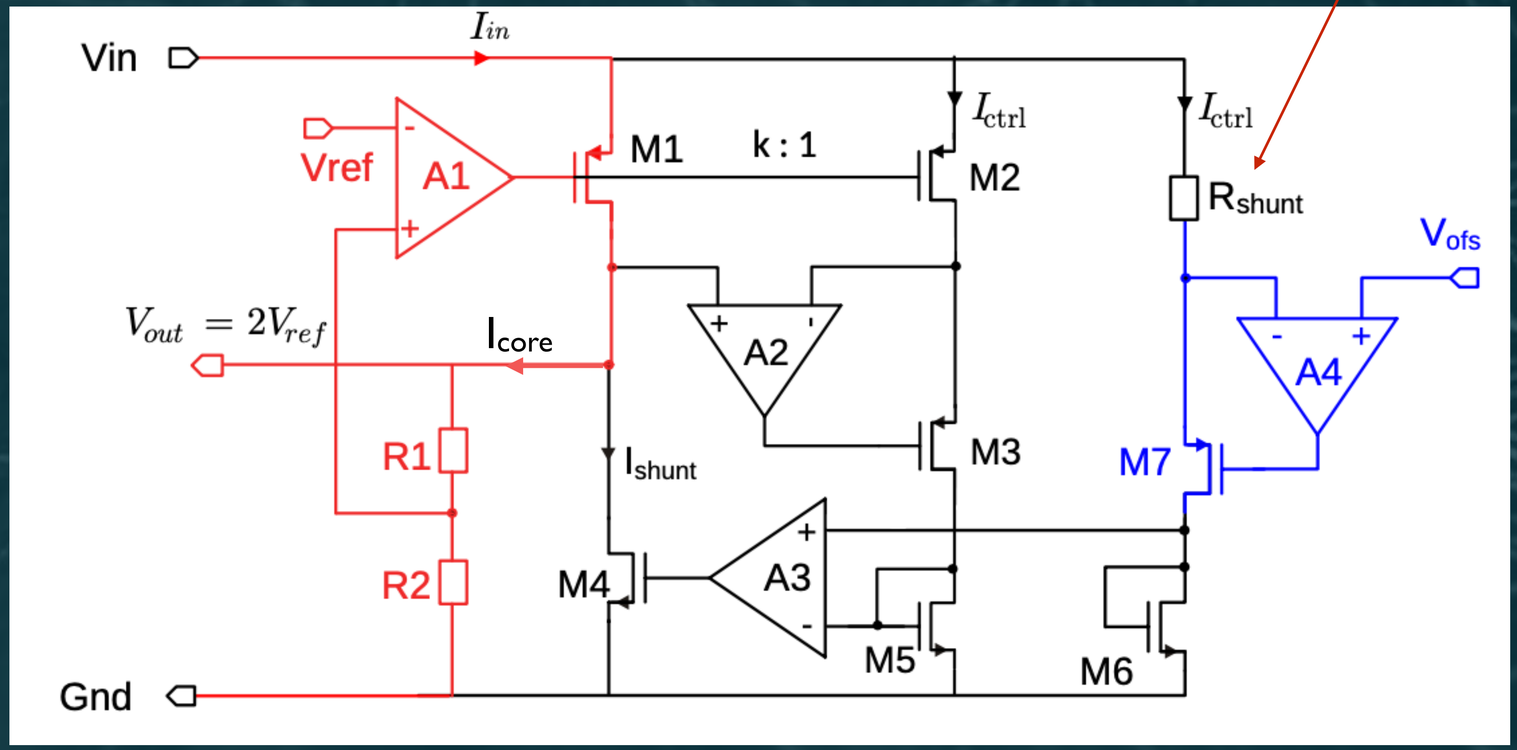



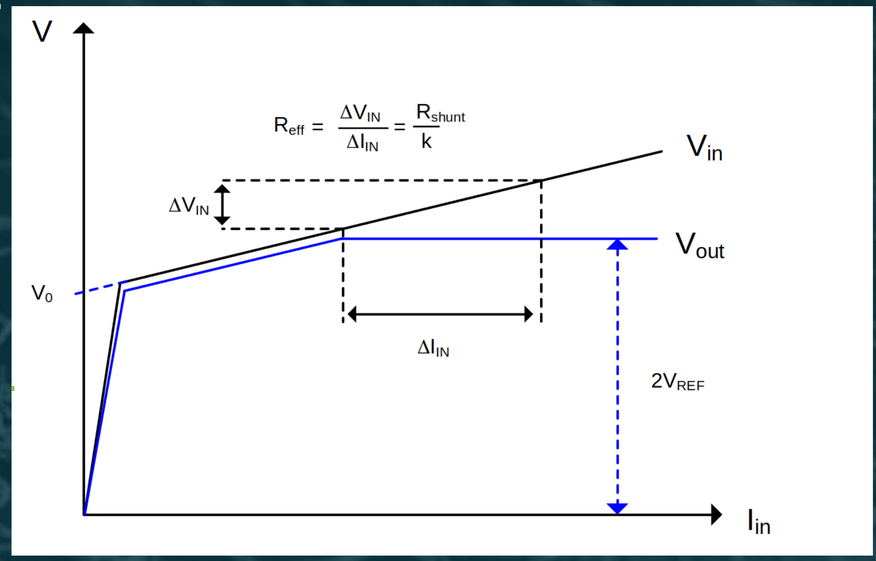

- Serial powering requires choice of constant current supplied through chain
- Current needs to satisfy chip core under any circumstances, otherwise loose regulation of Vin (undershunt) and likely proper operation of chip
- Shunt will burn off difference between $I_{in}$ and $I_{core}$

# Powering




Off-chip Resistor




k ≈ 1000

$$V_{in} = V_{ofs} + I_{in} * R_{shunt} / k$$

$$I_{in} = I_{core} + I_{shunt} = k * I_{ctrl}$$

$$I_{ctrl} = (V_{in}-V_{ofs}) / R_{shunt}$$

$$1.4V < Vin < 1.8V$$

(even if one chip in modules fails open)

# In Numbers

BERKELEY LAB

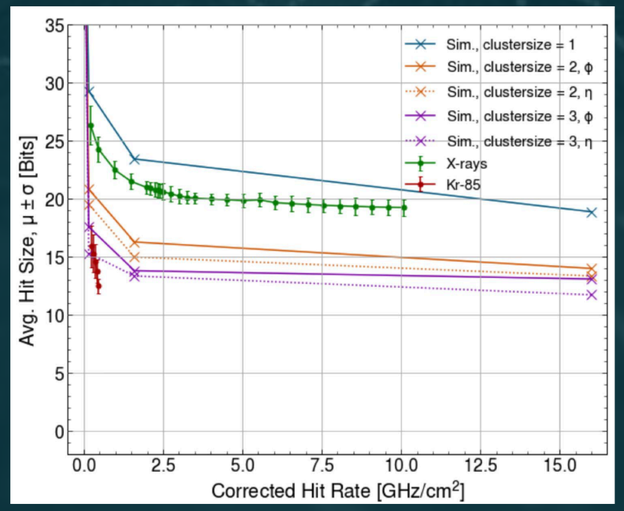
| Layer 2 - 4 Settings | | | | |
|---|---|---|---|---|
| | Analog | Digital | Total Chip | Total Module |
| Analog Periphery [A] | 0.120 | | | |
| Analog Matrix [A] | 0.440 | | | |
| Digital Periphery [A] | | 0.250 | | |
| Digital Periphery Activity [A] | | 0.010 | | |
| Digital Matrix [A] | | 0.450 | | |
| Digital Matrix Activity [A] | | 0.040 | | |
| Icore[A] | 0.560 | 0.750 | | |
| $I_{core}$+ overhead (10%/20%) [A] | 0.616 | 0.900 | | |
| $I_{shunt}$ | 0.056 | 0.150 | | |
| $I_{in}$ current per chip [A] | | | 1.516 | 6.064 |
| Total Power [W/cm2] | | | | 0.541 |
| k | 1000 | 1000 | | |
| Offset [V] | | | 1.000 | |
| Target $V_{in}$ [V] | | | 1.500 | |
| $R_{ext}$ [Ohm] | 812 | 556 | | |
| $R_{eff}$ [Ohm] | | | 330 | 82 |

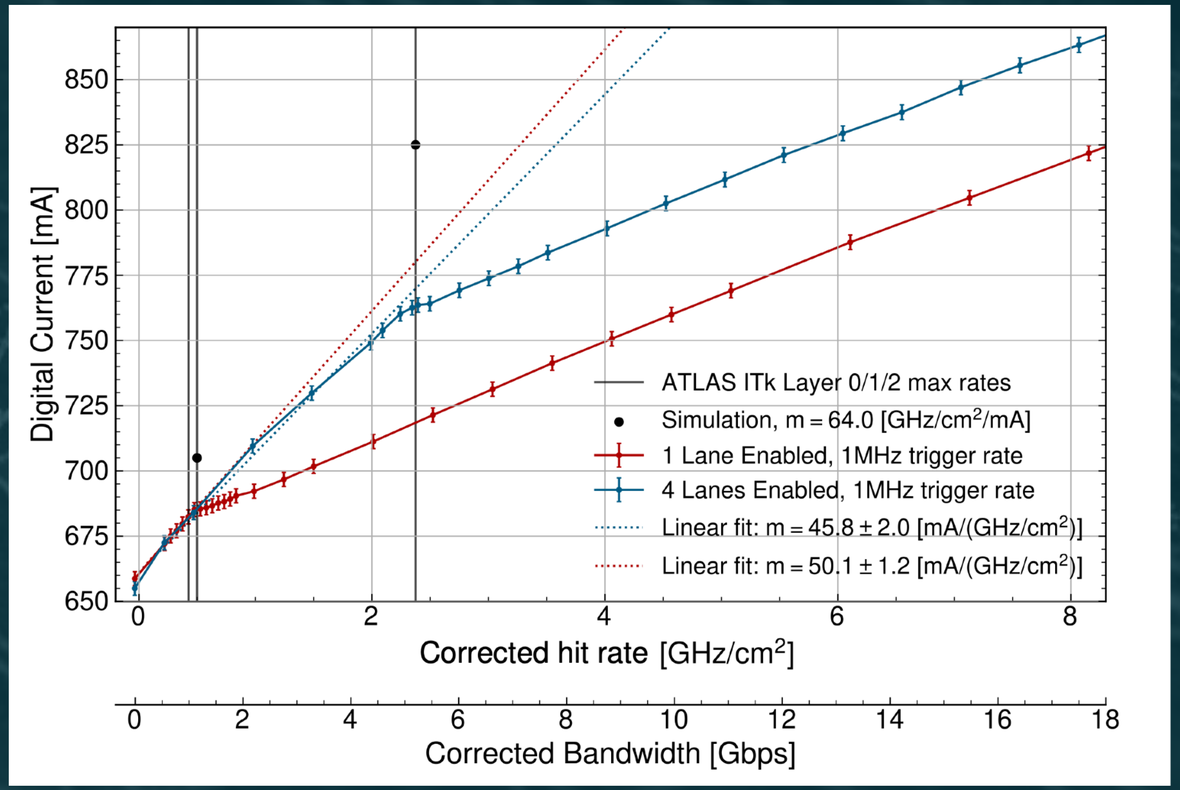
$$R_{shunt} = (V_{in}-V_{ofs}) / I_{ctrl}$$
$$= (V_{in}-V_{ofs}) / (I_{in} / k)$$
$$V_{in} = V_{ofs} + (R_{eff} * I_{in})$$

Impedance of chip/module will be equal to $R_{eff}$ unless $I_{shunt}$ goes to 0A!

# Activity Induced Current Measurement

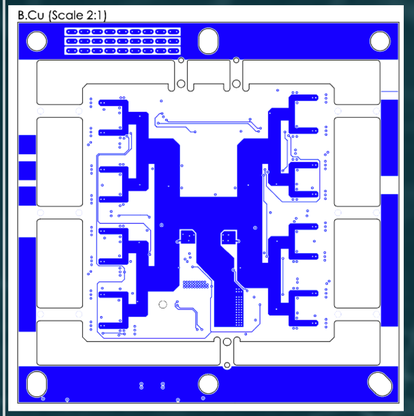
- Final measurement only possible very late in design pipeline, because it requires a hybridized detector module with the final chip version (ITkPixV2)
- Additionally requires quite a bit of DAQ firmware/software work to enable readout at full occupancy and trigger rate
- For this used single chip module and Xray source (smaller cluster size = more bandwidth compared to HL-LHC)
- Ultimately measurement is slightly below simulation value 😅
- It would have been really useful (also for many other measurements like SEE testing) to have a circuit on chip that can generate a somewhat realistic hit load!

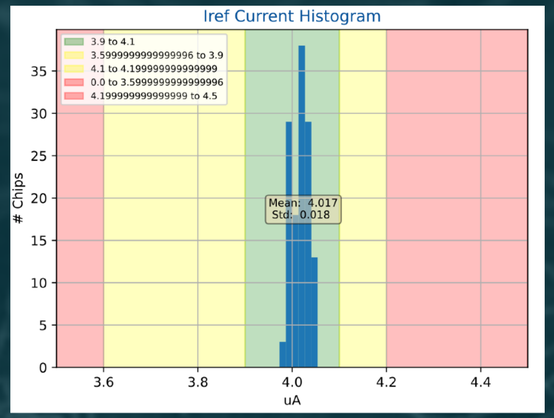


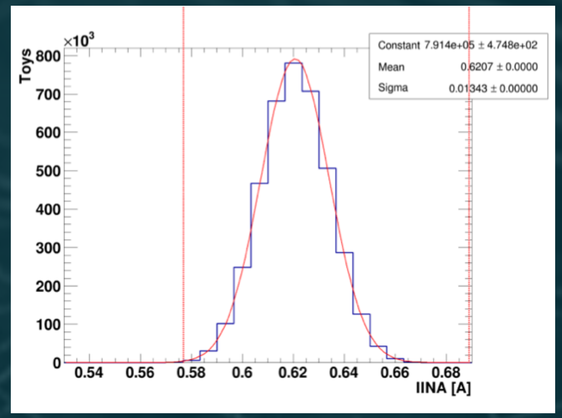



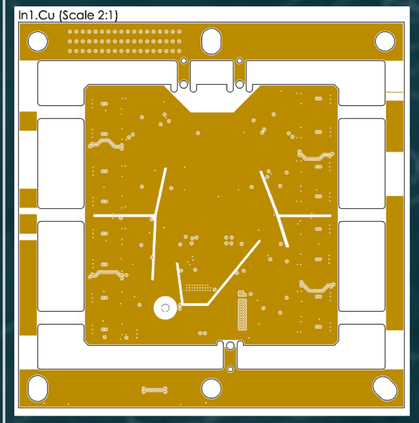
# The Culprit

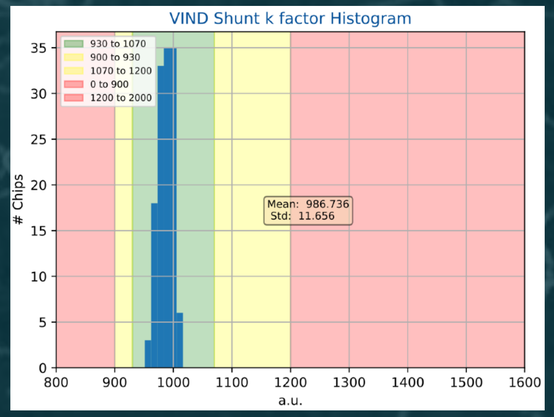
Module Flex design | Wafer probing data | Toy Sim created by Matthias Hamer

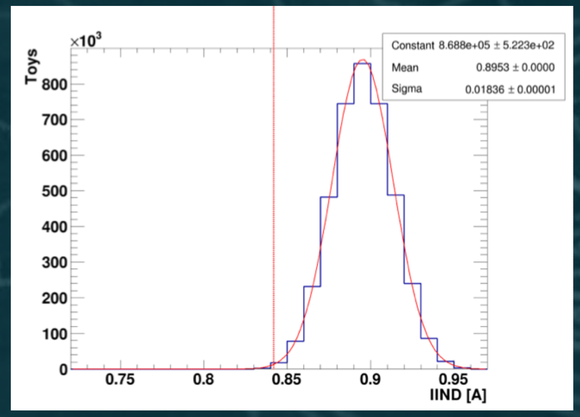


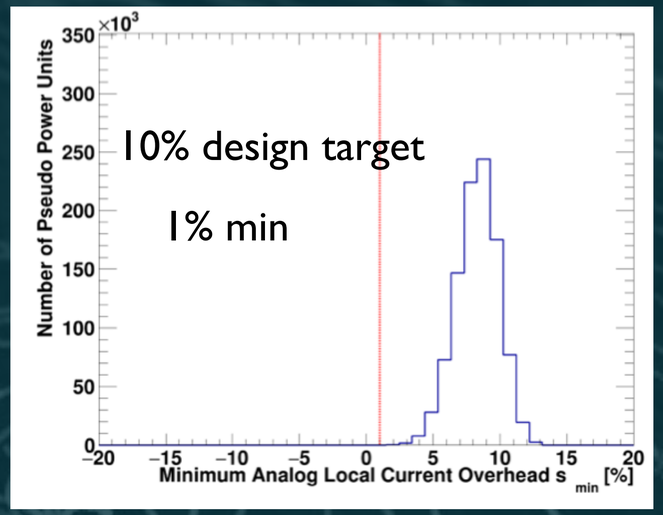



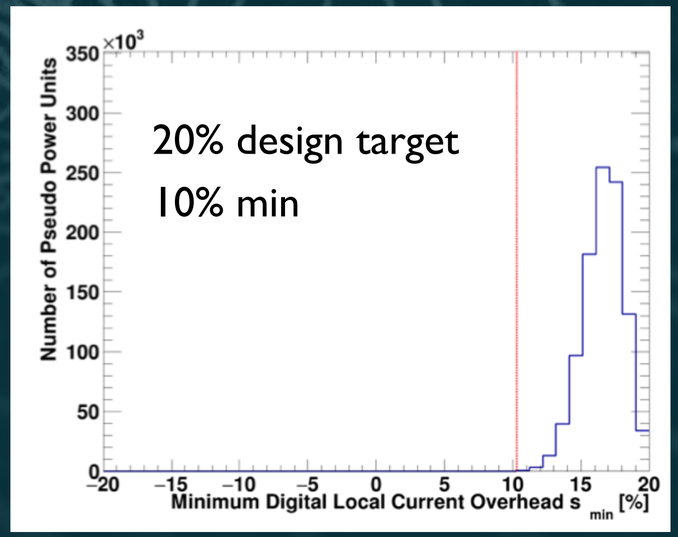



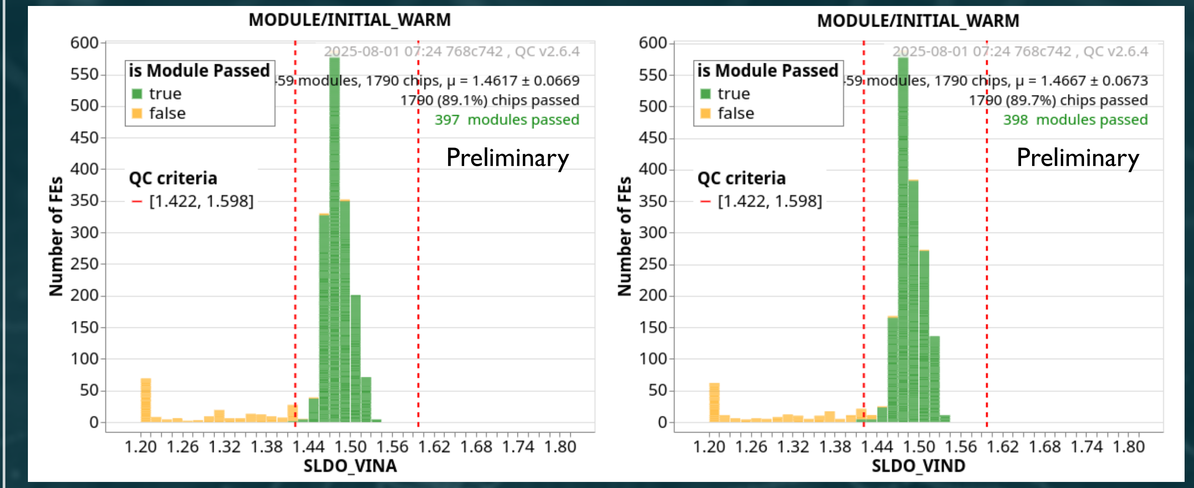



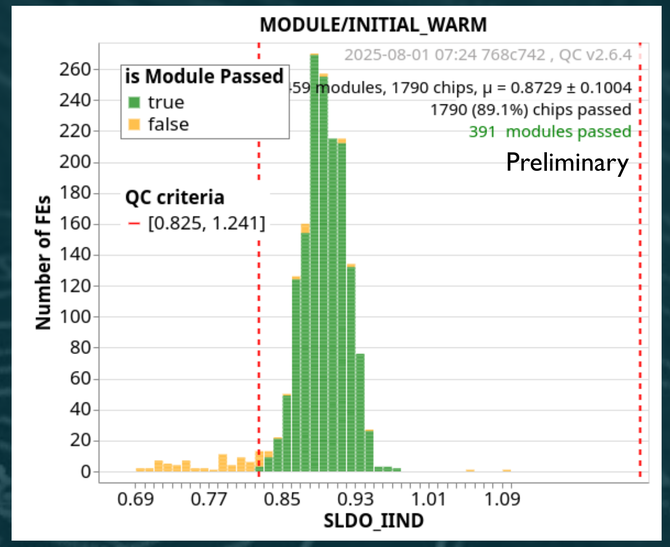



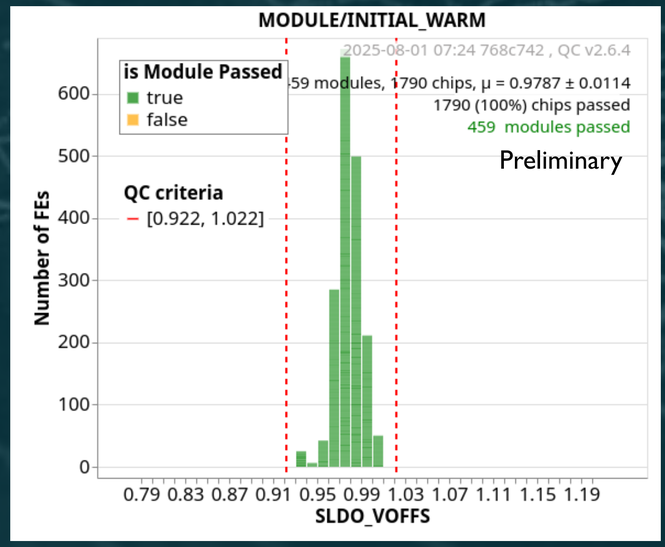

Toy Sim created by Matthias Hamer

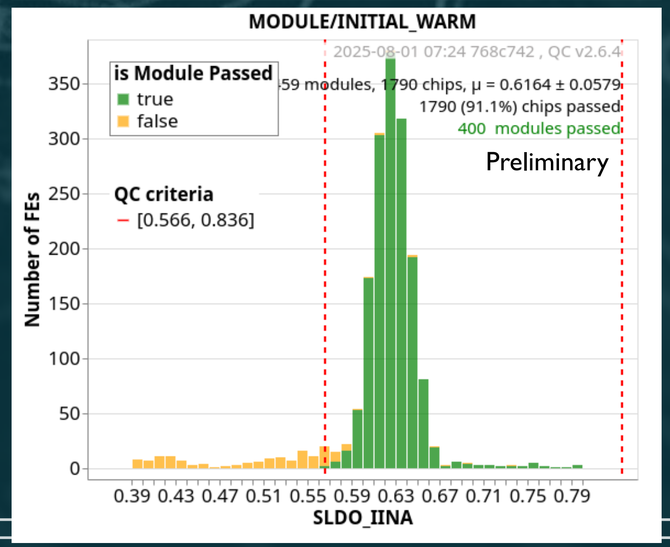
- Variations in k-factor, resistance, Vin, and Vofs will lead to change in impedance
  - k-factor measured and cut on during wafer probing
  - 0.1% tolerance resistors
  - $V_{ofs} = 2*(R_{ofs}*I_{ref})$ => $I_{ref}$ measured and cut on during wafer probing
- Variation in impedance will lead to unequal current splitting in module
  - Lower impedance chips will take away current from higher impedance chips
- Variation in $I_{core}$ will lead to reduced overhead

# How are we doing? (Preliminary)



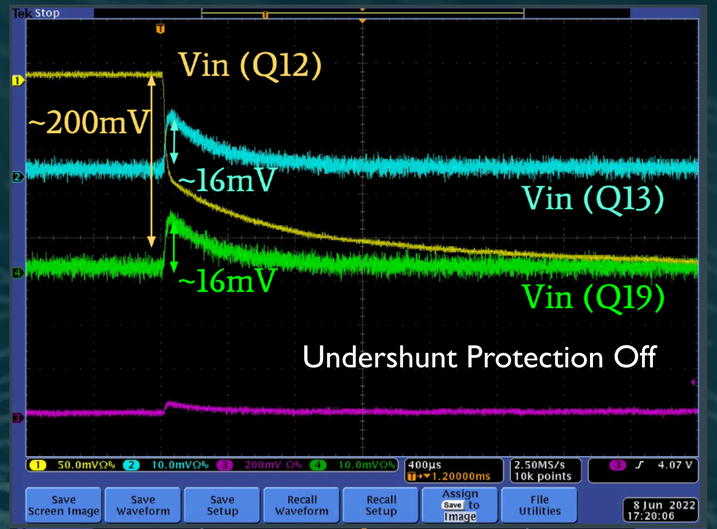



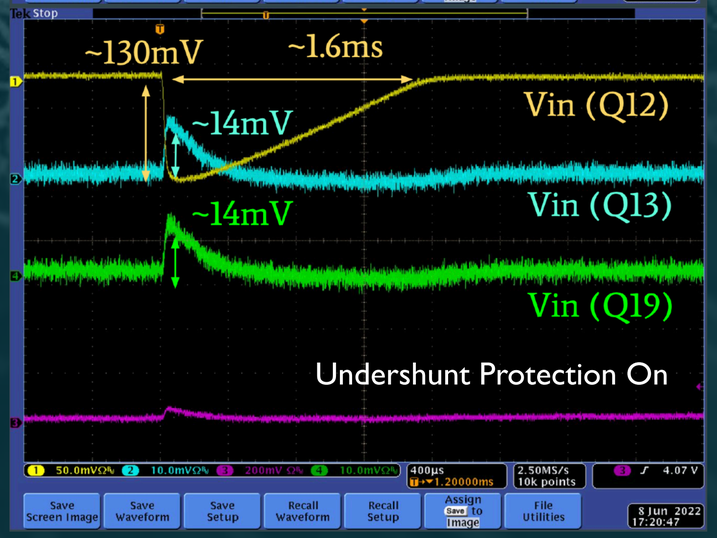



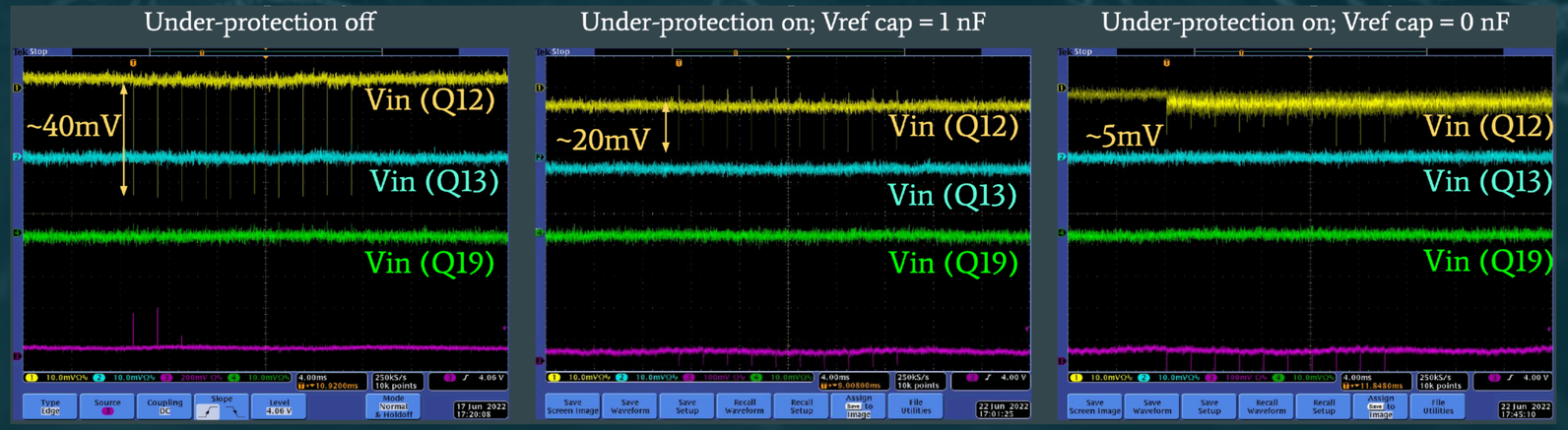

- Module production now on-going, can look at first results over large data set of SLDO tests
- SLDO circuit behavior highly reproducible
- Under tight ITk power budget we understood this SLDO test will likely be a yield driver
- Based on initial data increased current to modules by ~5% using up some safety margin from power budget to improve yield

# Undershunt Protection

- Wanted to further protect against undershunt condition in case of rare dynamic failure (e.g. extreme instantaneous hit rate)
  - Worried about voltage transient on other modules in chain
- Developed circuit that check for Ishunt <= 0 and if the case reduces Vref to the regulator, lowering VDDA/D until Ishunt > 0
- The problem: reaction speed
  - If circuit reacts fast -> could become unstable and oscillate (additionally leads to worse noise performance on Vref)
  - If circuit is slowed down -> does not protect against fast dynamic events only static issues
- Can be enabled through configuration, currently not clear if it will be used in ATLAS operation, opted for slow reaction -> Overvoltage protection circuit shown to protect other modules

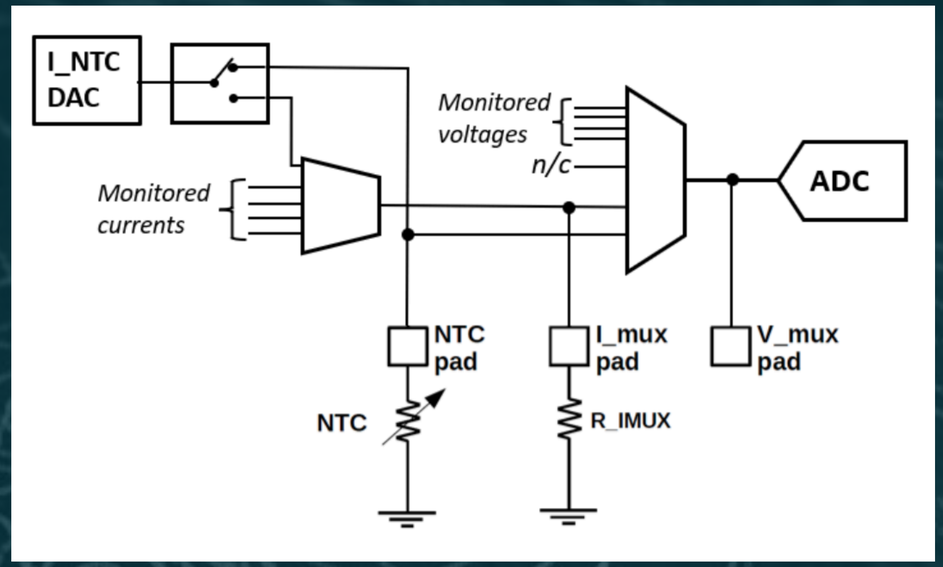


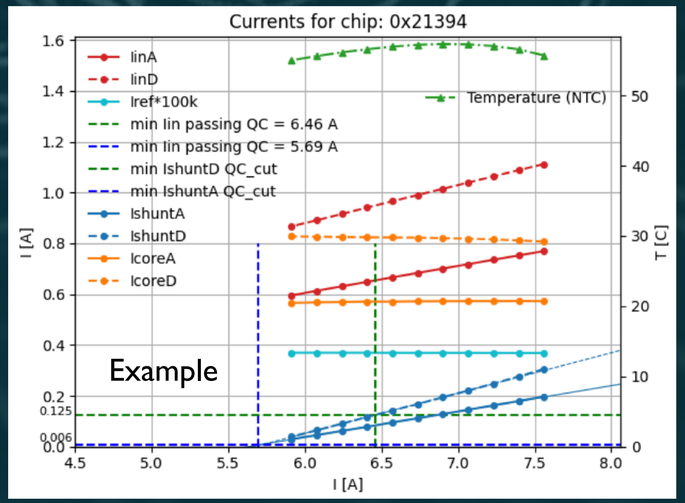



# Vmux/Imux

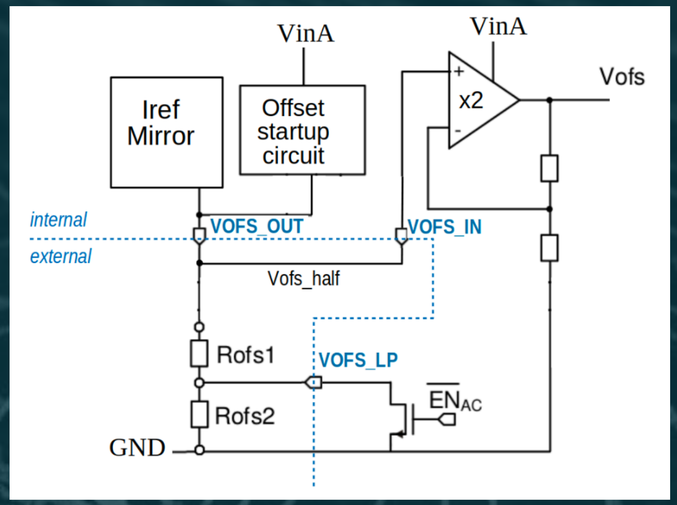
- Current consumption of chip can tell us a lot about its internal state, information not readily available in case of Serial Powering
  - Especially when trying to understand if SLDO powering is working well or during QC
- Voltage and current multiplexer vital in gaining insight into chip/module
  - During QC using off-chip DMM for high precision measurements (also used to calibrate ADC)
  - During operation can use on-chip ADC to keep tabs on internal state
- Culprit: ADC calibration will drift with radiation and did not include some stable absolute/external reference
  - E.g. total input current or magnetic field measurement

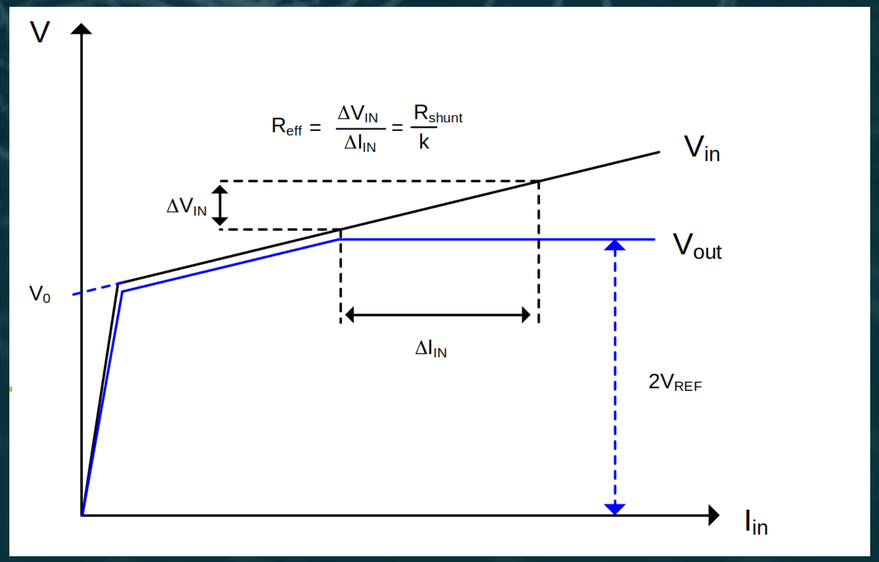


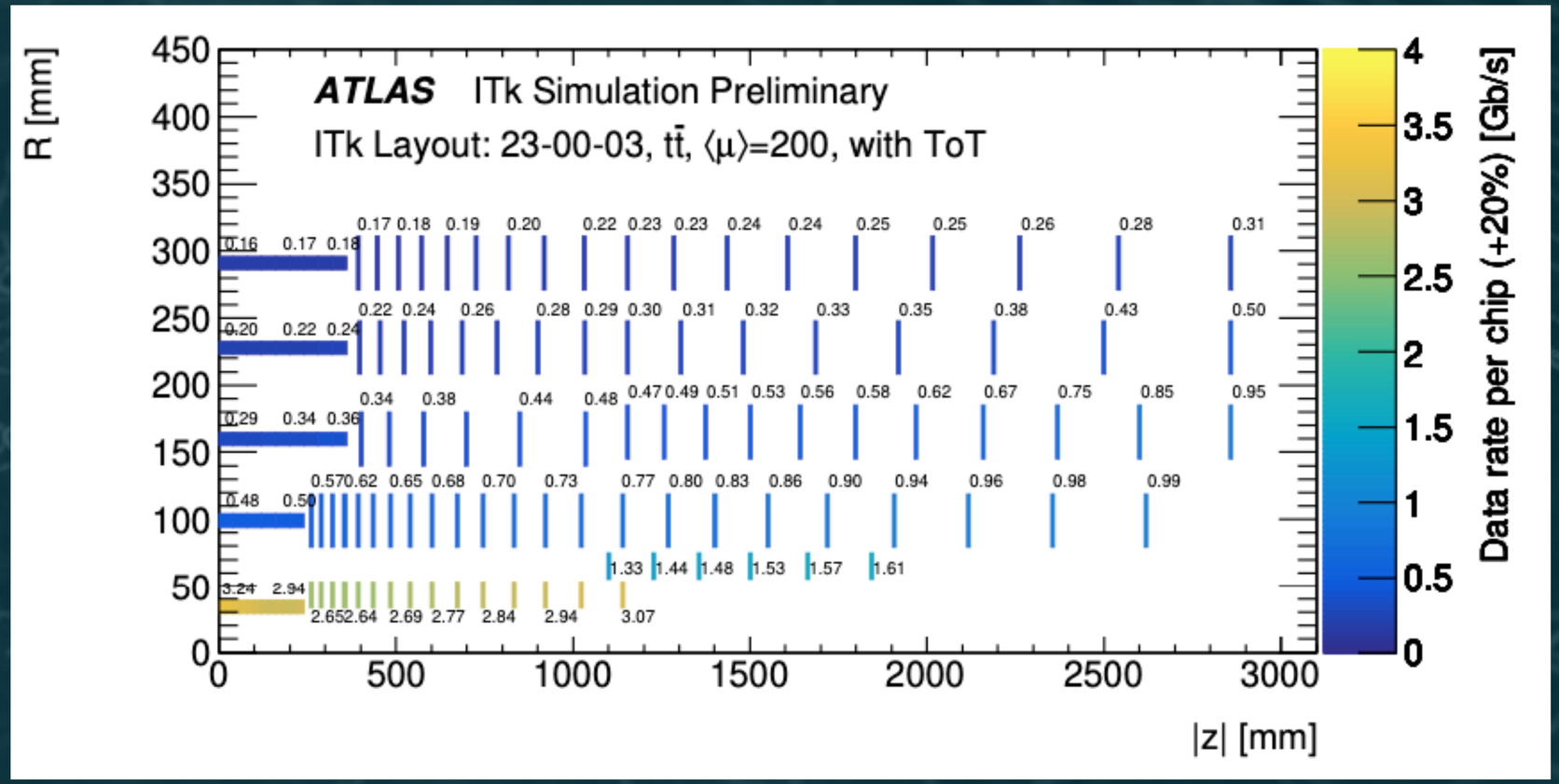
# Low Power Mode

- For serial power mode Voffset and Reff (slope) set through resistors on flex PCB -> fixed
  - Importantly ratio between Idig and Iana is fixed
- Reset state of chip is a low current state (= low Icore)
- But it's not possible to power the detector in a low current state because Vin would become to low
- Having low power mode is desirable during integration when cooling might not be available, e.g. to test cable connection
- Solution: allow for Voffset to be pushed up in order to power chip in lower current state
  - But because we cannot change the ratio between Iana/Idig, cannot go as low current as one might want to -> 0.2W/cm$^2$ vs 0.5-0.7W/cm$^2$
  - Additionally maxing out Voffset because Reff is typically chosen very low to protect against one-open failure case
- CMS afaik decided not to use LP mode, opting for a higher power reset state which avoids potential hot spots on the chip



# Data Links




- Same readout chip has to cover large range of hit/data rates
- Want data services mass to scale with data rate -> merge data from multiple chips into one link

# Link Configurations

BERKELEY LAB

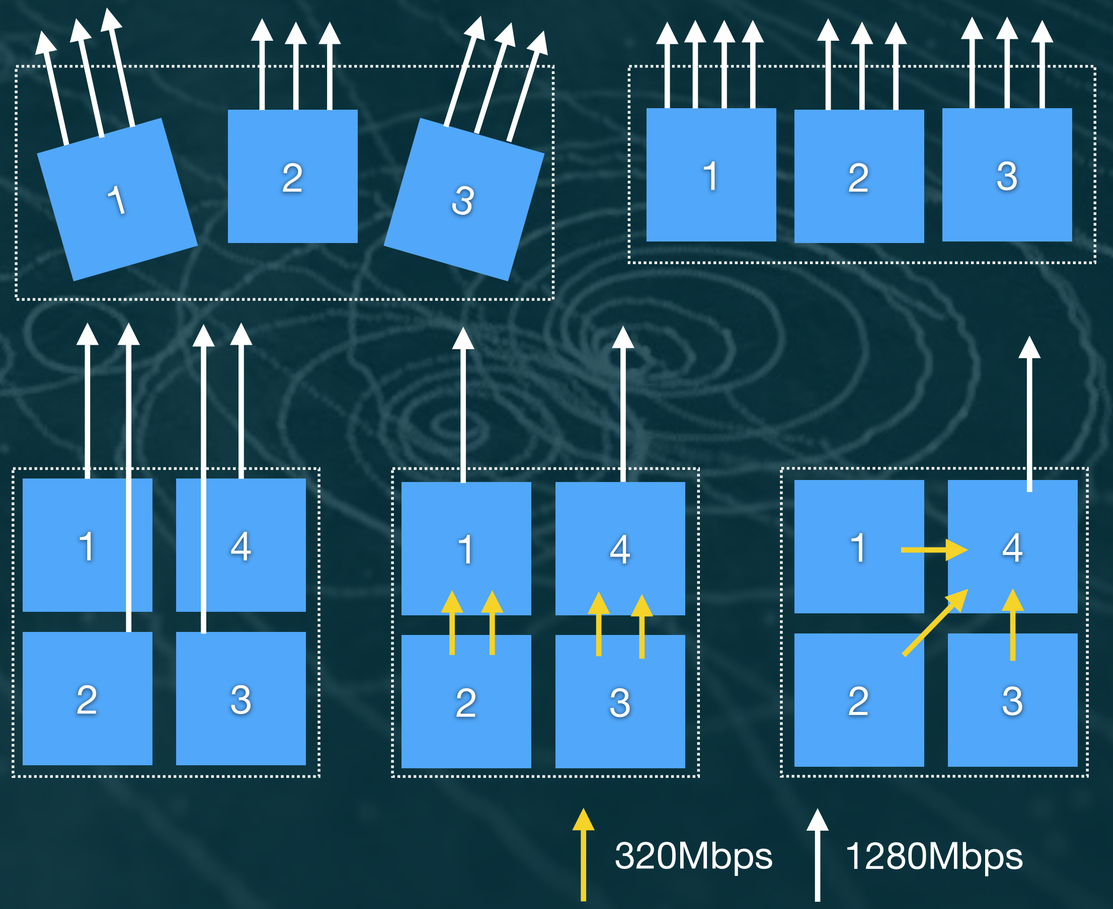
Common Quad Module:
- Three possible modes, chosen via chip configuration
  - 1 link per chip
  - 0.5 links per chip (1 primary, 1 secondary)
  - 0.25 links per chip (1primary, 3 secondary)

Triplet Module:
- Linear Triplet: 4 links per chip
- Ring Triplet: 3 links per chip

Triplet

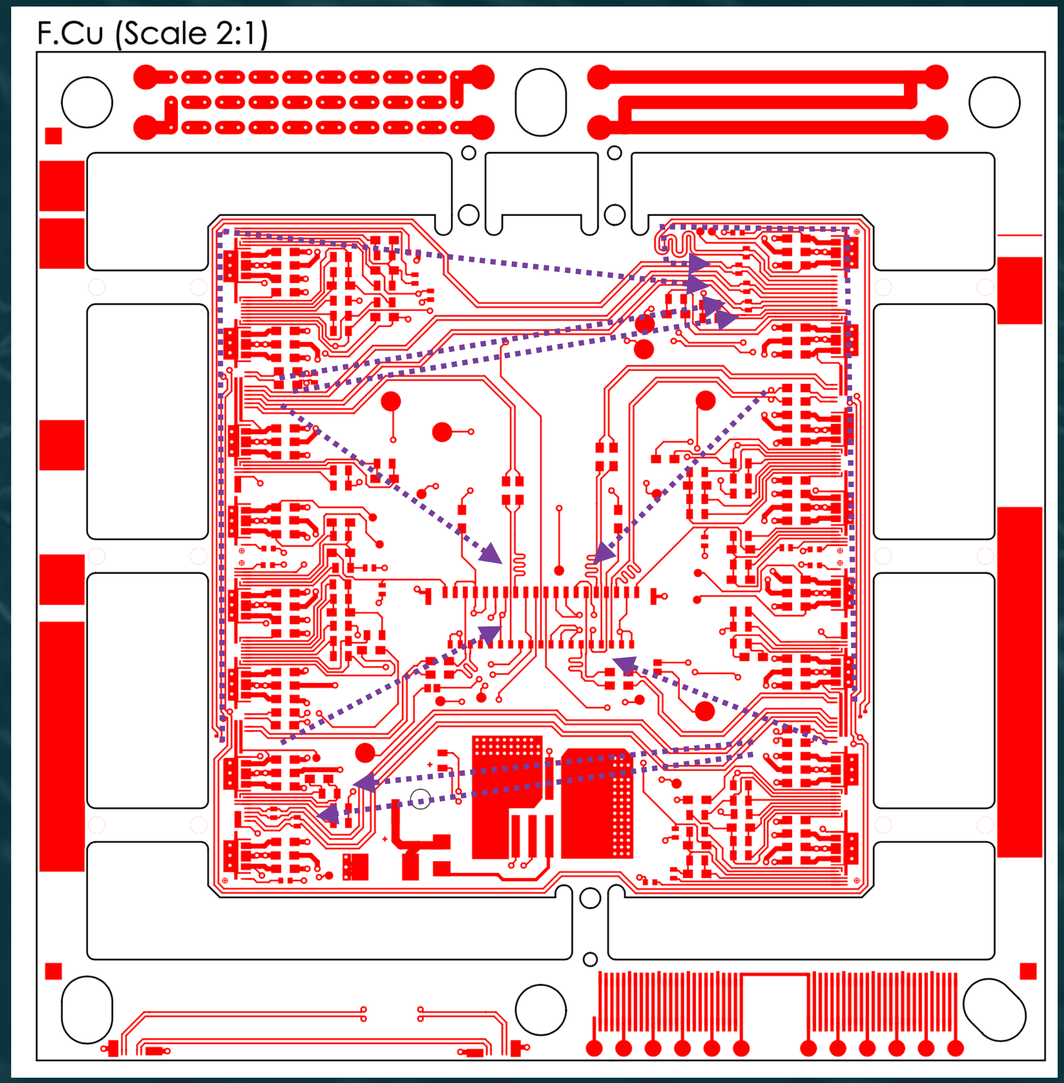
Common Quad

| Layer | Section | Number of Links/FE |
|---|---|---|
| 0 | Flat barrel | 4 |
| | Barrel rings | 3 |
| | End-cap rings | 2 |
| 1 | Flat barrel | 0.5 |
| | Barrel rings | 1 |
| | End-cap rings | 1 |
| 2 | Flat barrel | 0.5 |
| | Barrel rings | 0.5 |
| | End-cap rings (1-5) | 0.5 |
| | End-cap rings (6-11) | 1 |
| 3 | Flat barrel | 0.25 |
| | Barrel rings | 0.25 |
| | End-cap rings | 0.5 |
| 4 | Flat barrel | 0.25 |
| | Barrel rings | 0.25 |
| | End-cap rings (1-7) | 0.25 |
| | End-cap rings (8-9) | 0.5 |



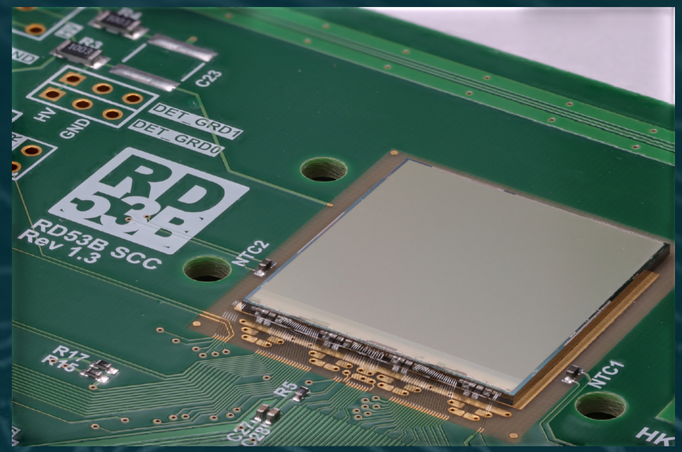
# Common Module Design

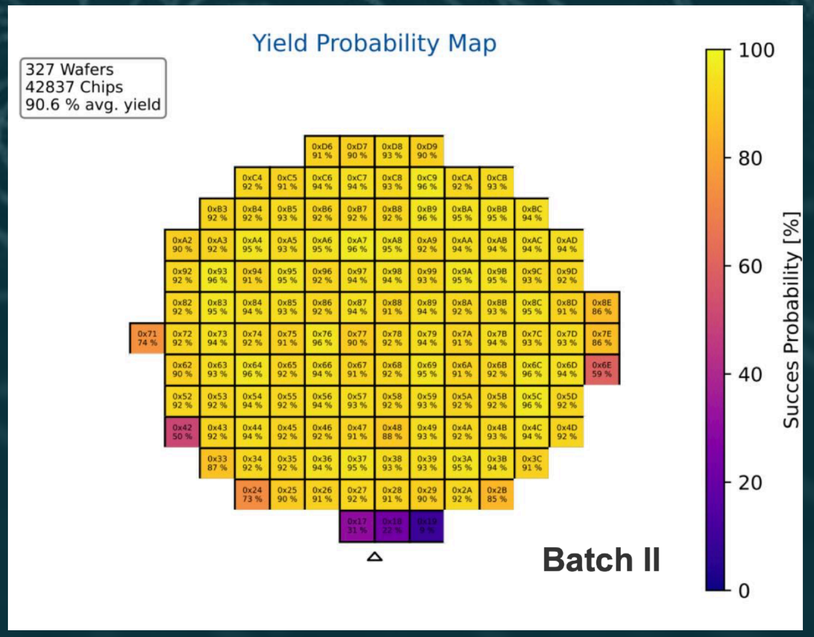
- Want one common module design that can support all required link configurations
- Also want low mass flex design with least amount of layers
- And need high speed (1.28Gbps) data signals to maintain signal integrity
- CMD signal is multi-drop LVDS bus shared between all chips
- Eventually arrived at 3 layer design with all high speed signal routing on the top layer
- Required some creative routing of data links that run between chips on perimeter of PCB
- Somewhat “lucky” that it all worked out, did not have this directly in mind when designing the chip
  - Could have potentially made this easier or even more versatile by having a slightly different pad layout and IO interface



# Summary & Conclusion

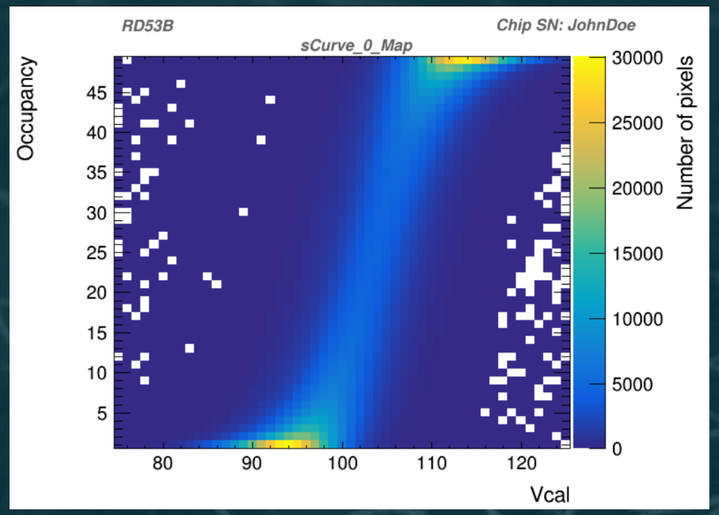
- To fulfill requirements in collider experiments need to make compromises in the front-end chip R&D phase
- Sometimes features thought to be important turn out to be not needed, and in other cases misc. features turn out to be absolutely vital
- Bench testing is becoming more and more complicated as operational environments are becoming more extreme - for any feature implemented ask ourselves how we will test it
- Ultimately the RD53C chip generation seems successful in fulfilling ATLAS & CMS requirements
- Chip production well underway (~30k chips out of 90k total) and seeing very good yield!

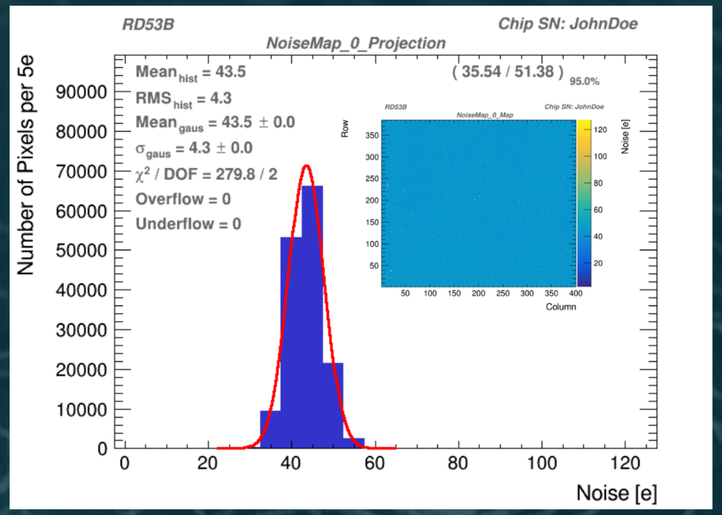


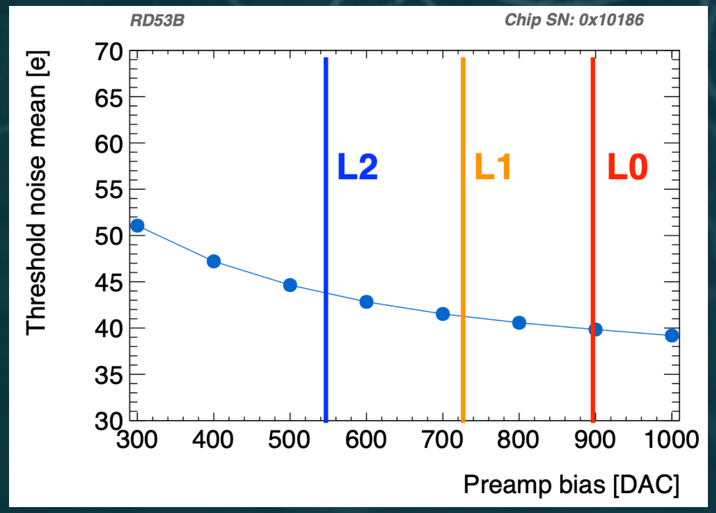



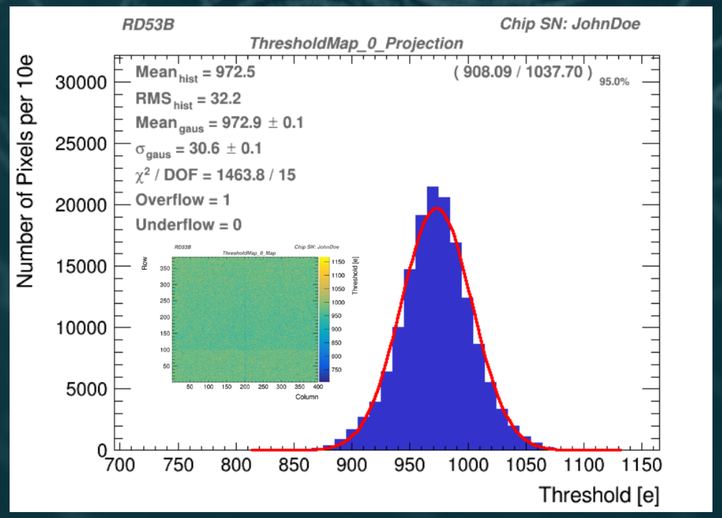
# Backup

# Threshold/Noise



# Data Protocol