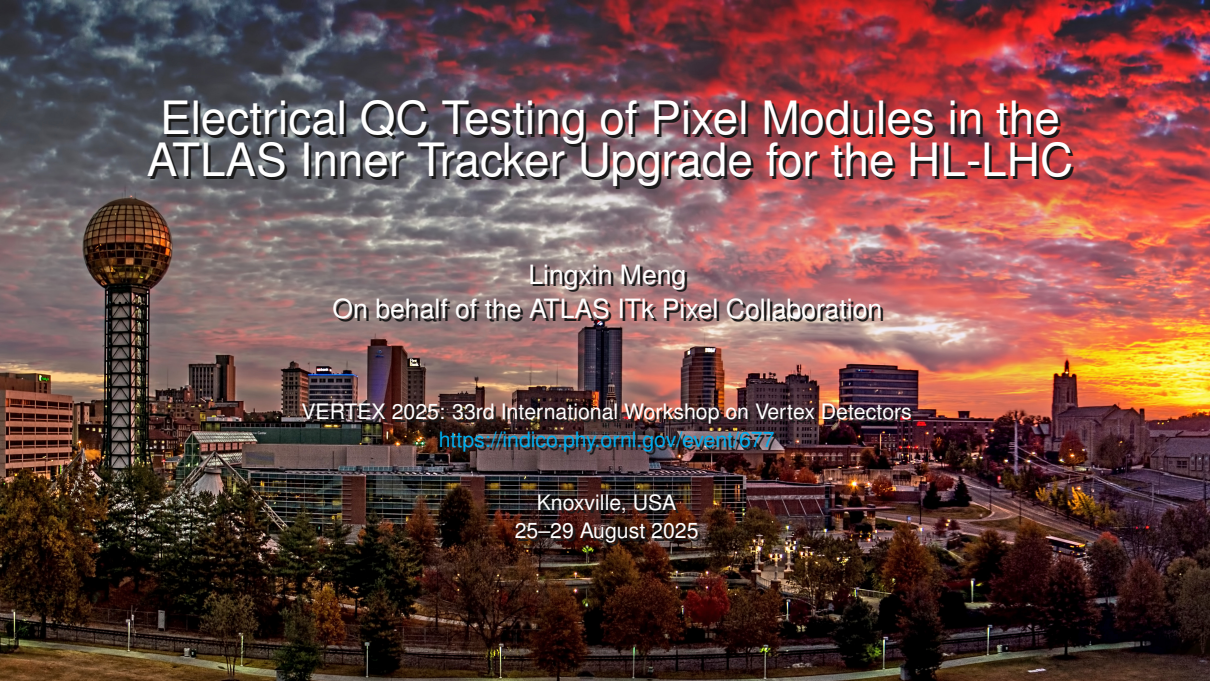
Electrical QC Testing of Pixel Modules in the ATLAS Inner Tracker Upgrade for the HL-LHC

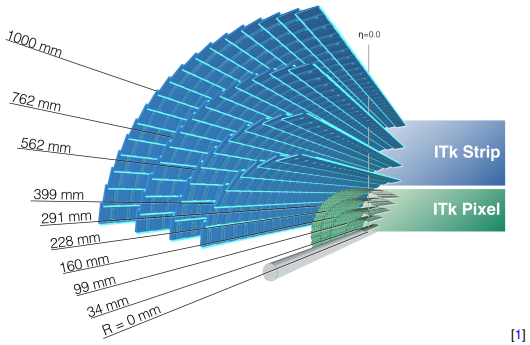
Lingxin Meng
On behalf of the ATLAS ITk Pixel Collaboration

VERTEX 2025: 33rd International Workshop on Vertex Detectors
https://indico.phy.ornl.gov/event/577

Knoxville, USA
25–29 August 2025



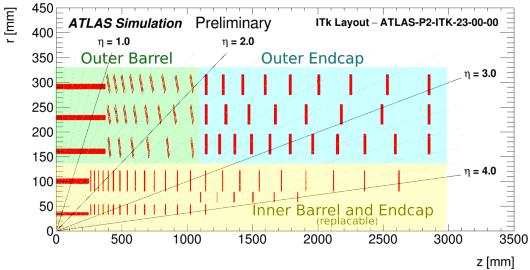
ITk Pixel Detector Layout



[1]

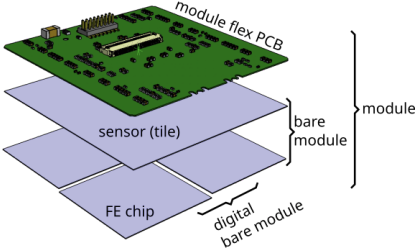
- ATLAS Inner Tracker Upgrade for the high luminosity era
- Replace the current Inner Detector with an all-silicon Inner Tracker
- Strip detector: $\sim$160 m^2 and 50M channels
- Pixel detector: $\sim$13 m^2 and 5B channels

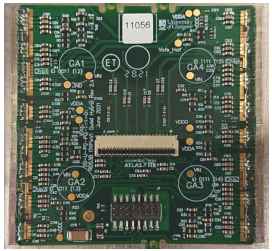
- Five pixel detector layers: L0–L4
- $\sim$10k modules will be built and tested at $\sim$25 sites world wide
- See Caterina's ITk overview talk on Monday



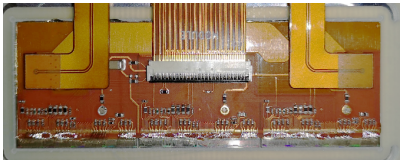
Pixel Module Flavours

- 8372 modules going into the detector
- L0: triplet modules ($\sim$ 5%) for barrel (linear) and rings (round)
  - Using single 3D sensors
- L1–4: quad modules ($\sim$ 95%)
  - Using quad planar sensors
- See Matias' talk on sensor testbeam results

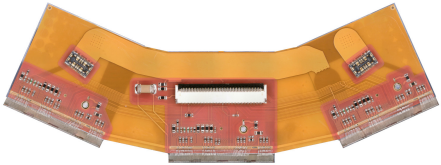




ITkPix v1.1 digital quad module on flexible printed circuit

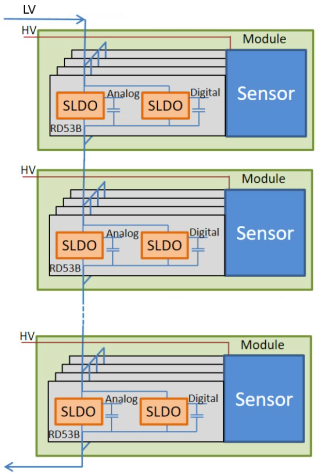


ITkPix v1 L0 linear triplet prototype



ITkPix v2 R0.5 round triplet module

Minimisation of Material Budget



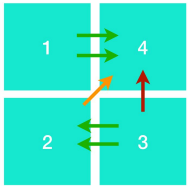
[2]

Serial powering:

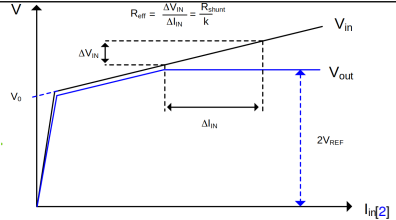
- On module: chips powered in parallel at 6.25 A (L2)
- On stave: modules powered in series of up to 14 modules
- Minimise material budget and thermal load in services

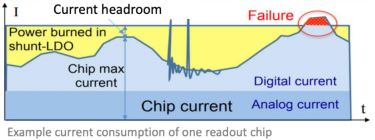
Data merging:

- Per FE chip up to 4×1.28 Gbps data uplinks $\rightarrow$ up to 16 links on a quad module
- Not all links required depending on module position and activity $\rightarrow$ data aggregation on FE chip
- Innermost layer: 12 links per triplet module (4 per FE)
  L3: down to 1 link per quad module (0.25 per FE)



RD53 Front-End Chip

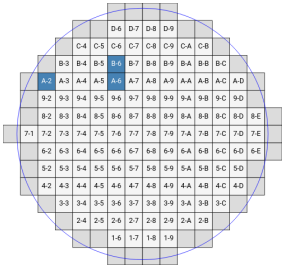




Example current consumption of one readout chip

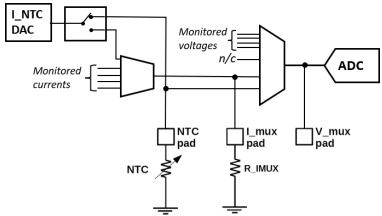
Powering

- On-chip shunt-LDO (SLDO) voltage regulator for serial powering
- Over-voltage protection
- Under-shunt protection
- Low-power mode



Identification:

- Unique efuse (e.g. 0x23F A 2) to encode a chip's wafer number, row and column position
- On module: 4-bit chip ID via wirebonds

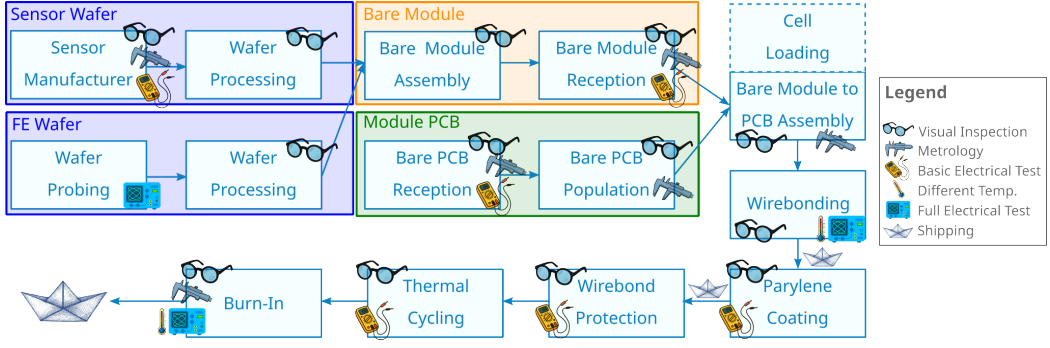


Monitoring:

- Analog multiplexer (MUX) for internal currents and voltages
- General purpose 12-bit ADC
- Temperature sensing via on-chip sensors or external NTC
- Ring oscillators for radiation monitoring

→ See Timon's talk about the RD53 FE chip on Tuesday ←

Pixel Module Production Flow



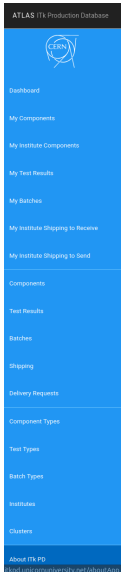
- Modules assembled and tested at about 25 institutes world wide - organisational challenge!
- Large diversity in laboratory infrastructure and production model

→ Development of exact specifications and procedures for each test

→ Development of common software tools for testing and accessing the central production database

→ Site qualification required for each assembly and testing site in many categories

Production Database (PDB)



Record of all parts used in the detector including their history and tests

- Outsourced to Unicorn University in Czech Republic
- Host of mongoDB of 25 GB, development of database API and GUI
- Hierachically structured by component types:
  - Each component type has intrinsic properties, parameters, **stages** and **tests** defined
  - A component type can have child component types and parent component types
  - Batches of components
  - Shipments
- Unique identifiers (UUID) or unique ATLAS serial number (SN) with encoding schemes
- Limited functionalities other than storage of information

Supplementary

- Large files stored on CERN EOS
- Custom `itkdb` python package as a wrapper to interface with the Unicorn API, used by most PDB interfacing common tools in ITk

Component Stages and Tests

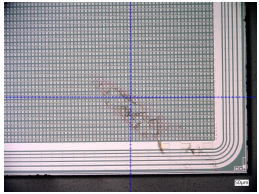
Stages / Components	FE Chip Stages	Sensor Stages	Bare Module Stages	Module Stages	HV Group Stages	SP Chain Stages	LLS Stages
FE Chip	FE tests		FE tests	FE tests	FE tests	FE tests	FE tests
Sensor		IV	IV	IV	IV	IV	IV
Bare Module							
Module				Module tests	Module tests	Module tests	Module tests
HV Group					HVG tests	HVG tests	HVG tests
SP chain						SPC tests	SPC tests
LLS							LLS tests

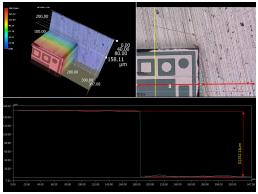
- All tests on a component defined in a pool associated with the lowest component
- Components get assembled onto parents and go through their stages
- At each stage always the same tests (or a subset) are run
- Only have to define the test once - ensure consistency of test definition and enable comparability between stages

Sensor QA/QC

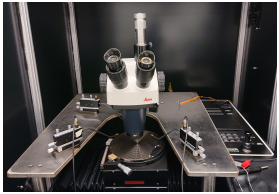
- Sensor QC (IV) on every sensor tile by the sensor vendor on the wafer, plus batch tests on test structures per wafer (CV)
- Sensor QA is done by a few ITk institutes on 1-2% per batch after dicing (QA'ed sensors will not be used in detectors)

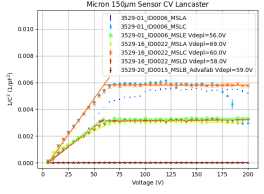
- Visual inspection of defects
- Metrology for thickness and bow measurements

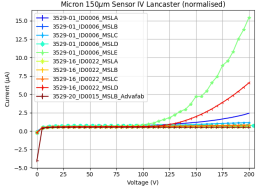




- IV, CV and IT (leakage current vs time)
- Irradiated samples
- Testbeam

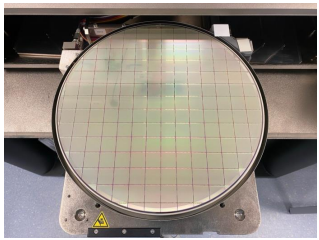


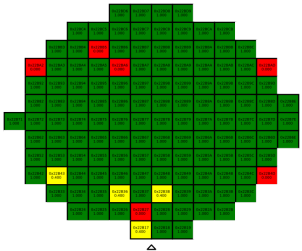


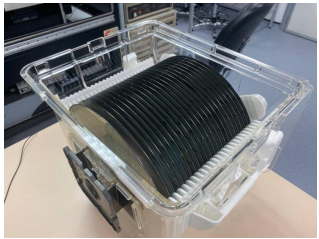


FE Wafer Probing

- All FE chip wafers are probed at ITk institutes using BDAQ before shipping to hybridisation vendors
- Bonn and Glasgow already probed production wafers
- Other sites (Paris, Hongkong) being qualified
- Rate (per site) is $\sim$1 wafer (131 chips) per day
- Exceptional yield of 90 %







Module Testing for Quality Control (QC)

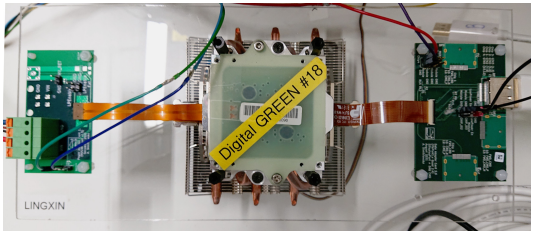
- Non-electrical QC aims to verify requirements:
  - Record any visible defects that can possibly lead to degradation in electrical performance
  - Ensure that physical module dimensions are suitable for a good thermal and mechanical performance
- Non-electrical tests: wirebond strength, visual inspection, metrology (module dimensions and bow)

- Electrical QC aims to verify two critical requirements:
  1. The module/chip has to function within the given system constraints
  2. Each module/chip has to have performance suitable for ”good physics”
- Electrical tests: sensor leakage current, FE calibrations and other basic chip functionalities, pixel matrix scans, tuning to provide a good configuration/baseline, and pixel failure evaluation
- Testing goals, detailled procedure and pass/fail criteria thoroughly documented

Module QC * Tools

Common elements for the testing setup:

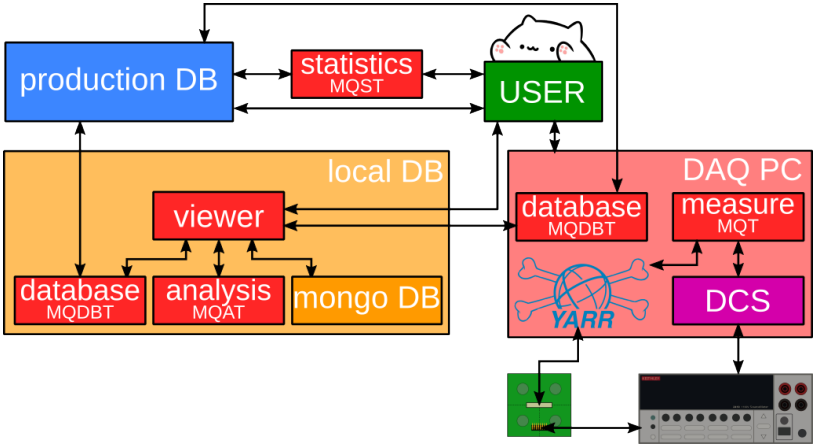
- Common modular enclosure to keep the module safe during handling and testing
- Common type-specific (for quads and triplets) power and data adapter boards and pigtails
- Module testing temperatures comparable to later stages with DCS, environmental control and monitoring
- Common design for coldbox available



Common QC software:

- Using YARR [3] as DAQ (SW and FW using commercial FPGA boards via common order)
- Module QC * Tools: `pip`-installable python packages:
  - module-qc-database-tools (MQDBT) [4] to interface with databases, e.g. generate config files or upload measurements
  - module-qc-measurement-tools (MQT) [5] to run measurements and record raw values
  - module-qc-analysis-tools (MQAT) [6] to interpret the measured results, do calibrations and apply cuts
  - local database (LDB) [7] to orchestrate these functionalities, automatically run analysis, act as local file manager
    Example here: → **https://itkpix-srv.ucsc.edu/localdb** ←
- Testing time per module full QC is 1h40 without IV and source scan → ∼2 hours per module

Interactions Overview



Module QC Electrical Tests

- Tests are ordered by relevance
- Sensor biased at operational voltage and module powered at nominal current
  (except sensor IV, SLDO and low power mode)
- Eye-diagram to obtain optimal data link delay settings
- Chip efuses always checked against expected

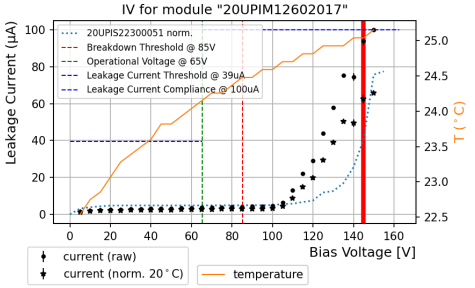
Simple (one test requires one input) and low level tests

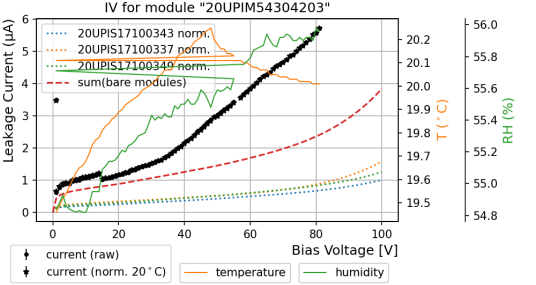
- Sensor IV
- Core column scan
- FE chip calibrations
  - Calibration of internal ADC
  - Analog register readback
  - SLDO regulator curve
  - Calibration of the injection circuit
  - Low power mode test
  - Data transmission

Complex (one test requires multiple inputs) and high level tests

- Minimum Health Test (MHT)
  - Digital scan
  - Analog scan
  - ToT scan
  - Threshold scan
- Tuning (TUN)
  - Global threshold tuning
  - ToT tuning
  - Global threshold tuning
  - Pixel threshold tuning
- Pixel failure analysis (PFA)
  - Digital scan
  - Analog scan
  - ToT scan
  - Threshold scan
  - Noise scan
  - Disconnected bump scan

Leakage Current vs Bias Voltage





- Measurement using `mqt`: defined voltage range, step, settling time and current compliance
- Analysis via `mqat`: output IV plot and results table
- Plot measurement, normalised current to 20 °C, voltage and current limits, breakdown indicator and environments
- Plot bare module IV: comparison required comparison by specification
- Triplet module: three single sensors are biased in parallel

IV_MEASURE for 20UPIM54304203

Parameter	Analysis result	QC criteria	Pass
BREAKDOWN_VOLTAGE	-999	[25, 999]	True
BREAKDOWN_REDUCTION	0	[-1, 10]	True
NO_BREAKDOWN_VOLTAGE_OBSERVED	True	-	-
MAXIMUM_VOLTAGE	81.04	-	-
LEAK_CURRENT	1.33	-	-
LEAK_INCREASE_FACTOR	1.21	[0, 2]	True
LEAK_PER_AREA	0.104	[0, 5]	True

ADC Calibration

Goal:

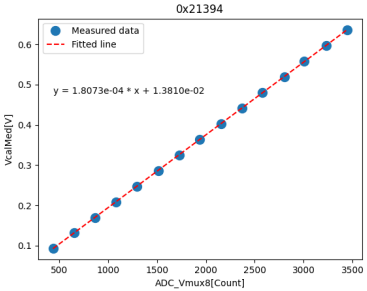
- Cross-check and update the ADC calibration done at wafer probing with the help of an external multimeter
- The calibrated ADC can be used to conduct all following measurements without an external multimeter

Procedure:

- Use the Vcal DAC range to output voltages
- Record the ADC count and measure the Vcal voltage via VMUX using an external multimeter

ADC_CALIBRATION for 0x21394

Parameter	Analysis result	QC criteria	Pass
ADC_CALIBRATION_SLOPE	0.181	[0.15, 0.224]	True
ADC_CALIBRATION_OFFSET	14.0	[-9, 31]	True
ADC_CALIBRATION_LINEARITY	0.65	[0.0, 4.0]	True
ADC_ANAGND30_MEAN	0.02	[0.012, 0.023]	True
ADC_ANAGND30_STD	0.0	-	-



Analog Register Readback

Goal:

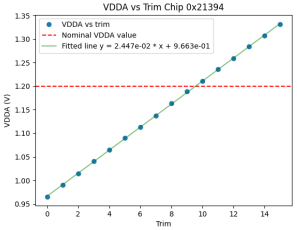
- Read back and verify all chip internal voltages and currents after configuration (e.g. reference voltage for over-voltage protection - VrefOVP)
- Cross-check and update the VDDA/D trim obtained at wafer probing

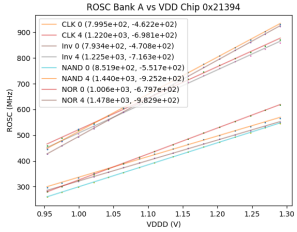
Measure:

- All internal currents and voltages
- Temperature using all on-chip sensors and external NTCs
- VDDA/D vs trim value
- All ring oscillators vs VDDD

ANALOG_READBACK for 0x21394

Parameter	Analysis result	QC criteria	Pass
AR_IREF	3.7e-06	[3.6e-06, 4.2e-06]	True
AR_GADC	0.776	[0.703, 0.924]	True
AR_VCALDAC	0.796	[0.668, 0.987]	True
AR_VREFCORE	0.457	[0.435, 0.49]	True
AR_VREFOVP	2.006	[1.8, 2.152]	True
AR_NOMINAL_SETTINGS	[0. ... 0.59]	-	-
ChipNTC_vs_ExtExt	-1.14	-	-
AR_VDDA_VS_TRIM	[0.96 ... 1.33]	-	-
AR_VDDD_VS_TRIM	[0.95 ... 1.29]	-	-
AR_VDDA_TRIM	10	[2.0, 13.0]	True
AR_VDDD_TRIM	11	[2.0, 13.0]	True
AR_ROSC_SLOPE	[799.48 ... 1628.39	-	-
AR_ROSC_OFFSET	[-462.21 ... -1061.9	-	-
AR_ROSC_MAX_RESIDUAL	[2.13 ... 1.63]	-	-
AR_VDDD_SATURATION	-1.0	-	-
AR_VDDA_SATURATION	-1.0	-	-
AR_IREF_TRIM	6	-	-





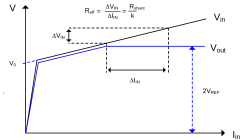
SLDO Regulator VI Curve

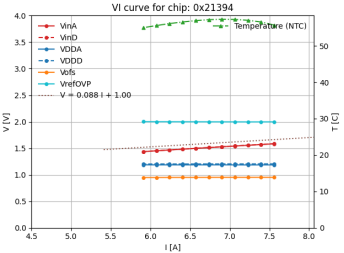
Goal:

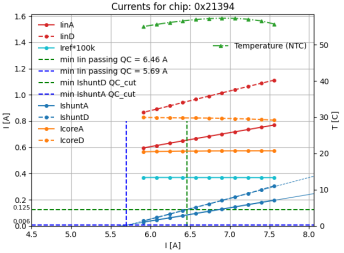
- Verify the characteristics of the SLDO curve
- Check all the FE chip internal values are within normal operational range (e.g. the shunt current)

Procedure:

- Record the voltage vs current at the linear portion from $\sim$7.5 A down to below the nominal current
- Measure relevant internal currents and voltages at each current point







SLDO for 0x21394

Parameter	Analysis result	QC criteria	Pass
SLDO_LINEARITY	0.029	[0, 0.09]	True
SLDO_VINA_VIND	-0.0	[-0.05, 0.05]	True
SLDO_VDDA	1.19	[1.18, 1.22]	True
SLDO_VDDD	1.2	[1.18, 1.22]	True
SLDO_VINA	1.452	[1.427, 1.603]	True
SLDO_VIND	1.454	[1.427, 1.603]	True
SLDO_VOFFS	0.949	[0.93, 1.03]	True
SLDO_IINA	0.613	[0.566, 0.663]	True
SLDO_IIND	0.89	[0.825, 0.978]	True
SLDO_IREF	3.7	-	-
SLDO_ISHUNTA	0.045	[0.006, 999]	True
SLDO_ISHUNTD	0.064	[0.125, 999]	False

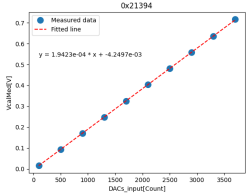
Calibration of the Injection Circuit

Goal:

- Cross-check and update the injection DAC (Vcal) calibration measured at wafer probing
- Measure injection capacitance to ensure chip tuning accuracy

Procedure for Vcal calibration:

- Scan the Vcal DAC from 100 to 4000
- Measure the Vcal value using VMUX

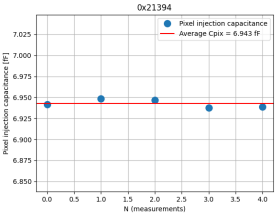


VCAL_CALIBRATION for 0x21394

Parameter	Analysis result	QC criteria	Pass
VCAL_MED_SLOPE	0.19	[0.16, 0.24]	True
VCAL_MED_OFFSET	-4.0	[-23, 17]	True
VCAL_MED_LINEARITY	0.81	[0.0, 4.0]	True
VCAL_MED_LINEARITY_SMALL_RANGE	0.88	-	-
VCAL_HIGH_SLOPE	0.19	[0.16, 0.24]	True
VCAL_HIGH_OFFSET	-1.0	[-23, 17]	True
VCAL_HIGH_LINEARITY	0.48	[0.0, 4.0]	True
VCAL_HIGH_LINEARITY_SMALL_RANGE	0.6	-	-
VCAL_HIGH_SLOPE_SMALL_RANGE_RATIO	0.5	[0.49, 0.51]	True
VCAL_MED_SLOPE_SMALL_RANGE_RATIO	0.5	[0.49, 0.51]	True

Procedure for injection capacitance:

- Measure from the capmeasure circuit I_{capmeas}, I_{cappar} and $VDDA_{\text{capmeas}}$ via VMUX



INJECTION_CAPACITANCE for 0x21394

Parameter	Analysis result	QC criteria	Pass
INJ_CAPACITANCE	6.94	[6.0, 9.0]	True

Low Power (LP) Mode

Goal:

- Verify functionality of the low power mode for the nominal low power current
- Ensure LP mode can be used during integration to check connectivity before the connection of cooling

Procedure:

- Send LP signal
- Power on module in at LP nominal current
- Measure relevant currents and voltages
- Run LP digital scan to ensure communication

LP_MODE for 0x21394

Parameter	Analysis result	QC criteria	Pass
LP_VINA	1.364	[1.39, 1.558]	False
LP_VIND	1.368	[1.39, 1.558]	False
LP_VOFFS	1.23	[1.229, 1.361]	True
LP_IINA	0.18	[0.15, 1.0]	True
LP_IIND	0.29	[0.25, 1.0]	True
LP_ISHUNTA	0.0031	[0.0001, 999]	True
LP_ISHUNTD	0.002	[0.0001, 999]	True
LP_DIGITAL_FAIL	82944	-	-

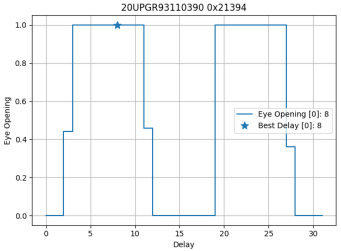
Data Transmission

Goal:

- Ensure data-link quality is sufficient for operation in the detector system with full services and connected to lpGBT
- Ensure on-module data aggregation is functional in different configurations

Procedure:

- Record an eye diagram with the DAQ
- Test data link sharing in 2-to-1 (0.5 link/FE) and 4-to-1 (0.25 link/FE) merging modes



DATA_TRANSMISSION for 0x21394

Parameter	Analysis result	QC criteria	Pass
EYE_WIDTH0	8	[3, 32]	True
4_TO_1	0	[1, 1]	False
2_TO_1	1	[1, 1]	True

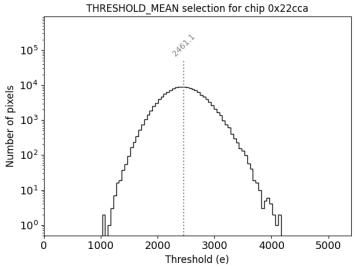
Minimum Health Test (MHT)

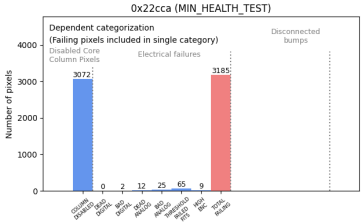
Goal:

- Minimal set of scans to check functionality of chip in between stages

MIN_HEALTH_TEST for 0x22cca

Parameter	Analysis result	QC criteria	Pass
THRESHOLD_MEAN	2461.14	-	-
THRESHOLD_SIGMA	332.13	-	-
NOISE_MEAN	118.79	-	-
NOISE_SIGMA	13.6	-	-
TOT_MEAN	8.66	-	-
TOT_SIGMA	2.03	-	-
BAD_ANALOG_INTEGRATED	3111	[0, 7680]	True
THRESHOLD_FAILED_FITS_INDEPENDENT	3168	[0, 7680]	True
HIGH_ENC_INDEPENDENT	15	[0, 1536]	True





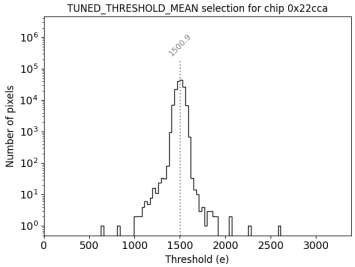
Tuning (TUN)

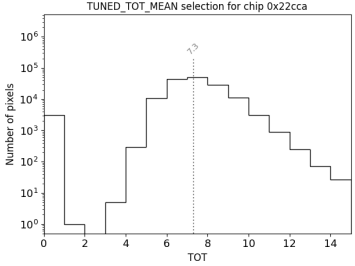
Goal:

- Check that a tuning was overall successful and the chip behaves as expected.

TUNING for 0x22cca

Parameter	Analysis result	QC criteria	Pass
TUNING_TUNED_THRESHOLD_MEAN	1500.9	[1350, 1650]	True
TUNING_TUNED_THRESHOLD_95_LOW	1426.26	-	-
TUNING_TUNED_THRESHOLD_95_HIGH	1570.61	-	-
TUNING_TUNED_THRESHOLD_SIGMA	38.0	[0, 100]	True
TUNING_TUNED_TDAC_MEAN	-1.4	[-6, 1]	True
TUNING_TUNED_TDAC_SIGMA	4.56	-	-
TUNING_TUNED_NOISE_MEAN	121.53	-	-
TUNING_TUNED_NOISE_SIGMA	12.05	-	-
TUNING_TUNED_NOISE_95_LOW	99.43	-	-
TUNING_TUNED_NOISE_95_HIGH	144.58	-	-
TUNING_TUNED_TOT_MEAN	7.3	[6, 8]	True
TUNING_TUNED_TOT_SIGMA	0.3	[0, 1]	True
TUNING_TUNED_TOT_95_LOW	5.0	-	-
TUNING_TUNED_TOT_95_HIGH	10.08	-	-
TUNING_TUNED_THRESHOLD_FAILED_FITS	3110	-	-

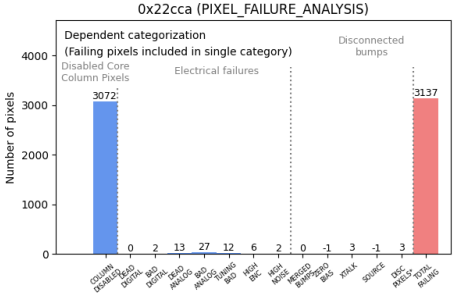




Pixel Failure Analysis (PFA)

Goal:

- Ensure good physics data efficiency and determine number of failed pixels in each category



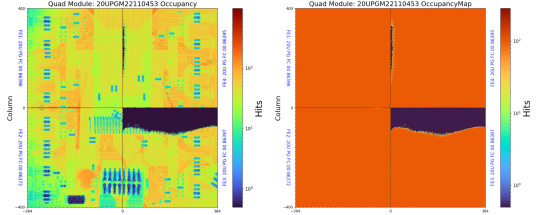
*DISC PIXELS uses combination of various disc. bump identificaiton methods, and is used to count the TOTAL FAILING category

- High to low level exclusive pixel failure categories
- Distinction between electrical and bump bond failure

PIXEL_FAILURE_ANALYSIS for 0x22cca

Parameter	Analysis result	QC criteria	Pass
ELECTRICALLY_FAILED	3134	[0, 7680]	True
DISCONNECTED_PIXELS	3	[0, 7680]	True
FAILING_PIXELS	3137	[0, 7680]	True

- Retiring source scan to be performed batch-wise
  - Radiation protection, setup, handling requirements
  - Disadvantage due to SMD components vs duration
- Crosstalk-based disconnected bump scan with analog injections into neighbouring pixels
  - As fast as analog scan and very reliable

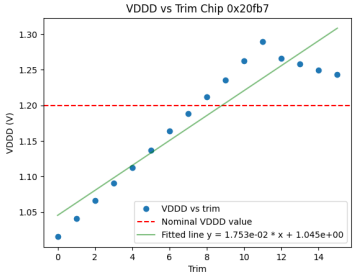


Source scan vs crosstalk-based scan to determine broken bump bonds

Issues Encountered

- Core column issue: see Charlie's core column talk on Tuesday
  - Core column scan added into module QC routine, further developments and investigations ongoing

- VDD trim saturation
  - VDDA and VDDD: voltage regulator trimmable via DAC
  - Measure the full range and determine the best trim for 1.2 V
  - Saturation often seen on modules, not observed during wafer probing, likely due to different powering conditions and power-sharing on module
  - Some chips on a module go into undershunt - less severe when given more power
  - ✓ Improved/solved by increasing the nominal current (6.06 A → 6.25 A for outer system quads)

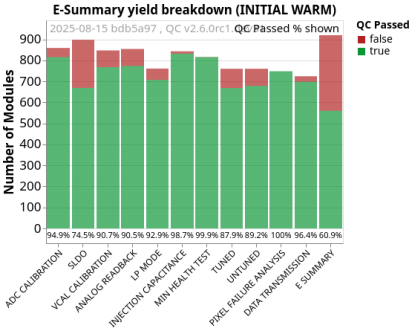


PreProd_03 FE1	AnaGND30	0.06	[0.015, 0.023]
PreProd_08 FE1	AnaGND30	0.024	[0.015, 0.023]
PreProd_12 FE1	AnaGND30	0.054	[0.015, 0.023]
PreProd_13 FE1	AnaGND30	0.08	[0.015, 0.023]
DgtFeb01 FE1	AnaGND30	0.024	[0.015, 0.023]
DgtP1 FE1	AnaGND30	0.026	[0.015, 0.023]

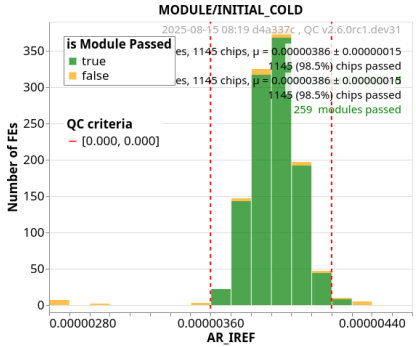
- Varying analog ground measurement
  - During site qualification observed large differences
  - Chip quantities through VMUX measured against module GND
  - Chip analog GND has an offset vs module GND defined only by the flex design and wirebonds
  - ✓ Diagnosed to be from GND loops in site-specific multi-module setup

Module Data Reporting - Module QC Statistical Tools

- We notice most of the issues through support on Mattermost and during site qualification
- Need to closely monitor systematic behaviour of relevant quantities
- ”Module QC Statistical Tools” create a website with module resports that shows various quantitites on all module data in the PDB
- Updated on a daily basis via git pipeline



Yield breakdown of each parameter per test



Distribution of each parameter value

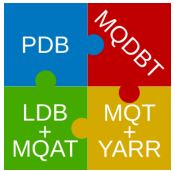
Conclusion and Outlook

Ready for ITk pixel module production:

- Developed a comprehensive QC testing suite with good documentation and robust software development
- Cover more than only electrical QC testing: interaction with databases, measurements, analysis, interpretations, visualisations and GUI
- Module electrical QC tests are in very good shape thanks to year long discussions and work at all fronts: test specifications, PDB structure, software development, user support and feedback, and careful monitoring of data

Future improvements

- Core column scan to cover more cases, e.g. threshold dependence
- Increase testing speed and automation, e.g. move to fileless communication between software packages
- Develop module categorisation and scoring system
- Support for module testing on loaded local support - many tests already work with FELIX HW



References I

[1] Georges Aad et al.
Expected tracking performance of the ATLAS Inner Tracker at the High-Luminosity LHC.
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[2] The RD53 collaboration et al.
RD53 pixel readout integrated circuits for ATLAS and CMS HL-LHC upgrades.
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[3] B Gallop T Heim et al.
Yarr: Yet another rapid readout, August 2025.
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[4] ATLAS ITk Pixel Collaboration.
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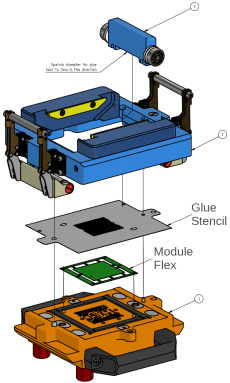
https://doi.org/10.5281/zenodo.15580222.

[7] ATLAS ITk Pixel Collaboration.
atlas-itk-pixel-modules/ldb, August 2025.
https://doi.org/10.5281/zenodo.16389123.

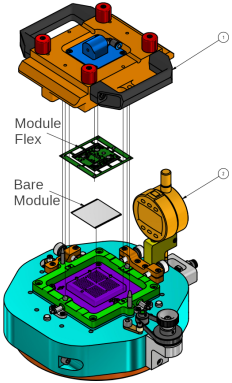
extra slides

Module Assembly

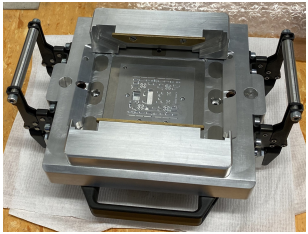
- All modules assembled by hand, using common custom tools
- Dispense glue via stencil to attach bare module (sensor-FE) and module flexes
  - Glue choice: thermal/electrical conductivity, mechanical property (hard, soft), strength, radiation hardness, thermal expansion → can potentially destroy bump bonds and more (see the Strips talk next week)
  - Glue pattern (stress), distribution/thickness → liquid is difficult to control
  - Very tight constraints → small tolerances of a few 10 μm

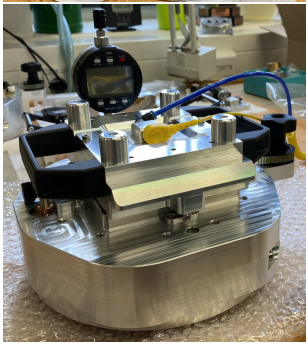


Dispense glue via stencil onto flex

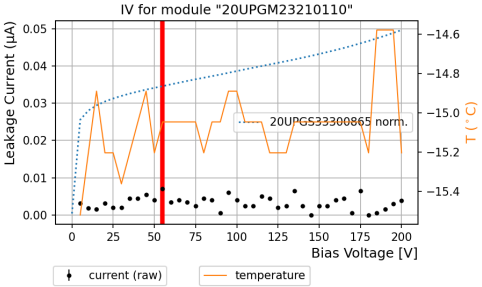


Assemble flex onto bare module





IV Analysis



- Original breakdown definition made for IV on sensor tile works fine on nice measurements performed on probestations
- IV measurement on a modules has more fluctuation
- Precision of HV supply often worse than specified - barely able to measure currents when cold

→ Simplify breakdown definition using leakage current as limit

Module QC Database Tools (MQDBT)

- `python -m pip install module-qc-database-tools`
- Repo: https://gitlab.cern.ch/atlas-itk/pixel/module/module-qc-database-tools
- Mostly used to generate module and chip configuration files once the module finishes the assembly stage
  - `mqdbt generate-yarr-config --sn <ATLAS serial number>`
  - Fills minimal values taken from wafer probing results: ADC calibration, Iref trim

```
[08/17/25 00:16:04] INFO     [core] chip 0x22d62 initiated.
[08/17/25 00:16:05] INFO     [core] chip 0x22d84 initiated.
[08/17/25 00:16:07] INFO     [core] chip 0x22d7a initiated.
[08/17/25 00:16:08] INFO     [core] chip 0x22d86 initiated.
                    INFO     [core] sensor 20UPGS33303840 initiated.
                    INFO     [core] quad module 20UPGM23211221 initiated.
INFO: Getting layer-dependent config from module SN...
                    INFO     [core] Generating module config for module 20UPGM23211221 with L2 from latest version for 1280 MHz.
                    INFO     [core] Latest chip configs found for FE1 (chip 0x22d62) L2 warm!
[08/17/25 00:16:10] INFO     [core] Generating chip config for readout at 1280 MHz.
                    INFO     [core] Latest chip configs found for FE2 (chip 0x22d84) L2 warm!
[08/17/25 00:16:11] INFO     [core] Generating chip config for readout at 1280 MHz.
                    INFO     [core] Latest chip configs found for FE3 (chip 0x22d7a) L2 warm!
[08/17/25 00:16:13] INFO     [core] Generating chip config for readout at 1280 MHz.
                    INFO     [core] Latest chip configs found for FE4 (chip 0x22d86) L2 warm!
[08/17/25 00:16:15] INFO     [core] Generating chip config for readout at 1280 MHz.
module connectivity file saved to v2test/20UPGM23211221/20UPGM23211221_L2_warm.json
FE1 config file saved to v2test/20UPGM23211221/L2_warm/0x22d62_L2_warm.json
FE2 config file saved to v2test/20UPGM23211221/L2_warm/0x22d84_L2_warm.json
FE3 config file saved to v2test/20UPGM23211221/L2_warm/0x22d7a_L2_warm.json
FE4 config file saved to v2test/20UPGM23211221/L2_warm/0x22d86_L2_warm.json
module information saved to v2test/20UPGM23211221/20UPGM23211221_info.json
```


```
"ITKPIXV2": {
  "GlobalConfig": {
    "AuroraActiveLanes": 1,
    "CdrcClkSel": 0,
    "CmlBias0": 800,
    "CmlBias1": 400,
    "CmlBias2": 0,
    "SerEnTap": 1,
    "SerInvTap": 1,
    "MonitorEnable": 1,
    "MonitorI": 63,
    "MonitorV": 32,
    "ServiceBlockEn": 1,
    "ServiceBlockPeriod": 50,
    "DiffLcc": 200,
    "DiffLccEn": 1,
    "DiffPreComp": 350,
    "DiffPreampL": 550,
    "DiffPreampM": 550,
    "DiffPreampR": 550,
    "DiffPreampT": 550,
    "DiffPreampTL": 550,
    "DiffPreampTR": 550,
    "Diffvff": 60,
    "EnCoreCol0": 65535,
    "EnCoreCol1": 65535,
    "EnCoreCol2": 65535,
    "EnCoreCol3": 63,
    "DataMergeOutMux0": 2,
    "DataMergeOutMux1": 3,
    "DataMergeOutMux2": 0,
    "DataMergeOutMux3": 1,
    "SerEnLane": 15,
    "SerSelOut0": 3,
    "SerSelOut1": 3,
    "SerSelOut2": 1,
    "SerSelOut3": 3,
    "SldoTrimA": 9,
    "SldoTrimD": 6
  },
  "Parameter": {
    "ADCcalPar": [8.224, 0.183, 10000.0],
    "InjCap": 7.878999999999999,
    "KSenseInA": 21179.821,
    "KSenseInD": 21663.984,
    "Name": "0x22d62",
    "ChipId": 12,
    "NfOSLDO": 1.2606678246083638,
    "NfASLDO": 1.2607392456916107,
    "NfACB": 1.2596536455262572,
    "VcalPar": [13.266, 0.196],
    "IrefTrim": 6,
    "KSenseShuntA": 21785.0,
    "KSenseShuntD": 22283.0,
    "KShuntA": 1010.95,
    "KShuntD": 997.087
  }
}
```

Module QC Database Tools - Other Functions

```
checks for 20UPGM23211221
├── ✓ check_attachments_exist_electrical(test_run, component)
├── ✗ check_attachments_exist_vis_inspect(test_run)
│   ├── ✗ 67bde262d89b87c79af8efbc (VISUAL_INSPECTION @ MODULE/ASSEMBLY): Missing front_image attachment
│   ├── ✗ 6798b6cc0205a7d43b024673 (VISUAL_INSPECTION @ BAREMODULERECEPTION): Missing front_image attachment
│   └── ✗ 67b896acd89b87c79ae5b265 (VISUAL_INSPECTION @ PCB_RECEPTION_MODULE_SITE): Missing front_image attachment
├── ✓ check_chip_configs(component)
├── ✗ check_duplicate_attachment_titles(test_run)
│   ├── ✗ 685bbc849092149c9f0c3a76 (VISUAL_INSPECTION @ MODULE/PARYLENE_UNMASKING): Test run has attachments with duplicate titles
│   ├── ✗ 68793a962cb2a5e98161c5ab (VISUAL_INSPECTION @ MODULE/WIREBOND_PROTECTION): Test run has attachments with duplicate titles
│   ├── ✗ 687941f7207cb9964803dd99 (VISUAL_INSPECTION @ MODULE/FINAL_COLD): Test run has attachments with duplicate titles
│   ├── ✗ 68793b9a2cb2a5e98161ce63 (VCAL_CALIBRATION @ MODULE/POST_PARYLENE_WARM): Test run has attachments with duplicate titles
│   └── ✗ 687941702cb2a5e98161e1cd (VCAL_CALIBRATION @ MODULE/FINAL_COLD): Test run has attachments with duplicate titles
├── ✓ check_iv_measure_bare_module(component)
├── ✓ check_iv_measure_sensor_tile(component)
├── ✓ check_missing_fechip_test_data(test_run)
├── ✗ check_missing_links_esummary(test_run)
│   ├── ✗ 67ee541973b21e31354b2043 (E_SUMMARY @ MODULE/INITIAL_COLD): Link is not set for MODULE_LP_MODE_FE_LINK_1
│   ├── ✗ 685bbcca6734e57026e048a2 (E_SUMMARY @ MODULE/PARYLENE_UNMASKING): Link is not set for MODULE_ADC_CALIBRATION_FE_LINK_1
│   └── ✗ 687941cc207cb9964803dcd0 (E_SUMMARY @ MODULE/FINAL_COLD): Link is not set for MODULE_LP_MODE_FE_LINK_1
├── ⊘ check_mqat_version(top_component, component, test_run)
├── ⊘ check_mqt_version(top_component, component, test_run)
└── ✓ check_same_stage(top_component, component)
```

← component review

Summary

Checks	Count
Total	1686
Passed	463
Failed	11
Not Ran	0
Skipped	1212
Grade	97.7%

All other `mqdbt` functions →

Commands

component	Commands to run on components
fetch-reference-iv	Main executable for fetching reference IVs from either production DB (default) or local DB.
generate-yarr-config	Main executable for generating yarr config.
get-bom-info	Main executable for get BoM Information
get-vfd-info	Main executable for get Vfd Information
ls	List up components stored in LocalDB.
recycle-analysis	Main executable for recycling a single analysis. !!! note "Added in version 2.5.1"
recycle-esummary	Main executable for bulk recycling a module entirely for each individual e-summary. !!! note "Added in version 2.5.0"
register-component	Main executable for registering components.
review-component	Main executable for reviewing component uploaded to Prod DB.
run-full-qc	Main function to execute all QC scans.
show-qc-pipeline	Summarize the QC pipeline status. Can specify "pre-production (v1.1)" or "production (v2)", and on top of that user can select modules by regex match to serial numbers using the -c option.
show-qc-status	Show the QC status of a component and its sub-components.
show-test	Show the contents of a test run in LocalDB. Only specifying the serial number will provide candidate test runs interactively.
sync-component-stages	Main executable for syncing component stages recursively.
upload-measurement	Walk through the specified directory (recursively) and attempt to submit all json files to LocalDB as the QC measurement
upload-test	List tests missing PDB uploading, and submit the selected test to ITkPD.

Module QC Measurement Tools (MQT)

- `python -m pip install module-qc-tools`
- Repo: https://gitlab.cern.ch/atlas-itk/pixel/module/module-qc-tools
- Interfaces with DAQ (and DCS if necessary)
- `mqt measurement <measurement> -c <hardware config> -m <connectivity>`
- Outputs raw values (no conversion/interpretation/fit) → rerun analysis if necessary
- Output data format strictly defined and schema-validated

Commands

adc-calibration	Records ADC counts against external measurements of the same voltage.
analog-readback	Reads back chip registers and records voltages vs trims of VDDA/D.
data-transmission	Run the Data Transmission measurement consisting of eye diagram and data merging check.
injection-capacitance	Measurement of chip parameters relevant to calculate the injection capacitance.
iv-measure	Records the sensor leakage current vs reverse bias voltage.
long-term-stability-dcs	Collect DCS data for the long-term stability test (high-voltage power, module temperature).
lp-mode	Set the module in low power mode, read registers and run LPM digital scan.
overvoltage-protection	Tests chip's overvoltage protection. Run in low power mode and requires the LP config.
sldo	Records the shunt LDO (SLDO) voltage vs input current.
undershunt-protection	Tests chip's undershunt protection. Run in low power mode and requires the LP config.
vcal-calibration	Records externally measured voltage against Vcal settings.

Module QC Analysis Tools (MQAT)

- `python -m pip install module-qc-analysis-tools`
- Repo: https://gitlab.cern.ch/atlas-itk/pixel/module/module-qc-analysis-tools
- Central repository/package for all module level electrical and non-electrical analysis
- Take well-defined measurement inputs (from `mqt` or other sources with the same schema)
- `mqat analysis <analysis> -i <input measurement>`
- Package and functions can be imported by other tools, e.g. localDB or software for loaded local support measurements
- Convert values using calibrated chip parameters, plots and pass/fail using a cut-file

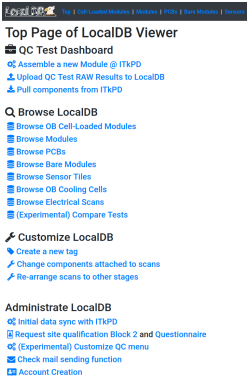
Commands

adc-calibration	Performs the ADC calibration.
analog-readback	Performs the Analog Readback.
bare-module-sensor-iv	
cutter-pcb-tab	
data-transmission	Performs the data transmission.
de-masking	
flatness	This analysis script performs QC criteria checks on the flatness measurement.
glue-module-flex-attach	
injection-capacitance	Performs the injection capacitance.
iv-measure	Analyses sensor leakage current vs voltage measurement.
long-term-stability-dcs	
lp-mode	Performs the Low Power mode analysis.
mass-measurement	
mln-health-test	Performs the minimum health analysis of YARR Scans.
overvoltage-protection	Performs the Overvoltage protection analysis.
parylene	
pixel-failure-analysis	Classifies pixel failures and performs the pixel failure analysis.
quad-bare-module-metrology	Performs analysis of quad bare module metrology.
quad-module-metrology	Performs analysis of quad module metrology.
sldo	Analyses the SLDO curve.
thermal-cycling	
triplet-metrology	
tuning	Analyzes the tuning performance from YARR scans.
undershunt-protection	Performs the Undershunt protection analysis.
vcal-calibration	Performs the VCal calibration.
visual-inspection	
wirebond-pull-test	Classifies pulls and performs the pulltest statistics.
wirebonding-information	
wp-envelope	Performs analysis of wire bonding protection roof envelope. The QC procedure is described in the following documentations: - https://edms.cern.ch/ui/file/2648149/1/OB_WBMP_Assembly_Procedure.pdf - https://edms.cern.ch/file/2648149/1/SQ_OBWBP_v8.pptx Tests are implemented in test_cli.py with a command "wp-envelope" Presentation; https://indico.cern.ch/event/1529894/

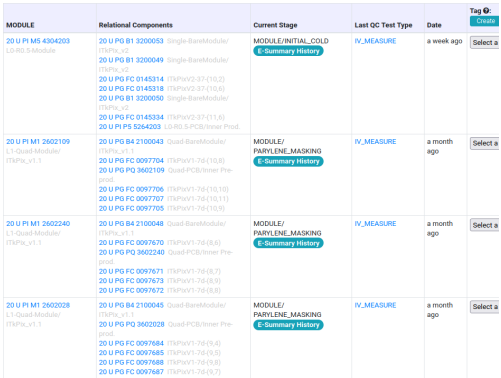

```
"ADC_CALIBRATION": {
  "ADC_CALIBRATION_SLOPE": { "sel": [0.15, 0.224], "precision": 3 },
  "ADC_CALIBRATION_OFFSET": { "sel": [-9, 31], "precision": 0 },
  "ADC_CALIBRATION_LINEARITY": { "sel": [0.0, 4.0], "precision": 2 },
  "ADC_ANAGND30_MEAN": {
  "LZero": { "sel": [0.003, 0.055], "precision": 3 },
  "LOne": { "sel": [0.018, 0.026], "precision": 3 },
  "LTwo": { "sel": [0.012, 0.023], "precision": 3 }
  }
},

"SLDO": {
  "SLDO_LINEARITY": { "sel": [0, 0.09], "precision": 3 },
  "SLDO_VINA_VIND": { "sel": [-0.05, 0.05], "precision": 2 },
  "SLDO_VDDA": { "sel": [1.18, 1.22], "precision": 2 },
  "SLDO_VDDD": { "sel": [1.18, 1.22], "precision": 2 }
},
"ANALOG_READBACK": {
  "AR_VDDA_TRIM": {"sel": [2.0, 13.0], "precision": 0 },
  "AR_VDDD_TRIM": { "sel": [2.0, 13.0], "precision": 0 },
  "AR_IREF": { "sel": [3.6e-6, 4.2e-6], "precision": 7 },
  "AR_GADC": {
      "LZero": { "sel": [0.666, 0.985], "precision": 3 },
      "LOne": { "sel": [0.703, 0.924], "precision": 3 },
      "LTwo": { "sel": [0.703, 0.924], "precision": 3 }
  },
  "AR_VCALDAC": { "sel": [0.668, 0.987], "precision": 3 },
  "AR_VREFCORE": { "sel": [0.435, 0.49], "precision": 3 },
  "AR_VREFOVP": { "sel": [1.800, 2.152], "precision": 3 }
},
"INJECTION_CAPACITANCE": {
  "INJ_CAPACITANCE": { "sel": [6.0, 9.0], "precision": 2 }
},
```

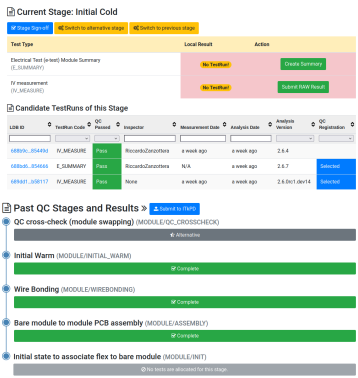
Local Database (LDB)



LocalDB top page with a list of functions



Searchable list of components



Display of past stages and results

- LocalDB consists of a local mongoDB and a custom viewer with a user-friendly and colourful GUI
- Automatically run analysis upon uploading measurement output and displays analysis results
- Local or cluster-wide file browser with customisations (e.g. defining site-specific stages/tests)
- Imports other `mq*t` to generate config, run analysis and compile module summary reports to sign off a stage