VERTEX 2025 : 33rd International Workshop on Vertex Detectors

Performance of the AstroPix Prototype Module for the Barrel Imaging Calorimeter at the ePIC Detector and in Space-Based Payloads

Bobae Kim (bobae.kim@anl.gov)

Argonne National Laboratory

for the ePIC Collaboration
on behalf of AstroPix team

U.S. DEPARTMENT of ENERGY

Argonne National Laboratory is a U.S. Department of Energy laboratory managed by UChicago Argonne, LLC.

Argonne NATIONAL LABORATORY

Contents

- Introduction
  - AstroPix
  - NASA space mission
  - Barrel Imaging Calorimeter at ePIC detector
    - Structure of Imaging Layer with AstroPix in BIC
- Test Setup
- Performance Test Results
  - v3 Single Chip
  - v3 Quad Chip
  - Three-layer of v3 Quad Chips: A-STEP prototype for space-based payload
  - 9-chip PCB prototype module: The smallest unit of imaging layer
- Summary & Plan

Overview of AstroPix

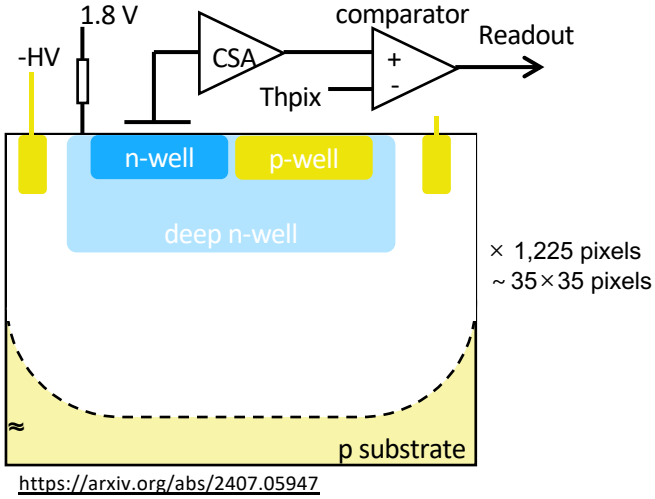
High-voltage CMOS monolithic active pixel sensor (HV-CMOS MAPS)

- Developed based on the experience from ATLASpix and MuPix since 2019 [arXiv:2109.13409]

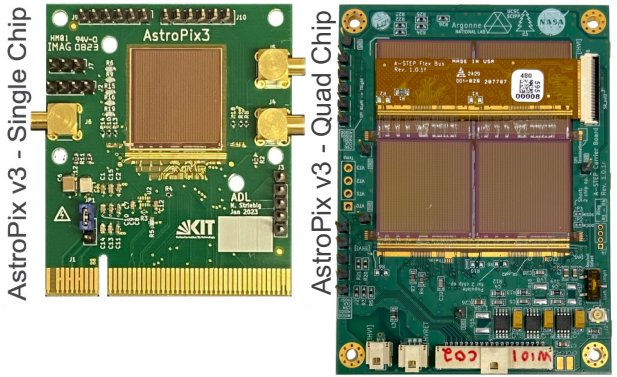
- For space-based missions, specifically for gamma-ray astrophysics
- Use as the imaging layers in the barrel imaging calorimeter for nuclear physics applications.

- Charge collection/signal processing
  (Charge Sensitive Amplifier → Comparator for ToT) on each pixel
  →low noise and low power consumption!

- AstroPix v3 chips
  - 2×2 cm² -size with 35 × 35 pixel matrix
  - 500 µm pixel pitch, 500 µm thickness
  - Time stamp clock: 8-bit at 2.5 MHz (400 ns)
  - Time-over-Threshold clock: 12-bit at 200 MHz (5 ns)
  - Streaming readout



https://arxiv.org/abs/2407.05947



Argonne NATIONAL LABORATORY

Overview of Space-based Mission in NASA

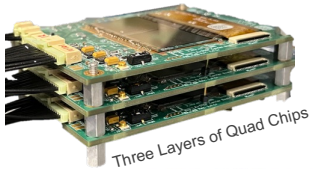
Space-based missions, specifically for gamma-ray astrophysics

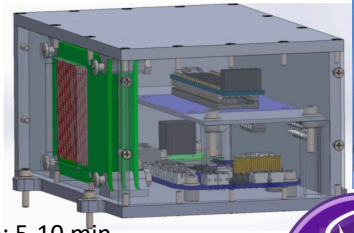
Future space-based application

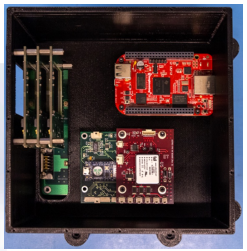
(End of March 2026)

A-STEP: **A**stroPix **S**ounding rocket **T**echnology d**E**monstration **P**ayload

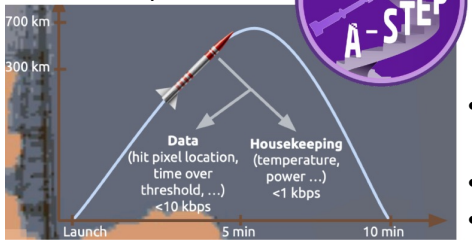
- Validate the AstroPix quad-chip design by tracking cosmic rays in a relevant space-like environment.



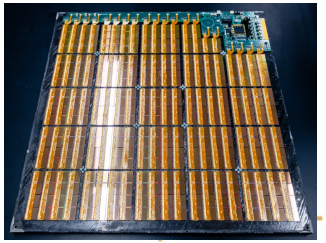


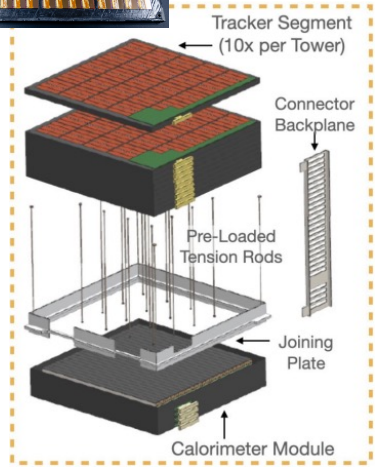


- Flight duration: 5-10 min
- Expect 1 Hz/cm^2 cosmic rays



ComPair-2 balloon mission

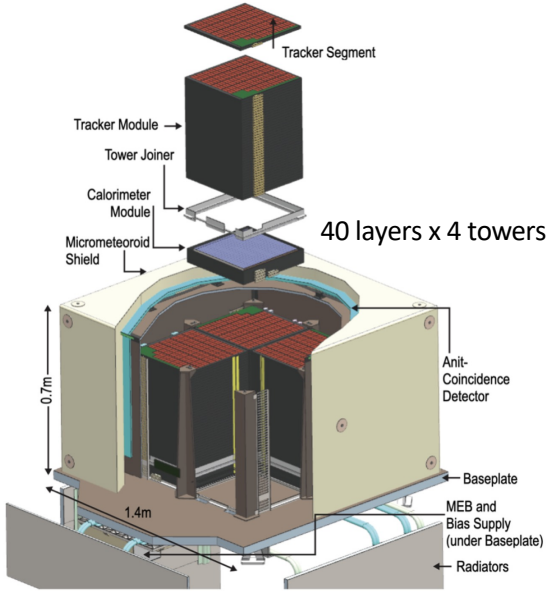




AMEGO-X detector

arXiv:2208.04990 [astro-ph.IM]

a next generation MeV γ-ray observatory

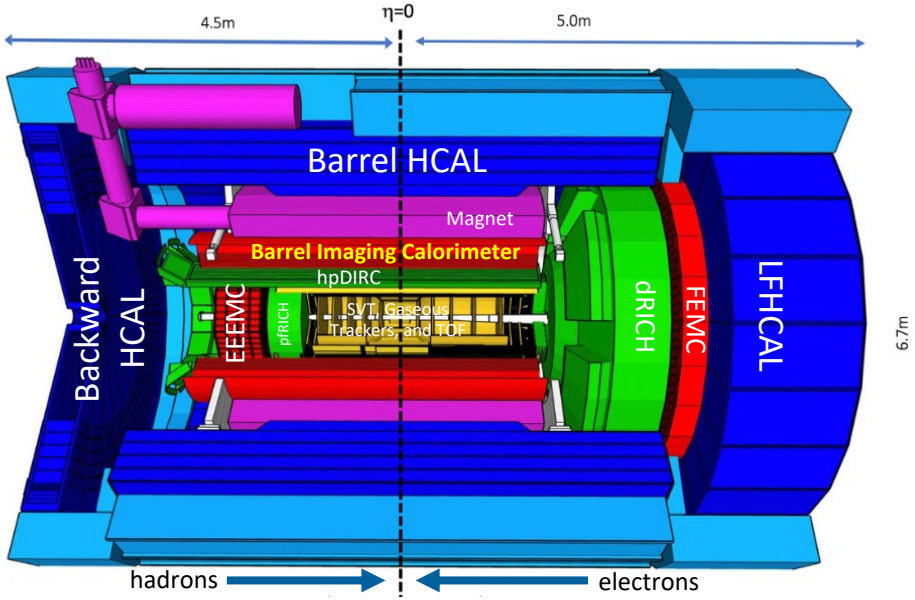


- Flight-like AMEGO-X Tracker tray: validating AMEGO-X requirements
  - 95 Quad Chips per layer
- Planning to fly 10 layers on balloon flight in ~ 4 years
- 2 prototype trays built at ANL and environmentally tested in NASA GSFC

U.S. DEPARTMENT of ENERGY

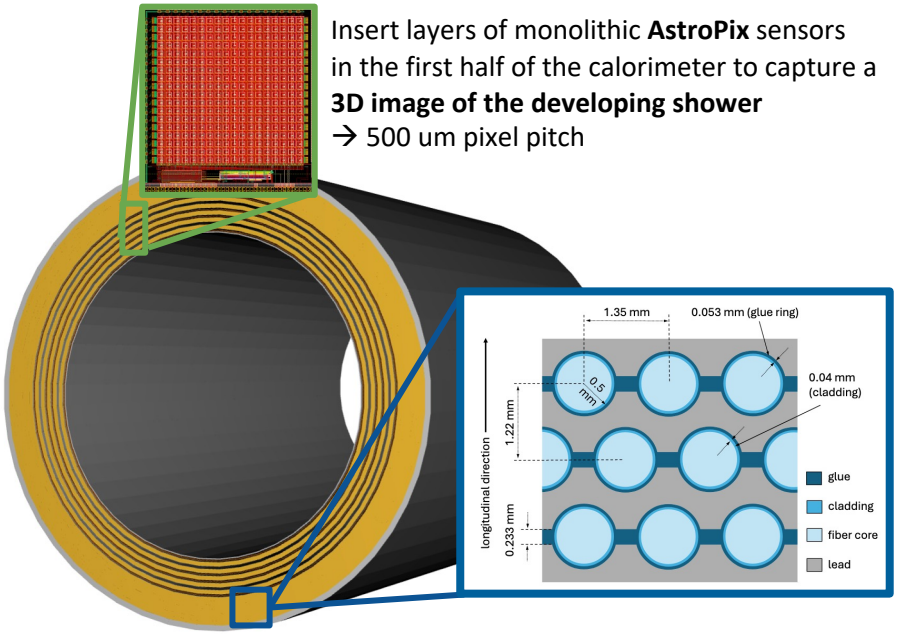
Argonne NATIONAL LABORATORY

Overview of Barrel Imaging Calorimeter at ePIC detector



- Requirements for Barrel EM Calorimeter [Yellow Paper]
  - Energy resolution < **10%/√(E) + (2-3)%**
  - **Photon measurements** in energies of 100 MeV – 50 GeV
  - **Electron ID** up to 50 GeV and down to 1 GeV and below
  - **e/π separation** for energies of 1 GeV – 50 GeV
  - **γ/π^0 separation** up to 10 GeV
  - Sufficient dynamic range to **detect MIP** signals

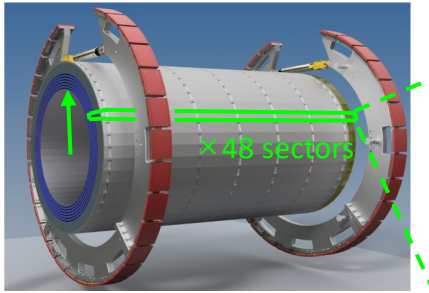
Combination of a high-performance sampling calorimeter with inexpensive silicon sensors for shower profiling



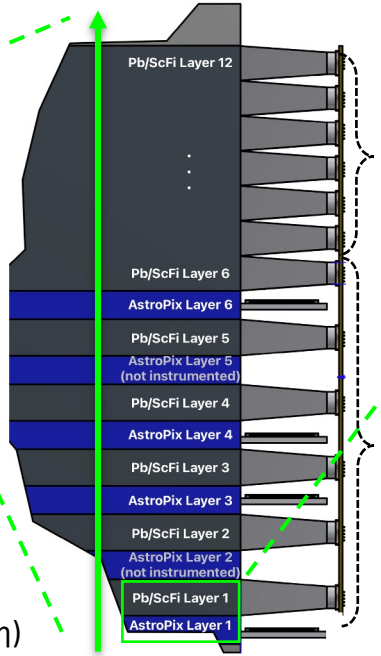
Insert layers of monolithic **AstroPix** sensors in the first half of the calorimeter to capture a **3D image of the developing shower**
→ 500 um pixel pitch

Pb/SciFi sampling calorimeter with two-sided SiPM readout
→ 1.1cm/√E position resolution in z-direction [NIMA 596 (2008) 327]
→ Energy resolution at GlueX: σ = 5.2% /√E ⊕ 3.6% [NIMA 896 (2018) 24]
→ Meet the energy resolution requirement [2025 JINST 20 P07028]

Structure of Imaging Layer with AstroPix in BIC



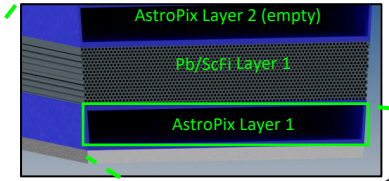
BIC Detector Geometry
Active Length: 435 cm
Inner Radius: 82 cm
Structure: 48 trapezoidal sectors
Weight: 42.5 US Tons
η Range: -1.71 < η < 1.31
Sector thickness: ~40cm
Total thickness > 17.1 X_0 (depending on η)

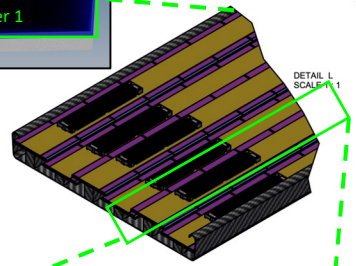


Large **back section of Pb/SciFi**

4 imaging layers with AstroPix interleaved with **5 Pb/SciFi layers**

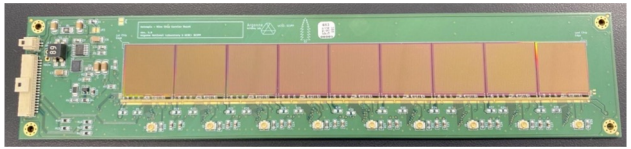
Astropix Layer + Pb/SciFi Layer





Tray
Structure holding the AstroPix staves for a single layer (217.5 cm long). Consists of 6-7 staves.

Stave
Consists of 12 modules.



AstroPix 9-chip Module
9 AstroPix sensors
daisy-chained together on PCB.

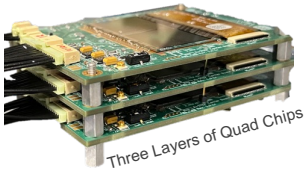
- 4 imaging layers in a Sector =Total 31,104 modules = Total 279,936 AstroPix chips
- All Trays will be built using same modules, standardizing the loading procedure
- **The first prototype module, built with v3 sensors for initial testing.**
  → v5 will be used for 9-chip module after fabrication is complete.

Test Setup

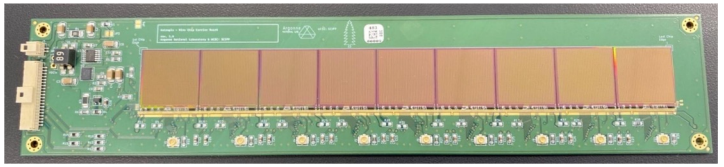
- 1x1

- 2x2

- (2x2)x3



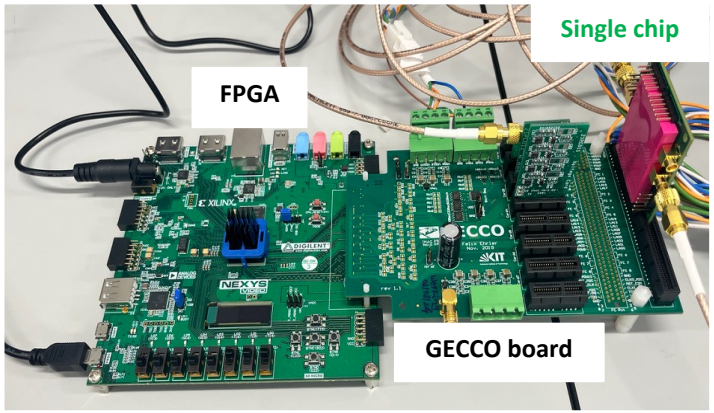
- 1x9

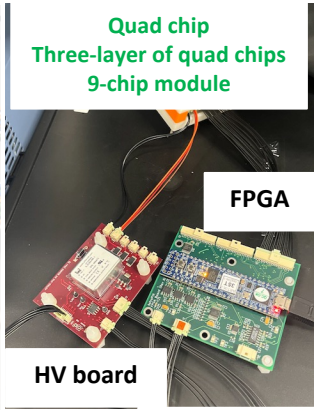


9-chip daisy-chained Prototype Module

- (1x9)x3

Two testing setups for AstroPix





Bench test

- Noise scan (w.r.t thresholds)
  - → Masking noisy pixels
- Injection test
  - → ToT response vs injection voltages
- Radiation source test
  - → Calibration curve each pixel
  - → w. Sr-90: Validation of configuration

Beam test

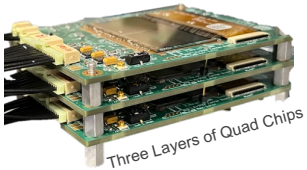
- 120 GeV Proton beam @FNAL (June.2024)
  - → MIP response
  - → Depletion depth

Test Setup

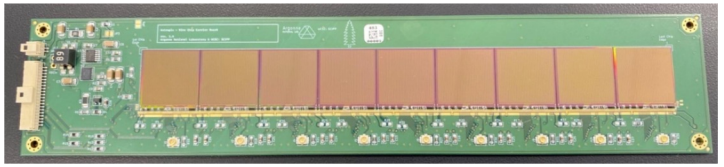
- 1x1

- 2x2

- (2x2)x3



- 1x9



9-chip daisy-chained Prototype Module

- (1x9)x3

Test Results

	Single chip	Quad chip	Three layer of Quad-chips	9-chip Module	Three layer of 9-chip Module
Noise scan	✅	✅		✅	On-going
Injection test	✅	✅		✅	
Source test	✅	✅	✅	✅	
Beam test	✅ (2024)				

*FNAL didn't provide beam in 2025.

Bench test

- Noise scan (w.r.t thresholds)
  → Masking noisy pixels
- Injection test
  → ToT response vs injection voltages
- Radiation source test
  → Calibration curve each pixel
  → w. Sr-90: Validation of configuration

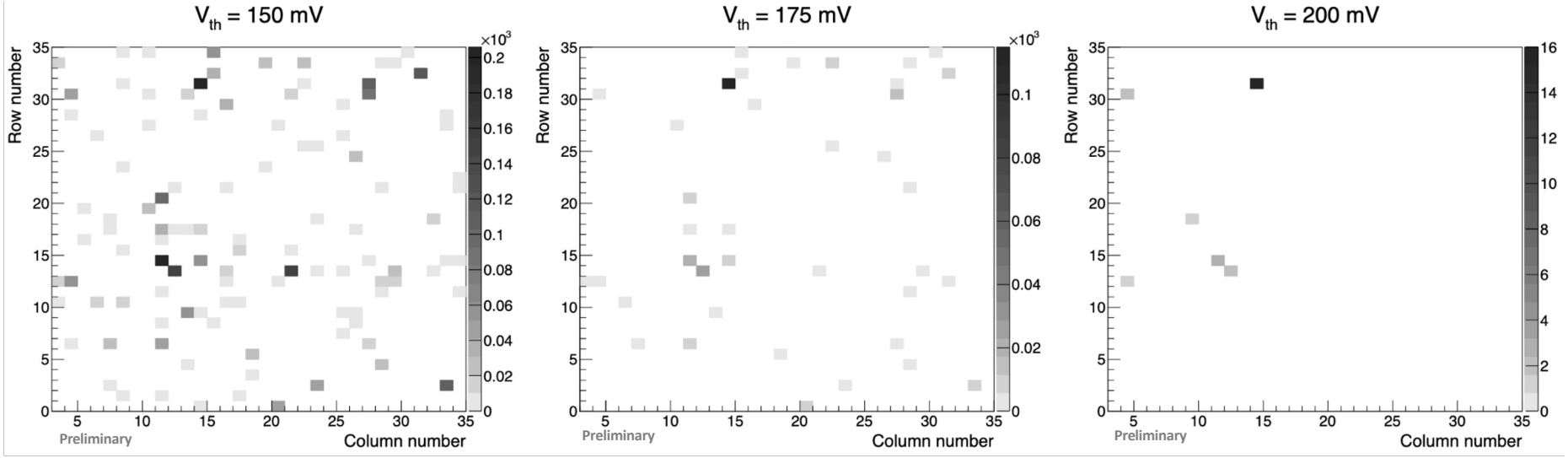
Beam test

- 120 GeV Proton beam @FNAL (June.2024)
  → MIP response
  → Depletion depth

v3 Single Chip: Performance Test Results (1)

Bench Test: Noise Study

- Determine the percentage of pixels which are sensitive to the dynamic range and record intrinsic noise rates lower than the set threshold (plots below show 5s of data taking)
- The AstroPix dynamic range floor (25 keV) allows for threshold values of more than 200 mV above baseline.
- < 0.5% of pixels (1 pixel/array) have a noise rate > 2 Hz for data collection and are masked
- **Fulfills BIC/AMEGO-X requirements on low energy threshold (25 keV tested in simulations), and yield of masked pixels.**



- Active pixels: 96.2%
- 43/1,120 pixels disabled

- Active pixels: 99.5%
- 6/1,120 pixels disabled

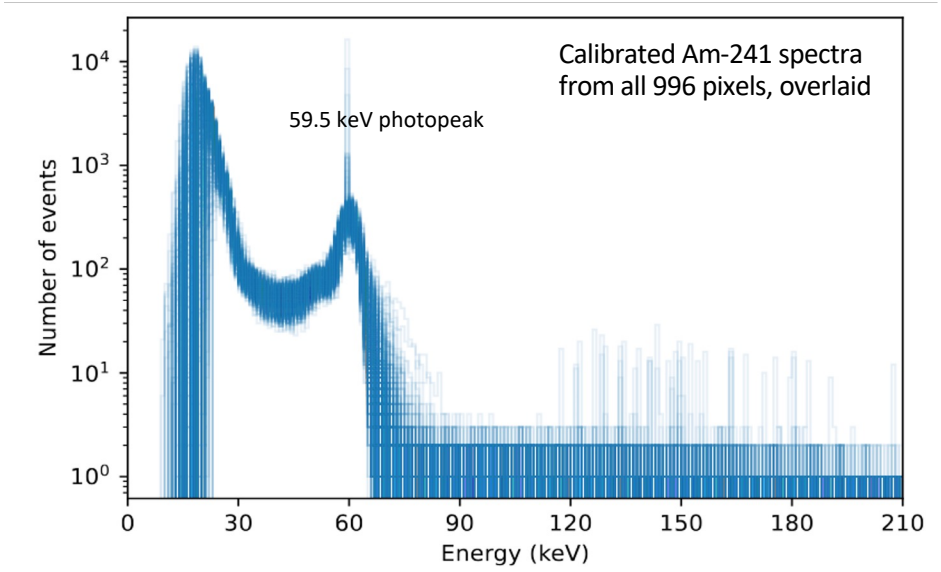
- Active pixels: 99.9%
- 1/1,120 pixels disabled

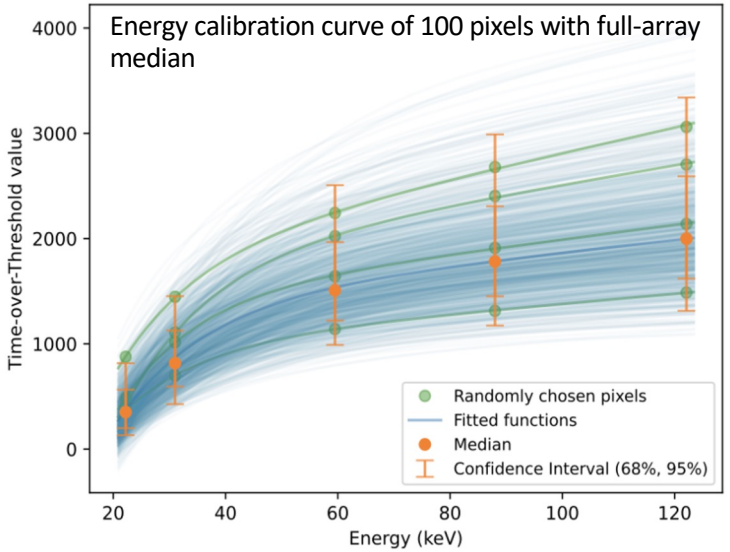
v3 Single Chip: Performance Test Results (2)

Plots by Hiroshima University, Japan
NIMA 1068 (2024) 169762

Bench Test: Radiation Source Test

- Energy resolution/calibration: Cd-109, Ba-133, Am-241, and Co-57; from 22.2 keV to 122 keV
- Dynamic range: 25-200 keV (v5 will test 25-700 keV dynamic range, required for BIC/AMEGO-X)
- **44% of pixels meet the energy resolution requirement of 10% at 59.5 keV** with a median full-width half-maximum of 6.2 keV (10.4%).
- **92.4% of pixels achieve the low-energy floor requirement** of 25 keV sensitivity, required for BIC/AMEGO-X.

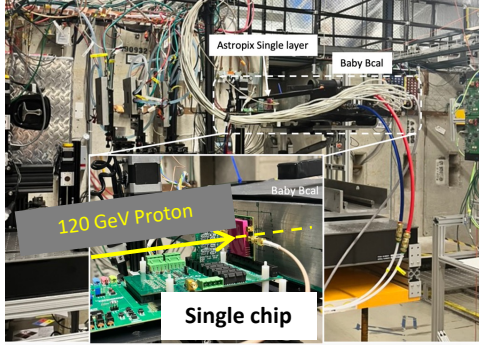


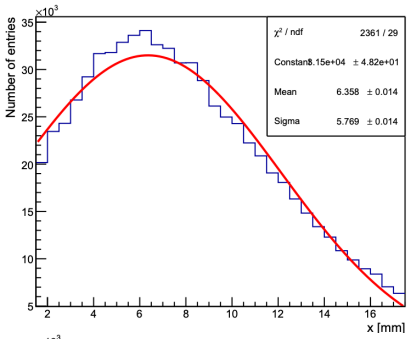


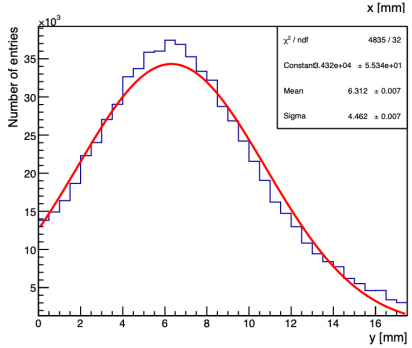
v3 Single Chip: Performance Test Results (3)

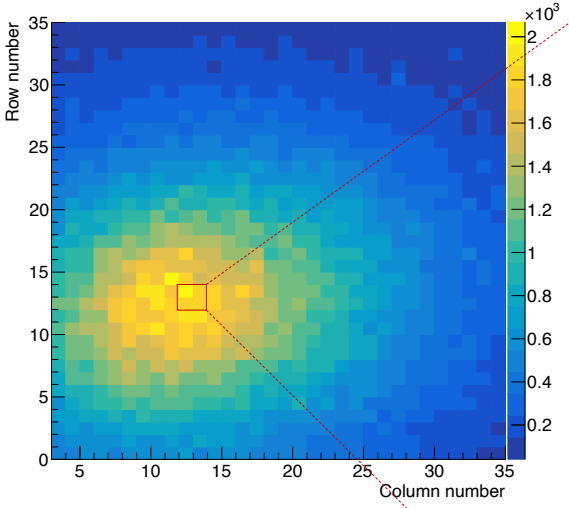
Beam Test: 120 GeV Proton Beam

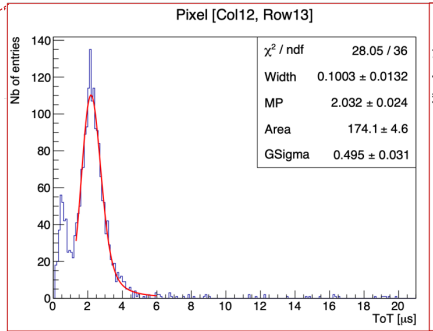
- The hit map reveals the proton beam profile: $\sigma_x \times \sigma_y = 5.8\ \text{mm} \times 4.5\ \text{mm}$
- ToT Histograms with MIP response → Fit with Landau convoluted with gaussian function

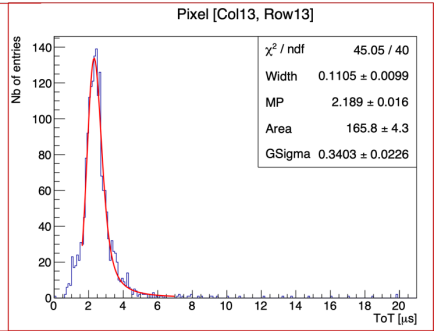


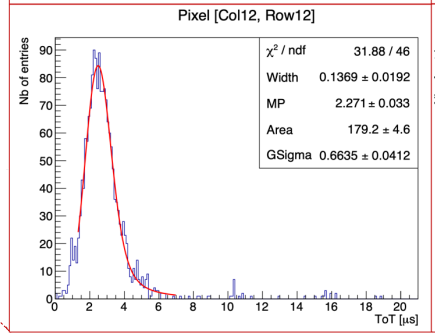


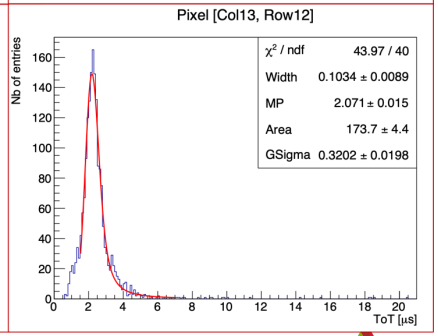












v3 Single Chip: Performance Test Results (4)

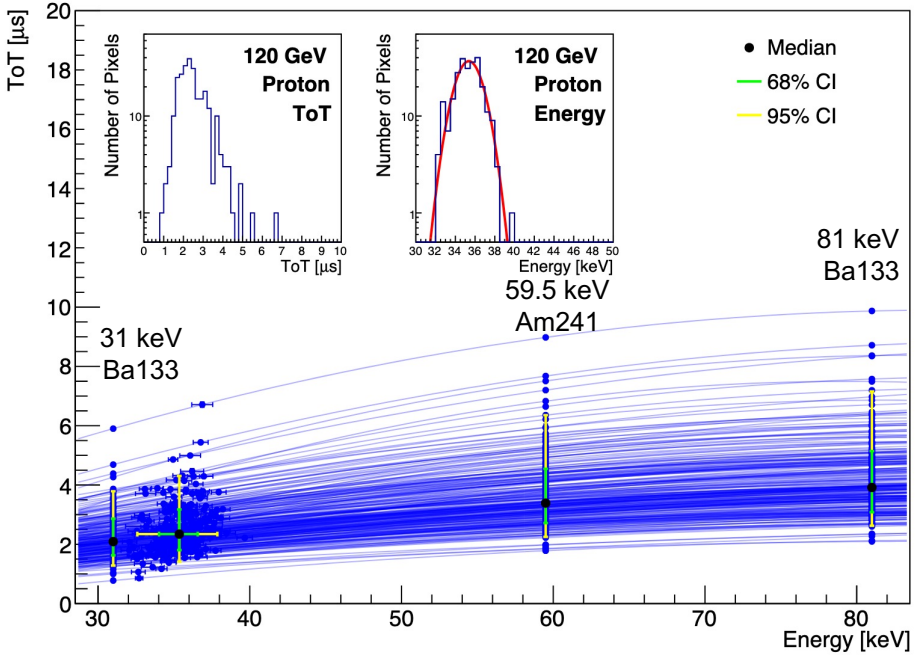
Beam Test: 120 GeV Proton Beam

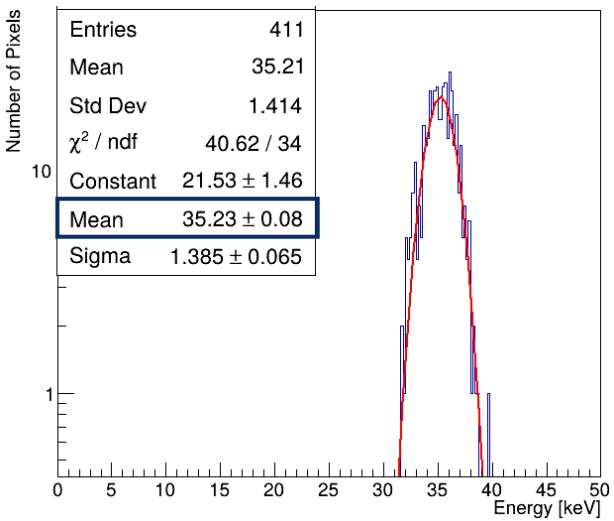
- Calibration curve as a function of energies for selected pixels
- First 120 GeV proton response: 35.23 keV for MIP sits well within dynamic range (25 keV - 200 keV) in AstroPix v3.

→ The corresponding depletion depth: $132.4\ ^{+4.8}_{-4.9}$ um

- Behaves well in the particle rates of 13 kHz

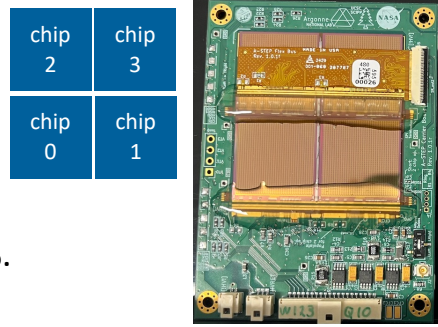
*Paper Publication in preparation





Measured energy of 120 GeV proton = **35.23 keV**

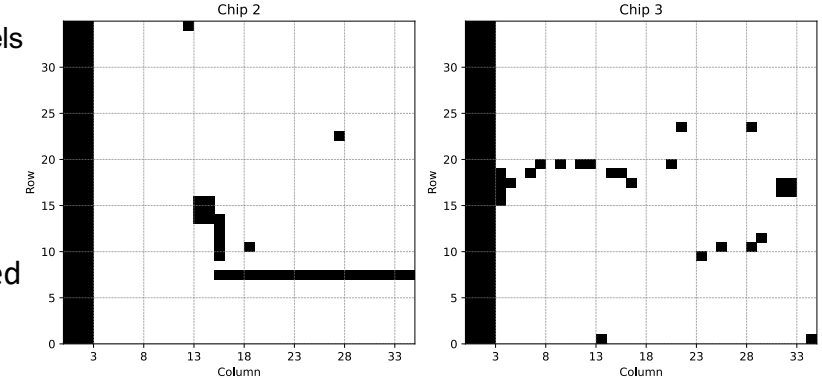
v3 Quad chip: Performance Test Results (1)



Bench Test: Noise scan

- Three column masked due to difference comparator for R&D purpose
- Pixels with noise rate > 2 Hz were masked, resulting in an active pixel yield of ≥ 97%.

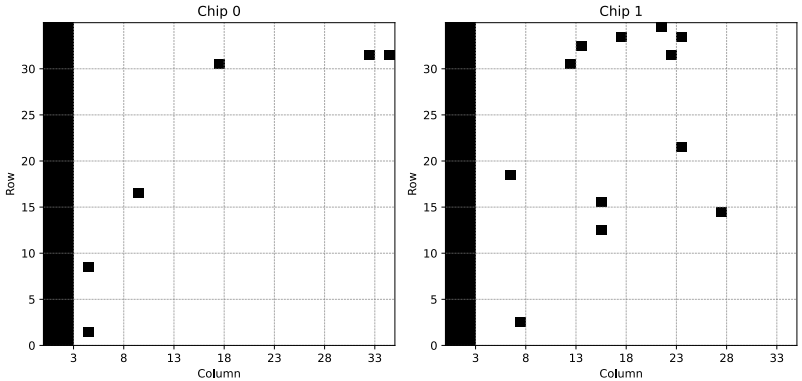
Black=Masked pixels



Active pixels: 97.0%
34/1,120 pixels disabled

*Chip 2 and Chip 3 have lower active pixel yield due to the special quad-chip structure (bus bar).

Active pixels: 97.7%
26/1,120 pixels disabled



Active pixels: 99.5%
6/1,120 pixels disabled

Active pixels: 98.9%
12/1,120 pixels disabled

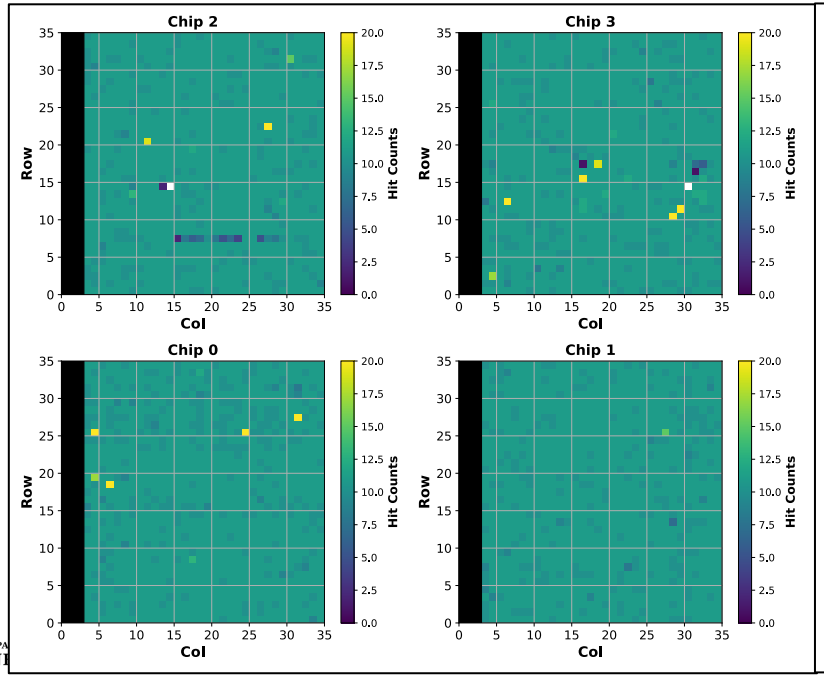
v3 Quad chip: Performance Test Results (2)

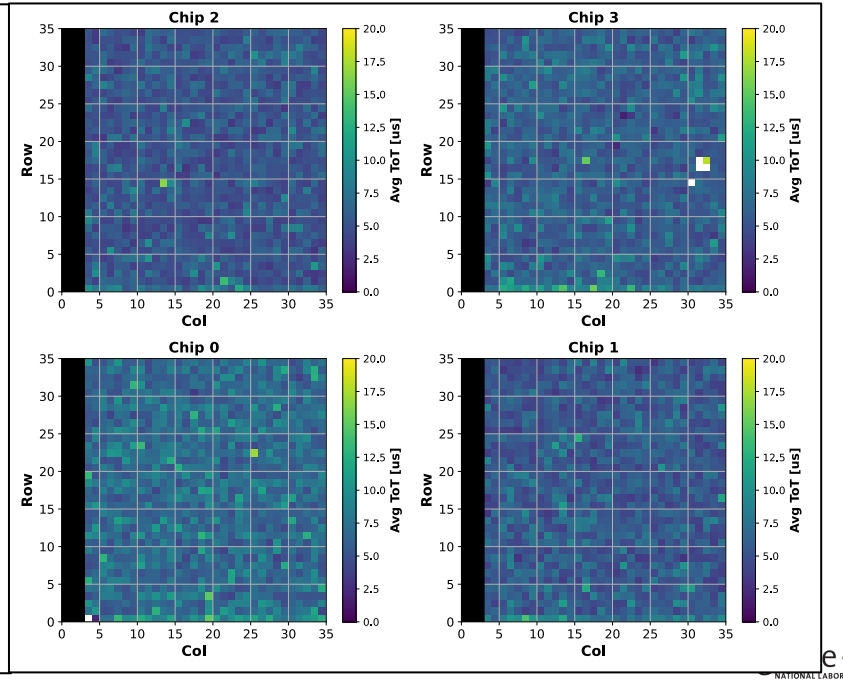
chip 2	chip 3
chip 0	chip 1

Bench Test: Injection scan

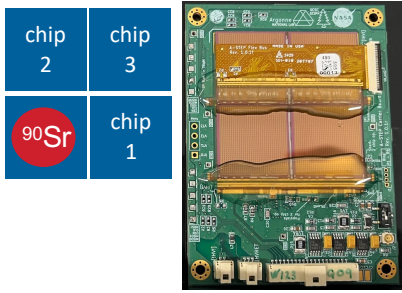
- Goal: Verify pixel response uniformity using the same injection voltage, evaluated via hit maps and ToT maps.
- Hit maps: Expected total 10-11 counts per pixel
- ToT maps: Most pixels have mean ToT values generally in the range of 5–7 µs.

  → both uniformity and pixel-to-pixel variation.



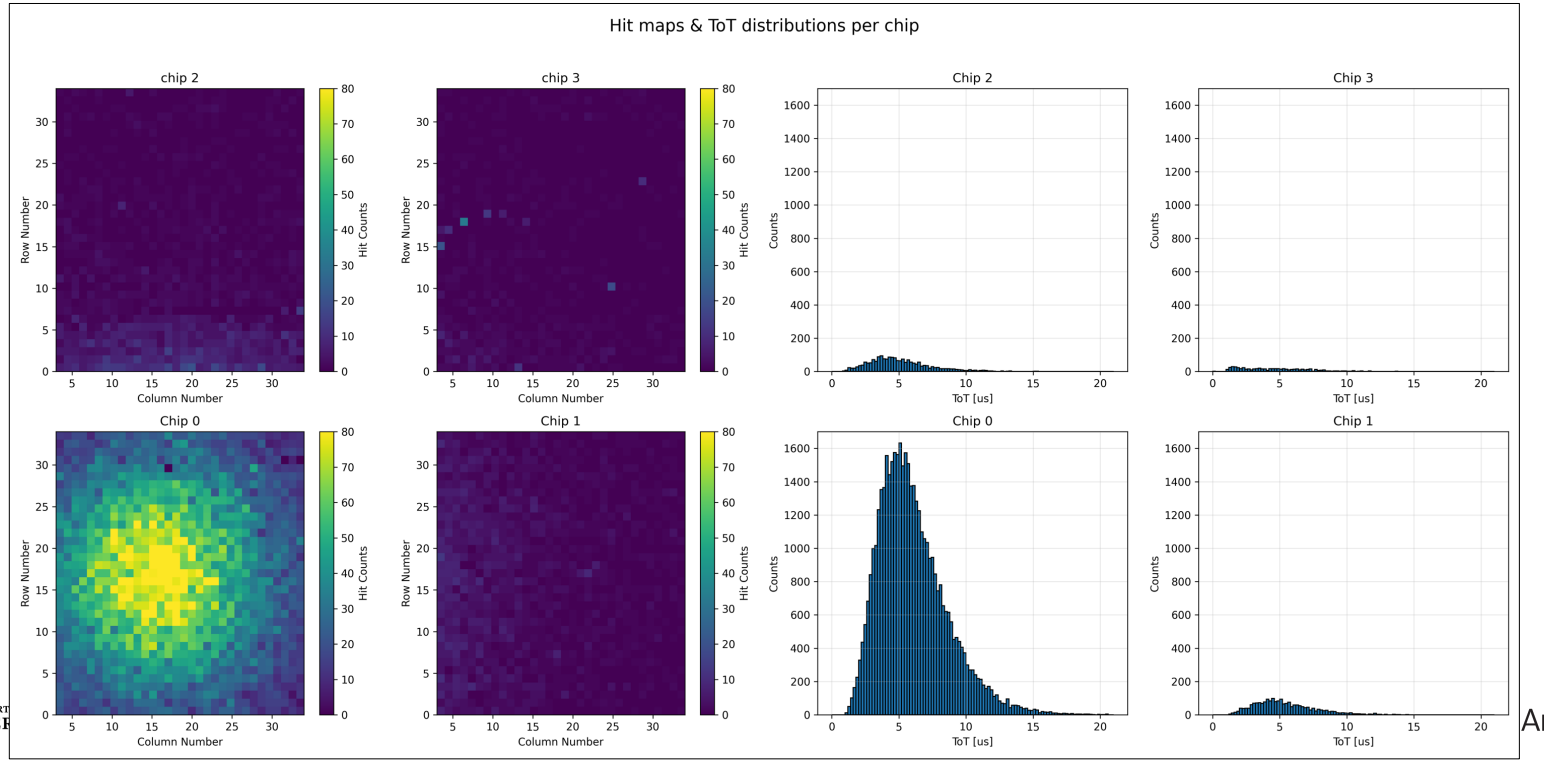


v3 Quad chip: Performance Test Results (3)



Bench Test: Source test with Sr90

- Goal: Verify source response using Sr-90, evaluated via hit maps and ToT maps.
- The hit map aligns well with the source position.
- The ToT distribution is well-described by a Landau convoluted with a Gaussian function.

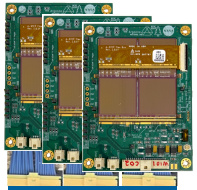


Three v3 Quad chips: Performance Test Results

Bench Test: Cosmic test using three layers of quad-chips

- Goal: verify that the software and firmware under development operate properly
- Display of a representative event where all three layers share the same timestamp
  - 1 Time Stamp = 400 ns

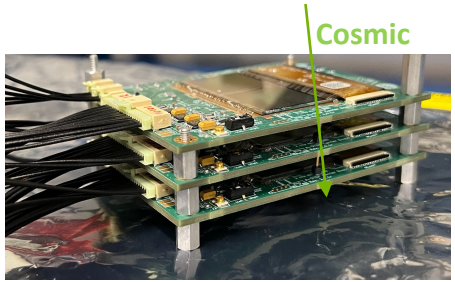
→ Validated the capability to read data from all quad chips. (up to 12 chips)

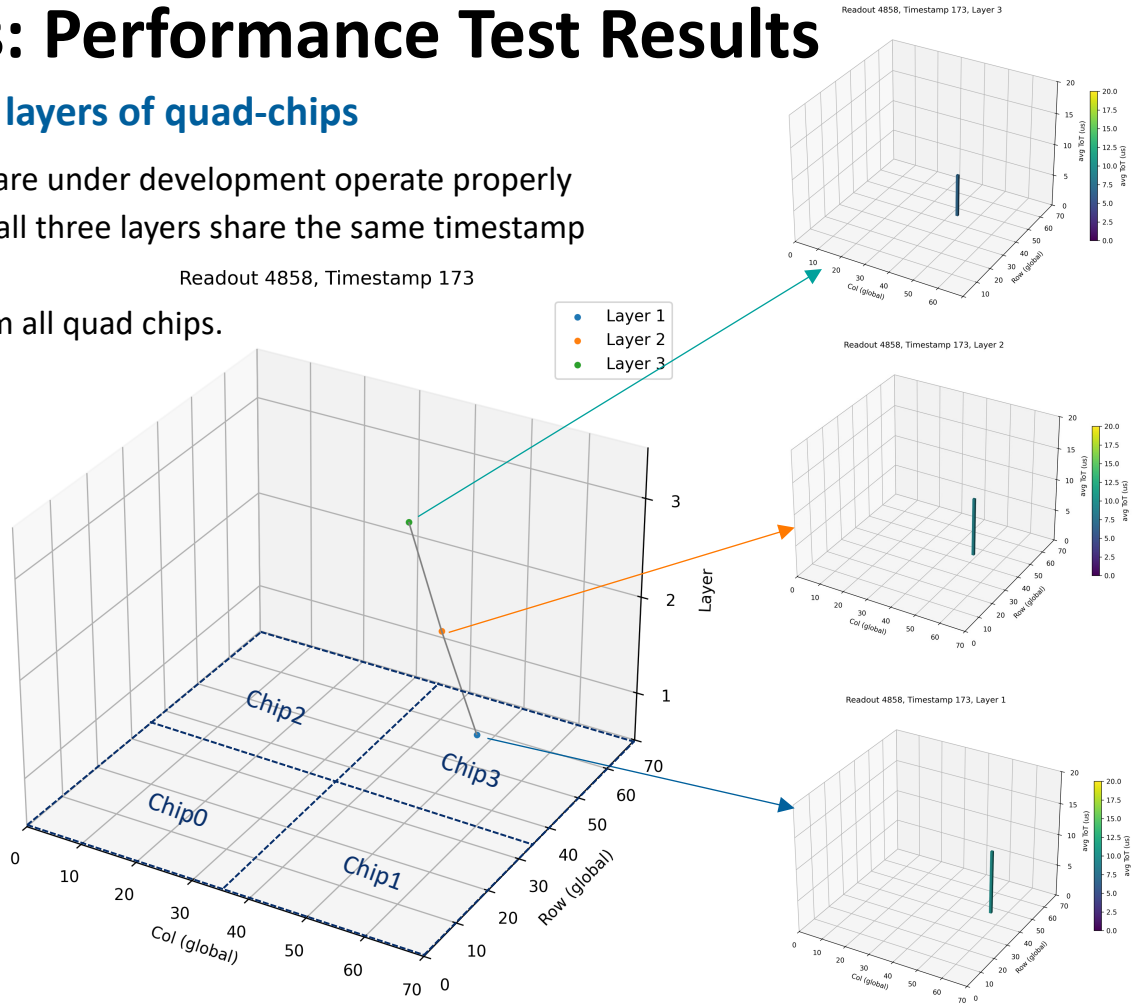


ASTEP-HW

FPGA

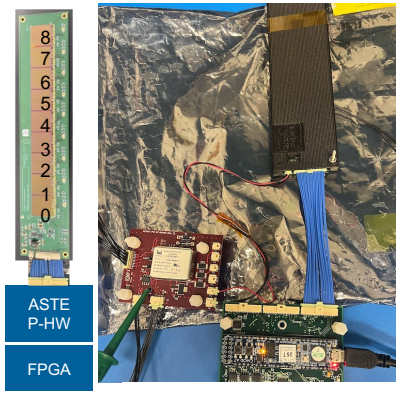
PC

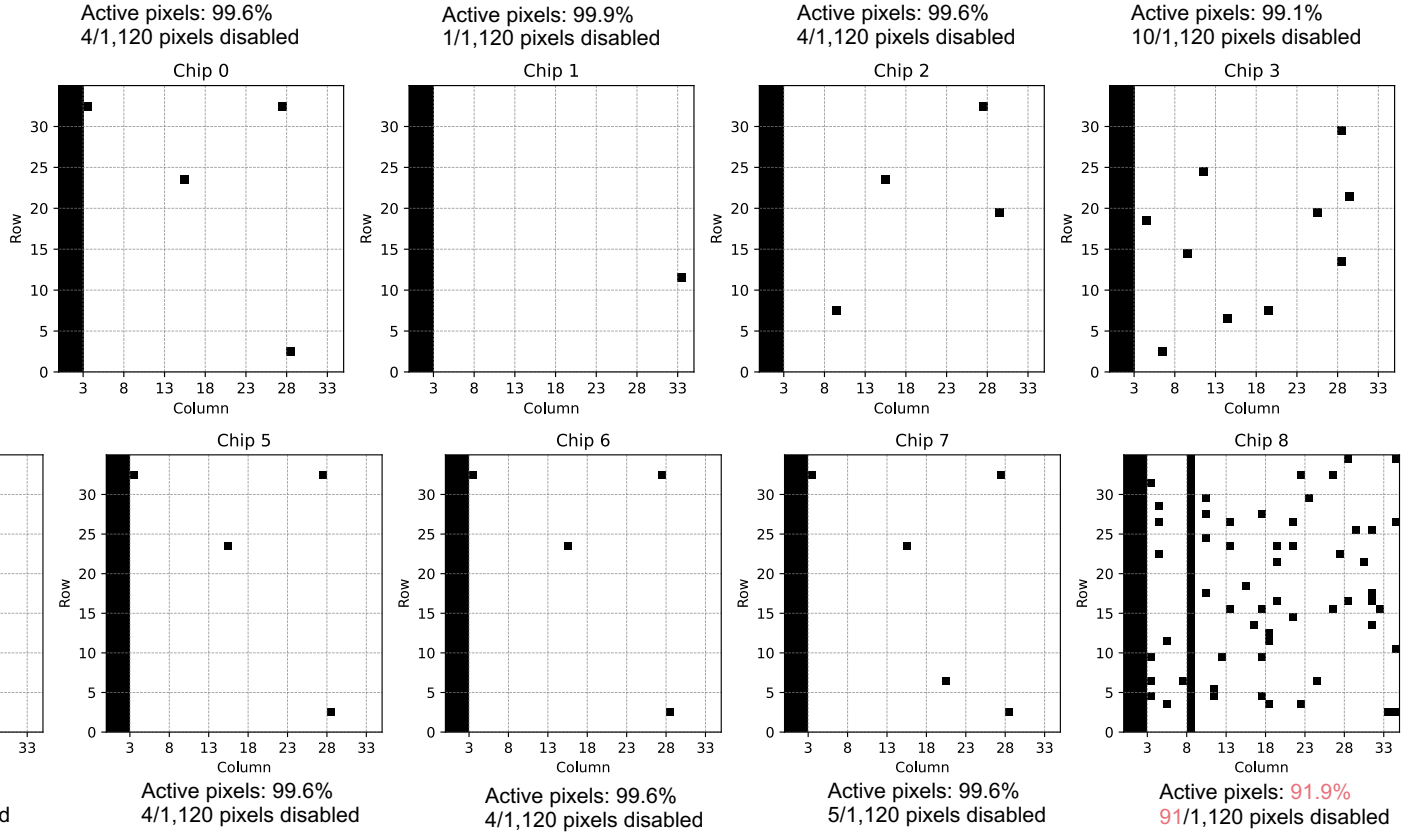




9-chip prototype module: Performance Test Results (1)

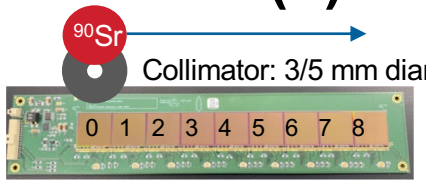
- ✅ Initial functionality confirmed – power stable and DAQ communication OK.
- ✅ Noise scan: Pixels with noise rate ≥ 1 Hz were masked and 99% active pixel yield for all chips (except chip 8: 91.9%)



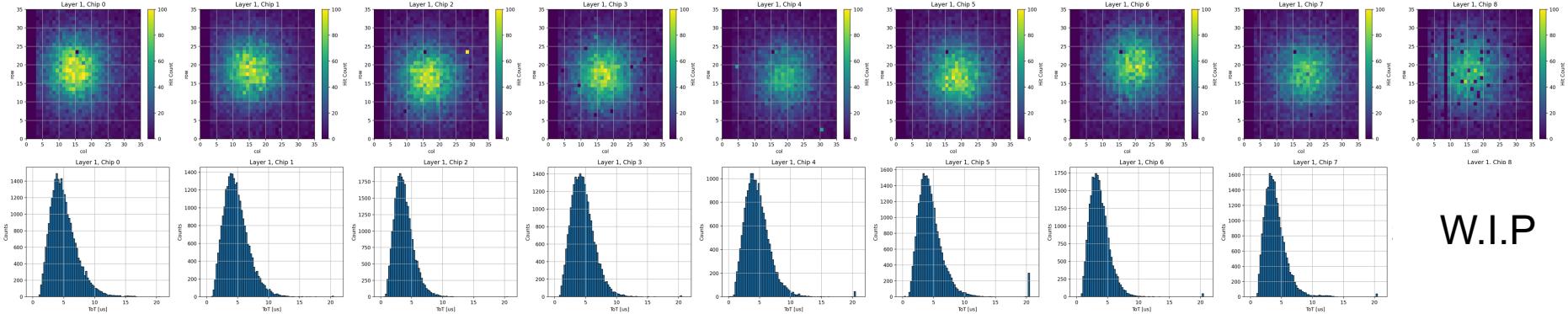


9-chip prototype module: Performance Test Results (2)

- Source test with 10 µCi Sr90: Source moved to the next chip every 1 minute
  - Results consistent with v3 single-chip performance, confirming proper operation

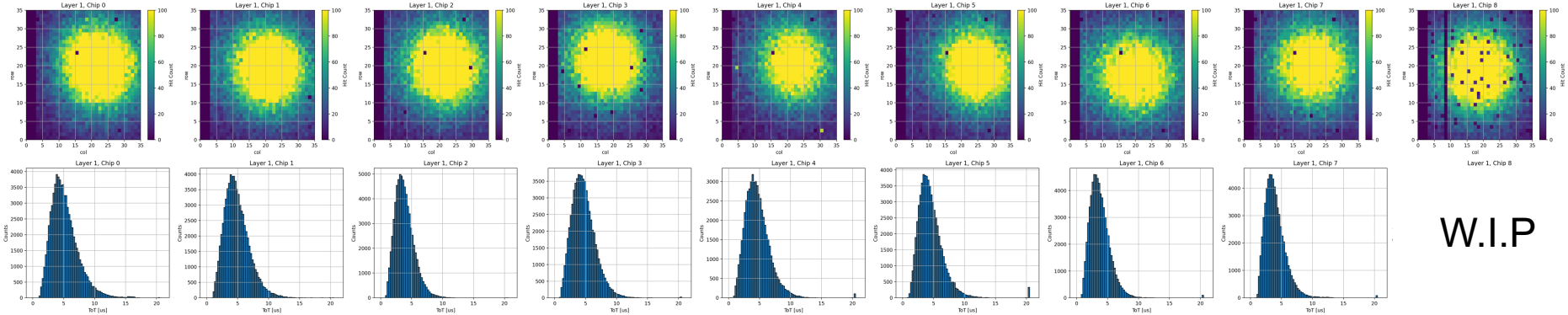


- 3-mm-diameter collimator



W.I.P

- 5-mm-diameter collimator

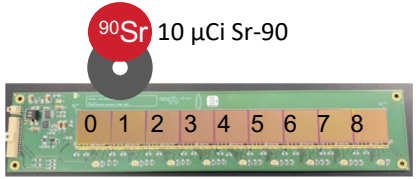


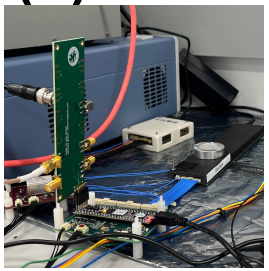
W.I.P

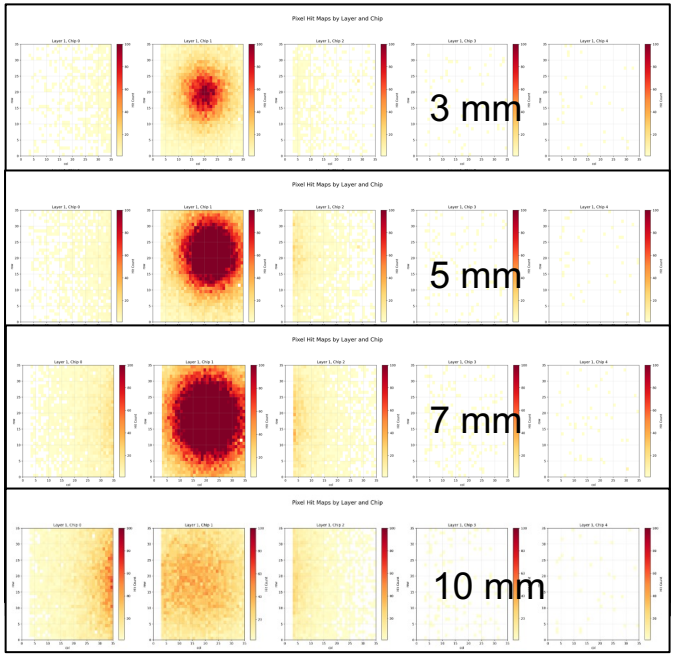
9-chip prototype module: Performance Test Results (3)

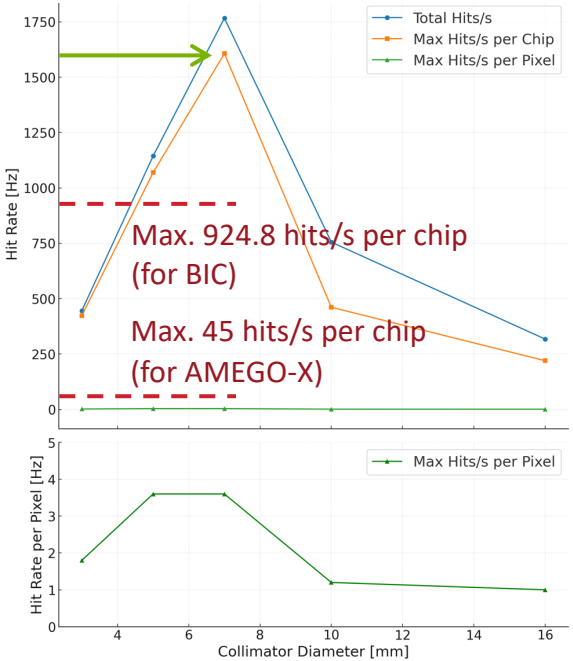
- Goal: Validate the capability to read out data from the 9-chip module with the current setup
- Maximum hit rate achievable with the current SW/FW:
  - **Per 9 chips:** 1,766.5 Hz
  - **Per chip:** 1,606.9 Hz
  - **Per pixel:** 3.6 Hz

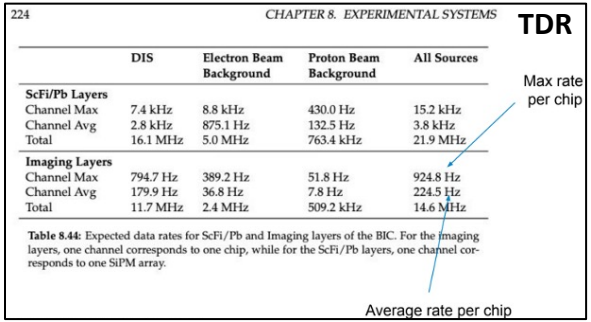
  → Meet estimated hits rates for BIC and space mission as well











	DIS	Electron Beam Background	Proton Beam Background	All Sources
ScFi/Pb Layers				
Channel Max	7.4 kHz	8.8 kHz	430.0 Hz	15.2 kHz
Channel Avg	2.8 kHz	875.1 Hz	132.5 Hz	3.8 kHz
Total	16.1 MHz	5.0 MHz	763.4 kHz	21.9 MHz
Imaging Layers				
Channel Max	794.7 Hz	389.2 Hz	51.8 Hz	924.8 Hz
Channel Avg	179.9 Hz	36.8 Hz	7.8 Hz	224.5 Hz
Total	11.7 MHz	2.4 MHz	509.2 kHz	14.6 MHz

Table 8.44: Expected data rates for ScFi/Pb and Imaging layers of the BIC. For the imaging layers, one channel corresponds to one chip, while for the ScFi/Pb layers, one channel corresponds to one SiPM array.

With collimators ≥ 10 mm, AstroPix reaches the **saturation limit**, where stable data-taking is no longer possible.

Argonne NATIONAL LABORATORY

Summary & Outlook

Several configurations with an increasing number of AstroPix sensors have been successfully tested:

- ✅ **Single chip** in a beam-like environment
  - First 120 GeV proton response: MIP response (35.2 keV) within dynamic range (25 keV – 200 keV)
  - depletion depth ~132 µm
- ✅ **Quad-chips** for use in space missions
- ✅ **Multi-layer quad-chips** for NASA sounding rocket mission studies
- ✅ **9-chip prototype module** for the BIC imaging layer
  - Max hit rates: 1,607 Hz (per chip) → meets BIC/space mission requirements

Outlook

- Continued development and testing of large-scale prototypes, targeting both the BIC and future space missions
- v4 chip testing is underway.
- **v5 chip** (pre-production prototype) currently in fabrication
- Module- and tray-level tests planned within the PREP sector


Argonne
NATIONAL LABORATORY

AstroPix and BIC Timeline

Not shown:
Early CD4 (Oct 2032)
CD4 (Oct 2034)

We are here

FY19 Q3 Q4 | FY20 Q1 Q2 Q3 Q4 | FY21 Q1 Q2 Q3 Q4 | FY22 Q1 Q2 Q3 Q4 | FY23 Q1 Q2 Q3 Q4 | FY24 Q1 Q2 Q3 Q4 | FY25 Q1 Q2 Q3 Q4 | FY26 Q1 Q2 Q3 Q4 | FY27 Q1 Q2 Q3 Q4 | FY28 Q1 Q2 Q3 Q4 | FY29 Q1 Q2 Q3

- AstroPix v1: Design & Fabr. | Test
- AstroPix v2: Design & Fabr. | Test
- AstroPix v3: Design & Fabr. | Test | Test
- AstroPix v4: Design & Fabr. | Test | Test
- AstroPix v5: Design & Fabr. | Test
- AstroPix v6: Design & Fabr. | AstroPix v6 (production) | Production Fab.

v3 has comprehensive test program: benchtop and testbeam, irradiation, quad-chip readout for NASA payload mission (A-STEP), integration with Pb/SciFi for ePIC (R&D studies and test article production)

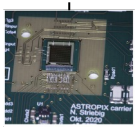
first v5 wafers used for preproduction
Start of production driven by project fund availability (estimated ~ 1 year after CD2/3)

EIC Project Milestone
New AstroPix version

ePIC BIC Timeline

- Design and generic R&D
- Final design and EIC R&D
- BIC Preproduction
- BIC Production

CD0 | CD1 | CD3a | CD3b | CD2/3 | Start of BIC installation at BNL



AstroPix v1

HV-CMOS MAPS based on ATLASPix3, designed for the AMEGO-X NASA mission, optimized for power dissipation and energy resolution
NIMA 1019 (2021) 165795

0.45 x 0.45 cm² chip, 175 µm pixel pitch
18 x 18 pixel matrix
Power dissipation 14.7 mW/cm²

AstroPix v2

1 x 1 cm² chip, 250 µm pixel pitch
35 x 35 pixel matrix
Row/column readout
Power dissipation 3.4 mW/cm²

AstroPix v3

First full-size chip

First full size design: 1.87 cm × 1.96 cm
Row/Column readout
Pixel pitch: 500 µm
Pixel matrix: 35 × 35
0.88 mW/cm² analog, 12 mW digital
2.5 MHz timestamp, 200 MHz ToT

AstroPix v4

Final design but smaller size

1 x 1 cm² chip, 500 µm pixel pitch
13 x 16 pixel matrix
Individual pixel readout
3 timestamps, 3.25 ns time resolution
TuneDAC for pixel-by-pixel thresholds

AstroPix v5
pre-production chip
1.87 x 1.9575 cm² chip, 500 µm pixel pitch
Design identical to v4 (with bug fixes)

AstroPix v6
production chip
2 x 2 cm² chip, 500 µm pixel pitch
Design identical to v5 (with bug fixes)

Argonne NATIONAL LABORATORY

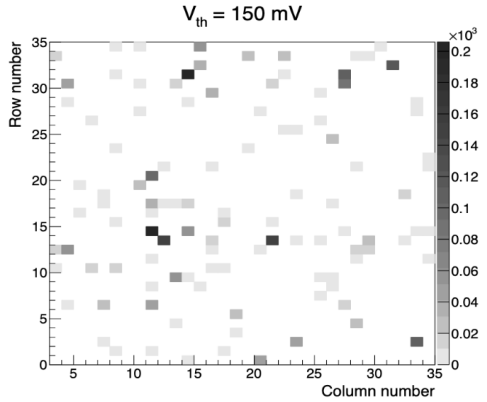
Key Performance and Parameters Metrics

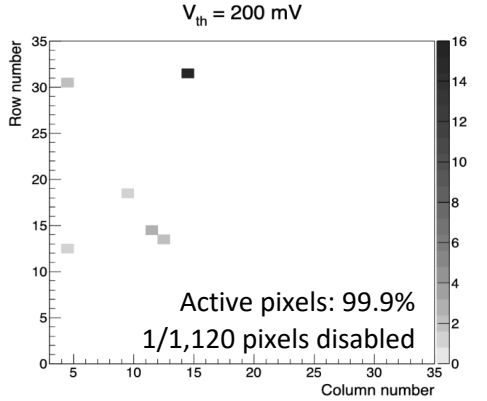
For Final Chip Version in AMEGO-X and BIC

	AstroPix for AMEGO-X requirements [arXiv:2208.04990]	BIC requirements	Status (AstroPix v3)
Pixel pitch	500 µm x 500 µm		.
Power usage	< 1.5 mW/cm^2	~ 2 mW/cm^2 in v5 acceptable	4.1 mW/cm^2
Energy resolution	< 10% (FWHM) @ 59.5 keV		.
Dynamic range	25 - 700 keV		25-200 keV
Passive material	< 5% on the active area of Si	not applicable	
Time resolution	1 us	20 ns (in v5 acceptable)	
Si Thickness	500 µm Fully depleted		~ 100 µm depleted

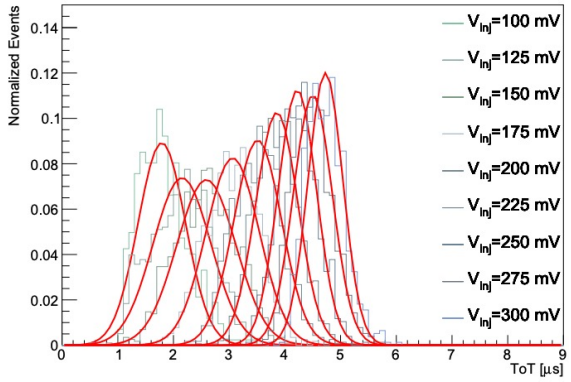
v3 Single Chip: Performance Test Results (1)

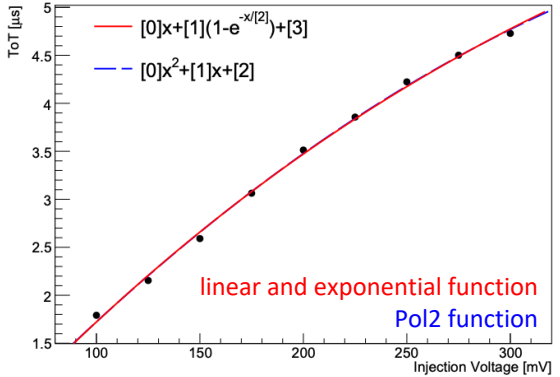
Bench Test: Noise Scan, Injection scan and source test



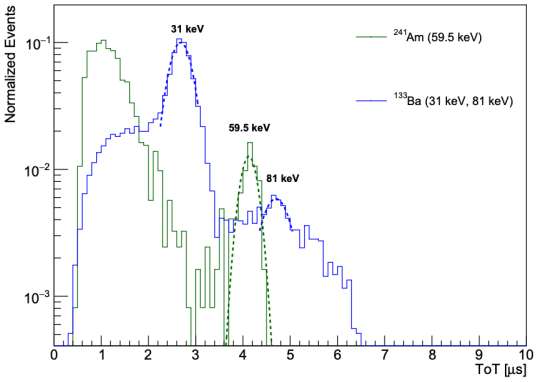


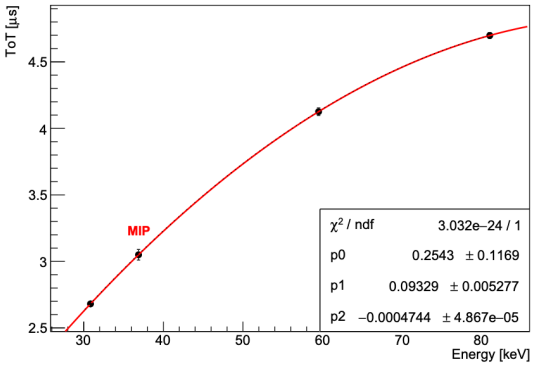
- ToT distribution and injection vol. vs ToT





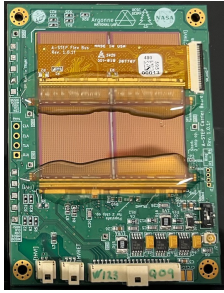
- Calibration curve (Am241 and Ba133)





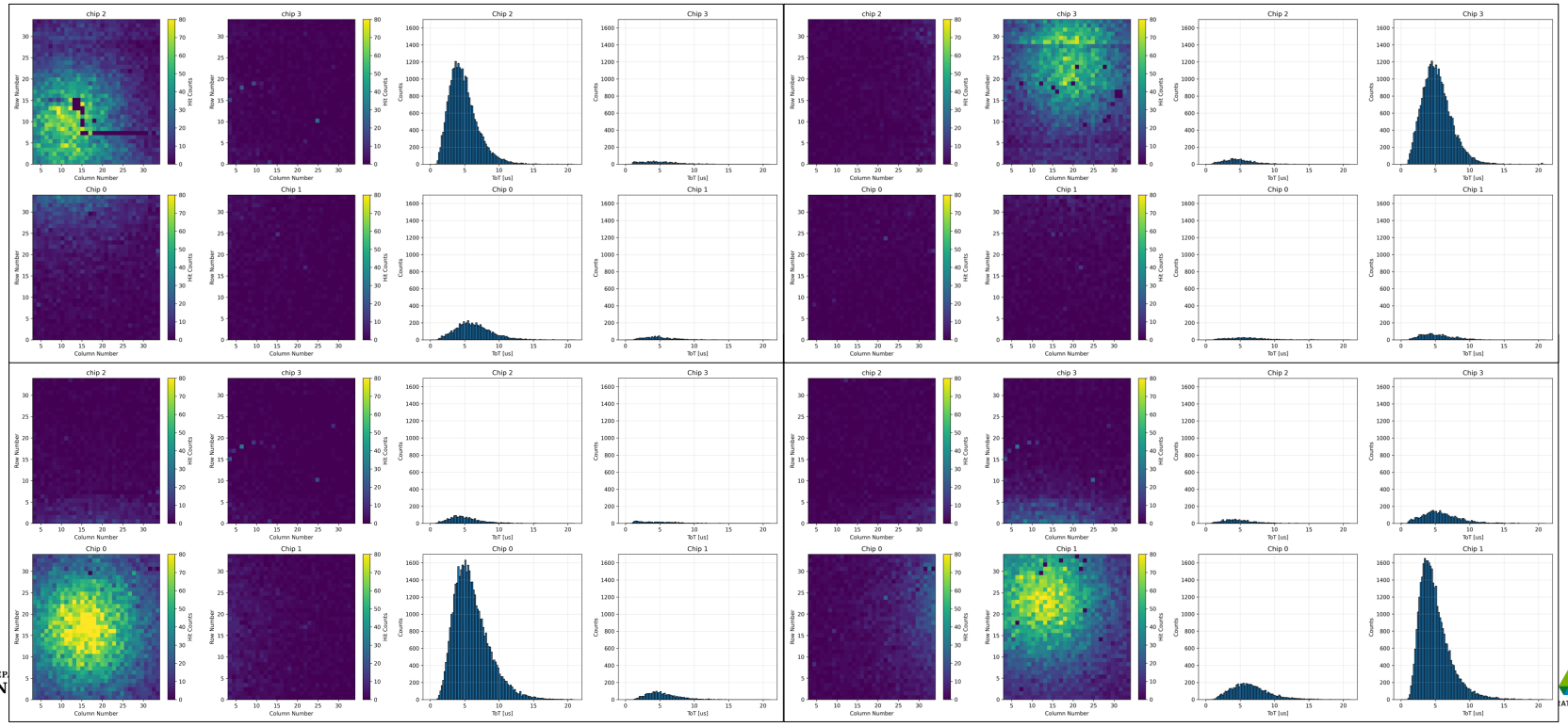
v3 Quad chip: Performance Test Results (3)

chip 2	chip 3
chip 0	chip 1

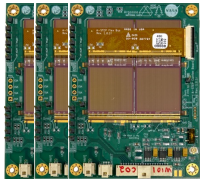


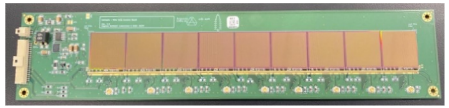
Bench Test: Source test with Sr90

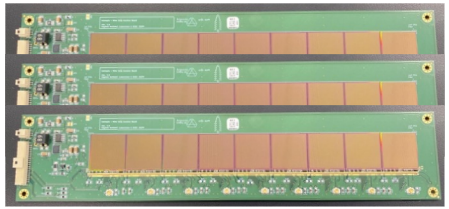
- Goal: Verify source response using Sr-90, evaluated via hit maps and ToT maps.
- The hit map aligns well with the source position.
- The ToT distribution is well-described by a Landau convoluted with a Gaussian function.



Goals of System Synchronization Testing

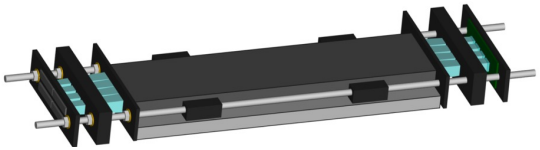




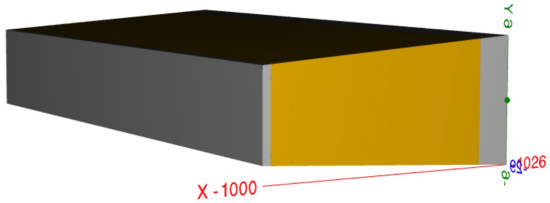


+

Pb/SciFi calorimeter



Thin Pb/SciFi layers



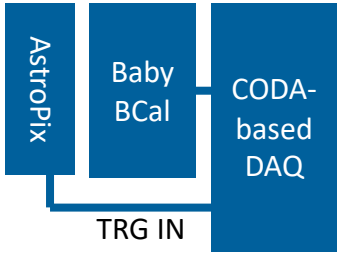
Baby BCAL

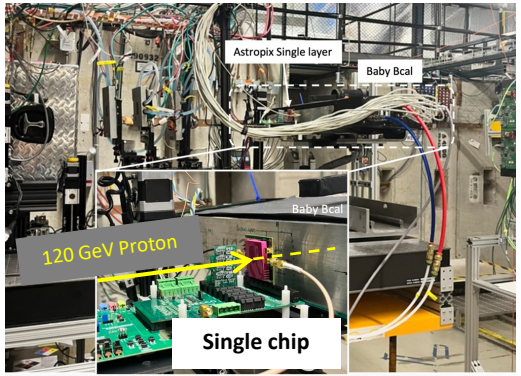
How to	AstroPix DAQ	Pb/SciFi DAQ
Analog signal of AstroPix as TriggerIN	Single chip+ GECCO+Nexys	Jlab CODA-based DAQ
MISO signal of AstroPix as TriggerIN	Single chip+ GECCO+Nexys	Jlab CODA-based DAQ
External clock for FPGA TimeStamp	Quad chip+ ASTEP+CMOD a7	HGCROC

System Testing for Integration (1) Previous test

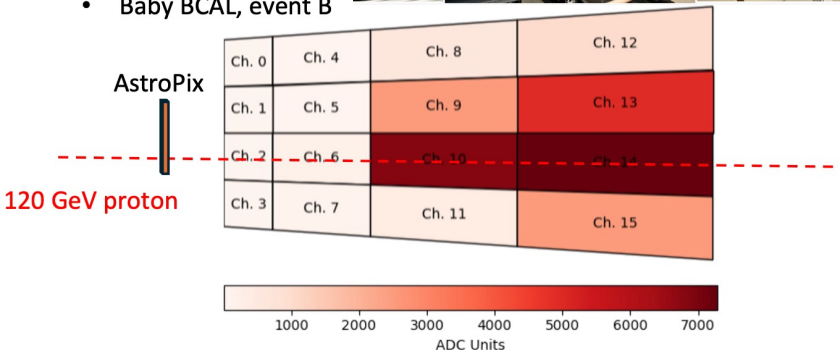
AstroPix+BabyBCAL @Beam test (June 2024)

- Baby BCAL triggered by analog signal from one pixel of AstroPix





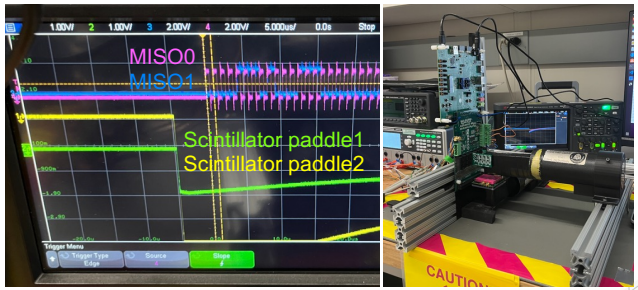
- Baby BCAL, event B

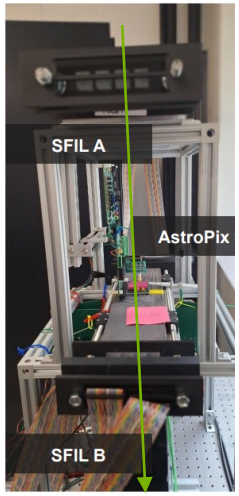


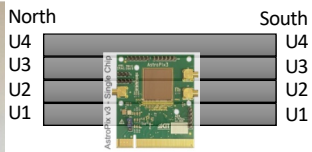
*Example plot of 120 GeV proton event display from an integrated system of Baby BCAL and a single-layer AstroPix v3 chip by Henry Klest

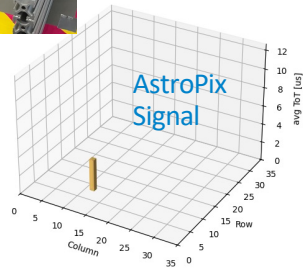
AstroPix+SFILs @Bench test

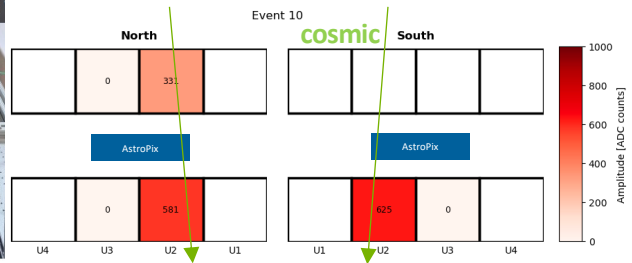
- Synchronization Plan: LVDS MISO signals that generated from AstroPix used as trigger IN for DAQ







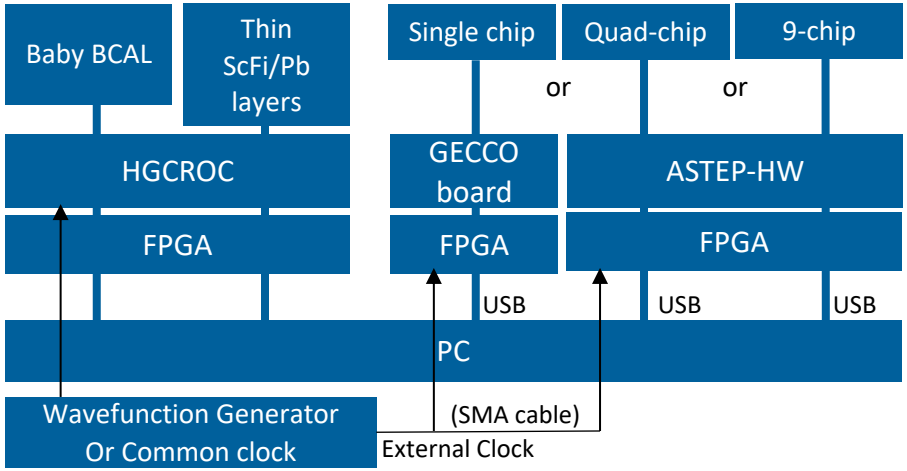




System Testing for Integration: Current status

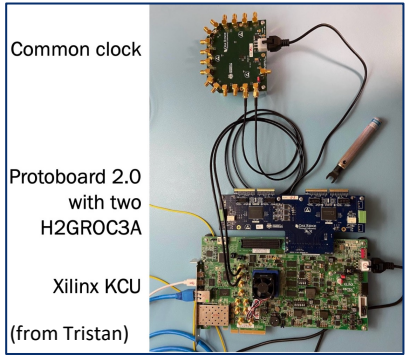
Synchronization Plan between AstroPix DAQ and HGCROC for Pb/SciFi

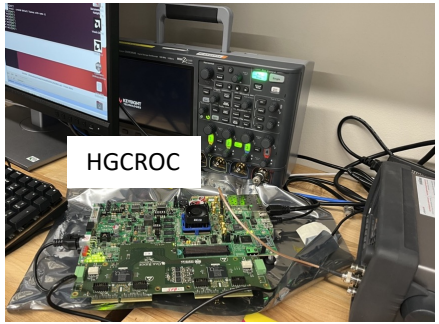
- Provide 40 MHz external clock to HGCROCs and AstroPix DAQ by comparing with FPGA TS difference

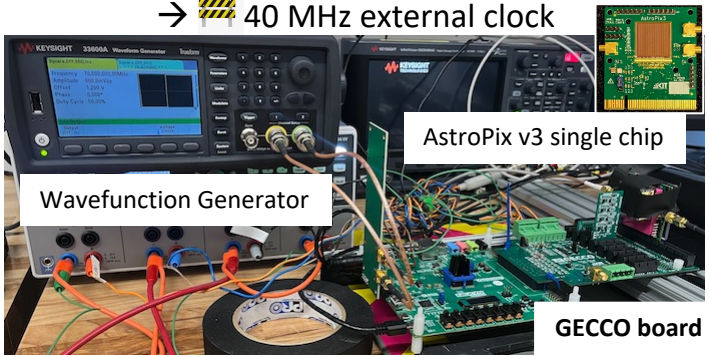


- **AstroPix single chip+**
  GECCO board + Nexys + ASTEP sw/fw
  - 10MHz LVDS external clock
  - Both Timestamp and the FPGA timestamp external
  - 🚧 Debugging: fixed FPGA TS and broad ToT distribution
- **AstroPix quad-chip / 9-chip prototype module +**
  ASTEP HW board + CMOD + ASTEP sw/fw
  - 10 MHz single-ended external clock
  - Both Timestamp and the FPGA timestamp external
  - ✅ Work with quad/9-chip modules

  → 🚧 40 MHz external clock

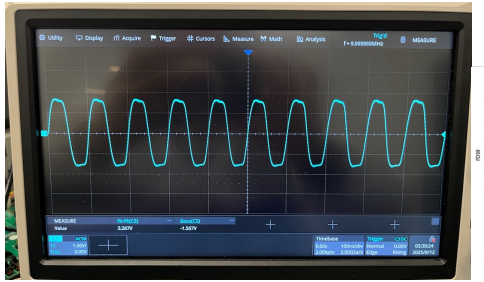


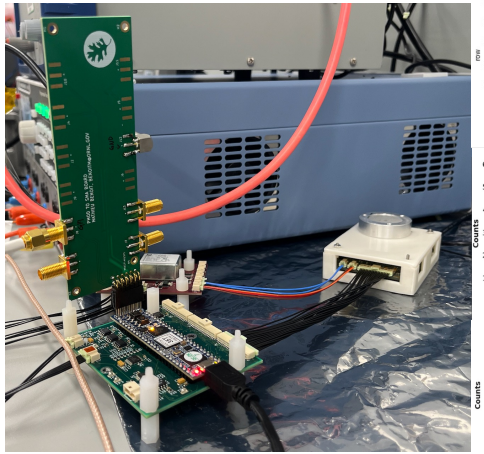




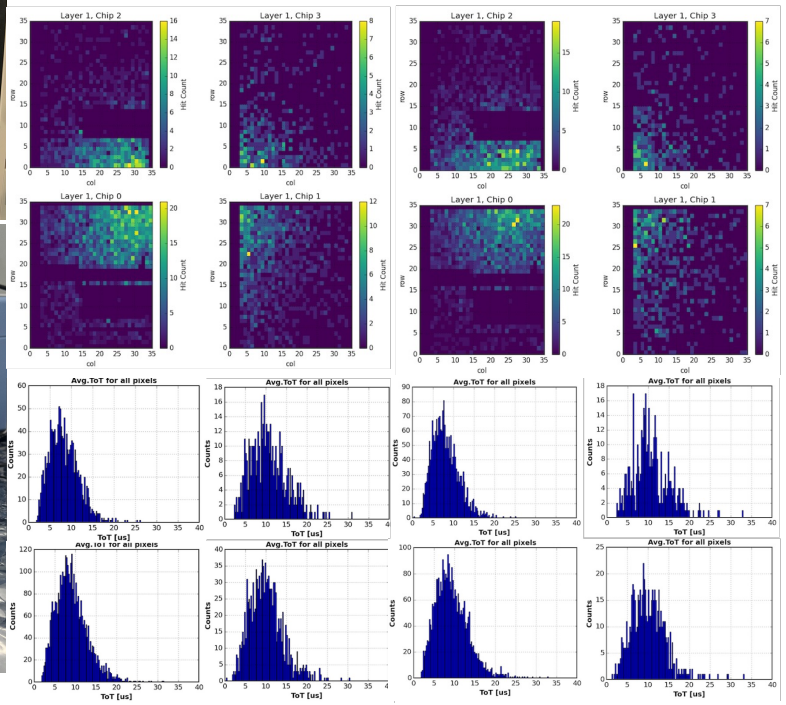
System Testing for Integration: External Clock Testing

- Goal: Verify external-clock operation and basic readout stability
- First attempt: AstroPix quad-chip + ASTEP HW board + Cmod A7 + ASTEP SW/FW
  - 10 MHz single-ended clock via PMOD → working as intended

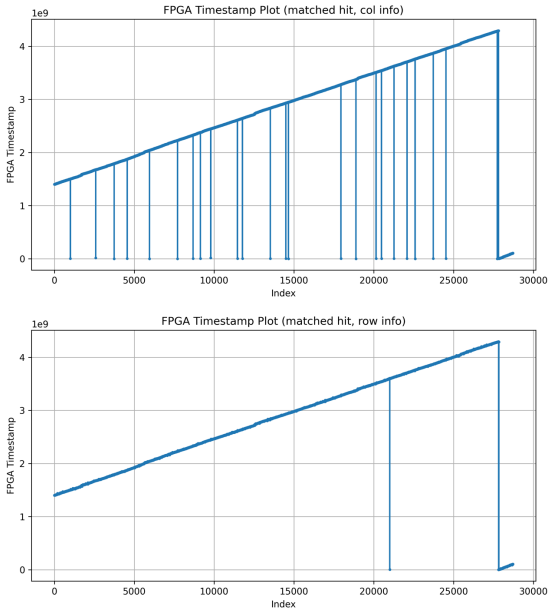




- internal clock vs external clock

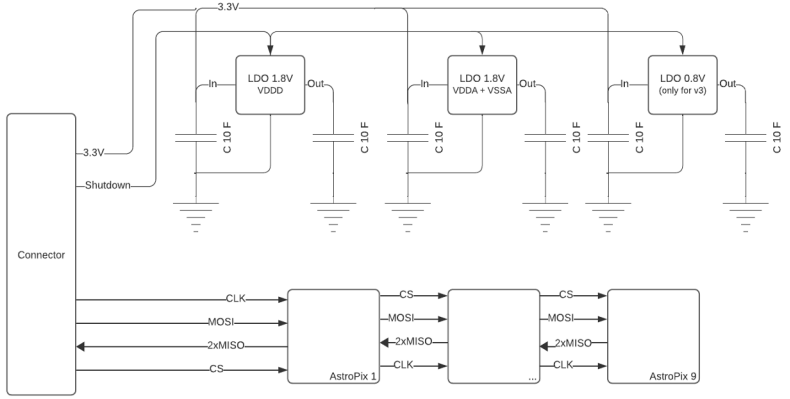


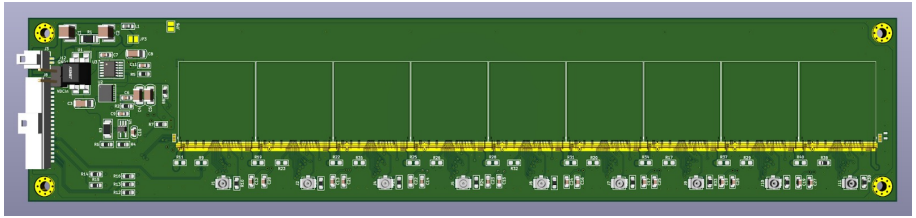
- FPGA TS (external clock)



AstroPix 9 Chip PCB Test Module

- Similar design to quad chip board (no busbar required)
- Nine AstroPix Chips, **Daisy-chained on the Module**
- Each Module plugs into its adjacent Module
- All Modules will be **controlled by the End-of-Tray Card**
- The broadcast commands/data readout through **SPI protocol**
- One main HV line (~500V) and one (or 2) LV line (3.3V)
- Voltage Regulators (LDO) to regulate power on each Module
    - Analog and digital power of 1.8V at Module
- 4 **differential data SPI (Clk, MOSI, 2MISO)** common for stave
- One **single-ended Chip-select SPI** per Module
- Approximately **24 I/O + GND** Pins per Stave
    - Exploring connector options (radiation hard, smaller size)





AstroPix

PED: Preliminary/Final Designs

AstroPix v3

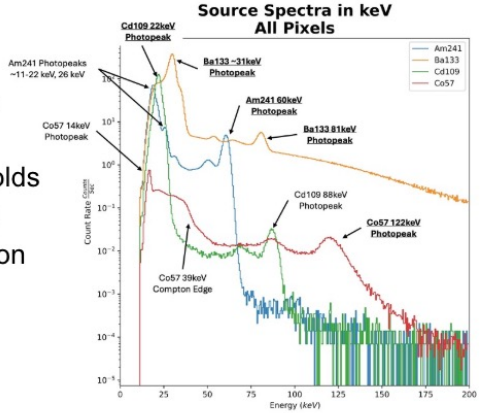
- First full size design: 1.87 cm × 1.96 cm
- Row/Column readout
- Pixel pitch: 500 µm
- Pixel matrix: 35 × 35
- 0.88 mW/cm^2 analog, 12 mW digital
- 2.5 MHz timestamp, 200 MHz ToT

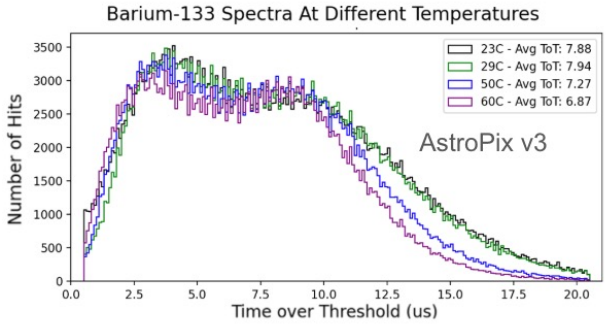
→ **Large size chip for mechanical testing, early performance criteria, daisy chaining**

AstroPix v4

- MPW run, small size: 1 cm × 1 cm
- Individual pixel readout
- TuneDAC for pixel-by-pixel thresholds
- 0.96 mW/cm^2 analog, 3 mW digital
- 3 timestamps, 3.25ns time resolution
  - bug: flash TDC reset
- Pixel pitch: 500 µm
- Pixel matrix: 13 × 16

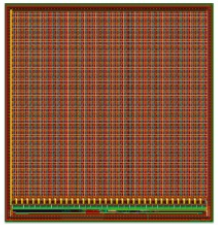
→**Excellent tuning, energy resolution**





AstroPix

BIC PRE-Production:

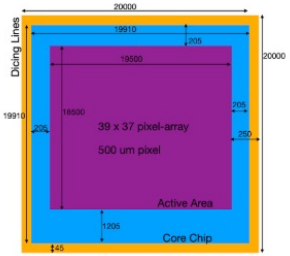


AstroPix v5

- Large size: 1.87 cm × 1.96 cm
- Pixel pitch: 500 µm
- Pixel matrix: 36 × 34
- 0.96 mW/cm^2 analog, 3 mW digital
- 3 timestamps, 3.25ns time resolution (bug-fix)
- **Change of design to new vendor (AMS)**
  - **Switch to deep p-well (from n-well)**
  - **No in-pixel CMOS comparators → implemented some columns with different NMOS comparators in order to optimize power/performance**
  - **Two columns with full dynamic range**

→Being submitted for fabrication now (experienced delays with contract)

BIC Final Chip Design:



AstroPix v6

- Final Full Size: 2 cm × 2 cm
- Pixel pitch: ~500 µm
- Pixel matrix: 39 × 37
- 2 mW/cm^2
- **Expected**
  - **Minor updates to size**
  - **Select comparator design (from v5 columns)**
  - **Bug fixes (if any)**

→Expect to submit the Final production design in an engineering run in 2026

- paid for by EIC Project
  - timescale does not match NASA funding, would have to wait until December 2028 for the next full size run (as decided in NASA AstroPix proposal in January 2025)
- verify the design before production fabrication can start


Argonne
NATIONAL LABORATORY
U.S. DEPARTMENT
of ENERGY