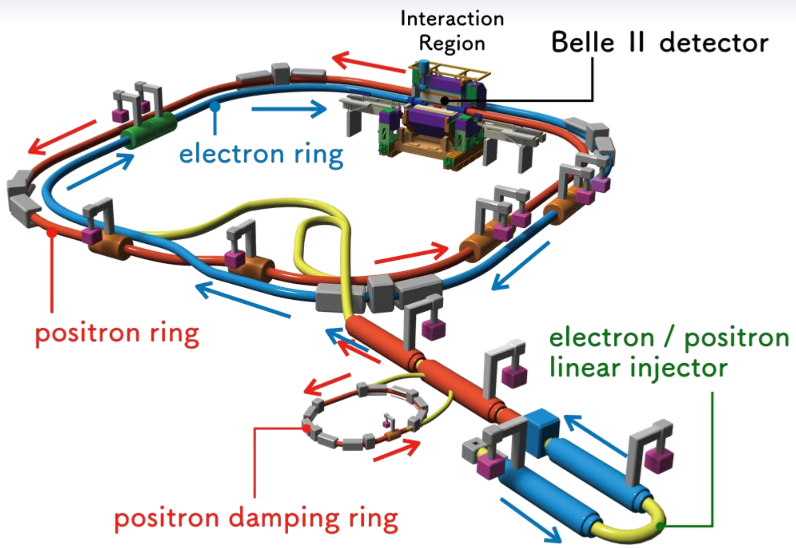
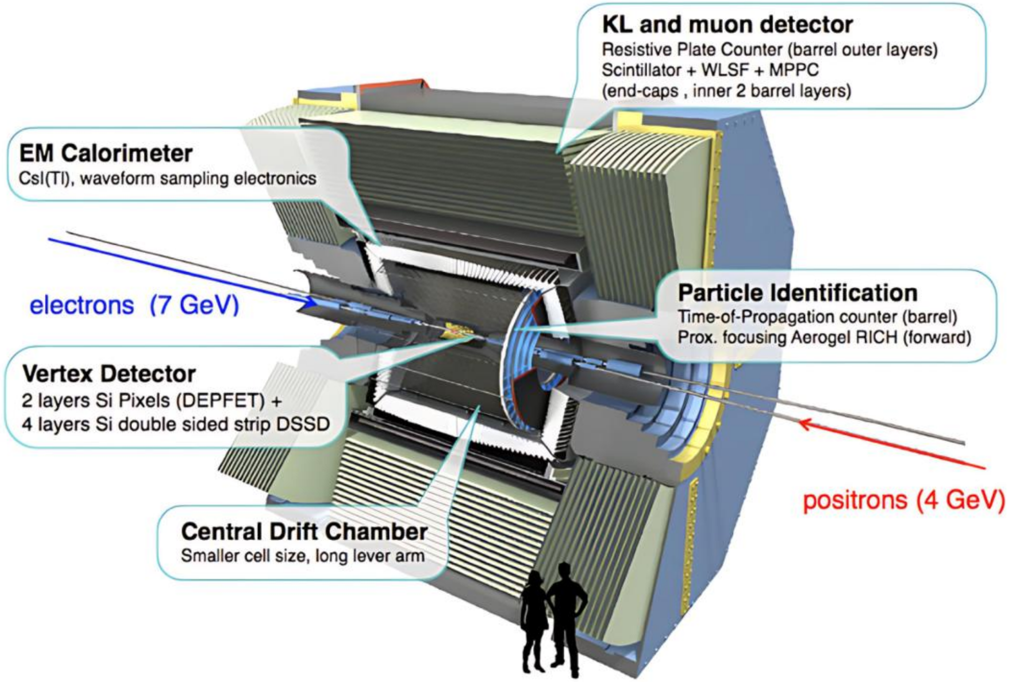
Belle II Vertex Detector: Run Performance (PXD + SVD) and Upgrade Developments (VTX)

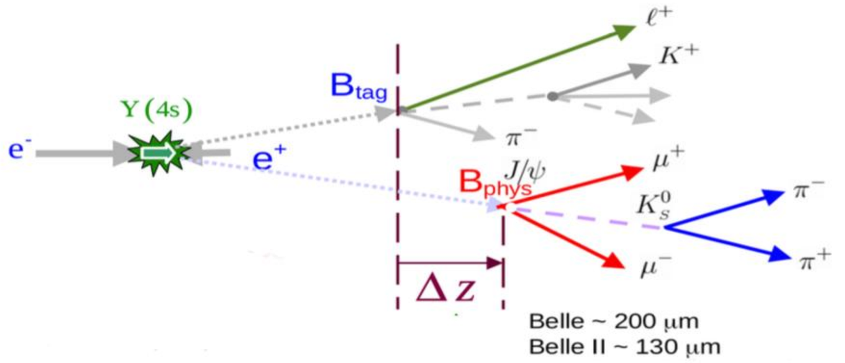
Ravinder Dhayal
On behalf of PXD, SVD, VTX collaborations

VERTEX25

SuperKEKB & Belle II



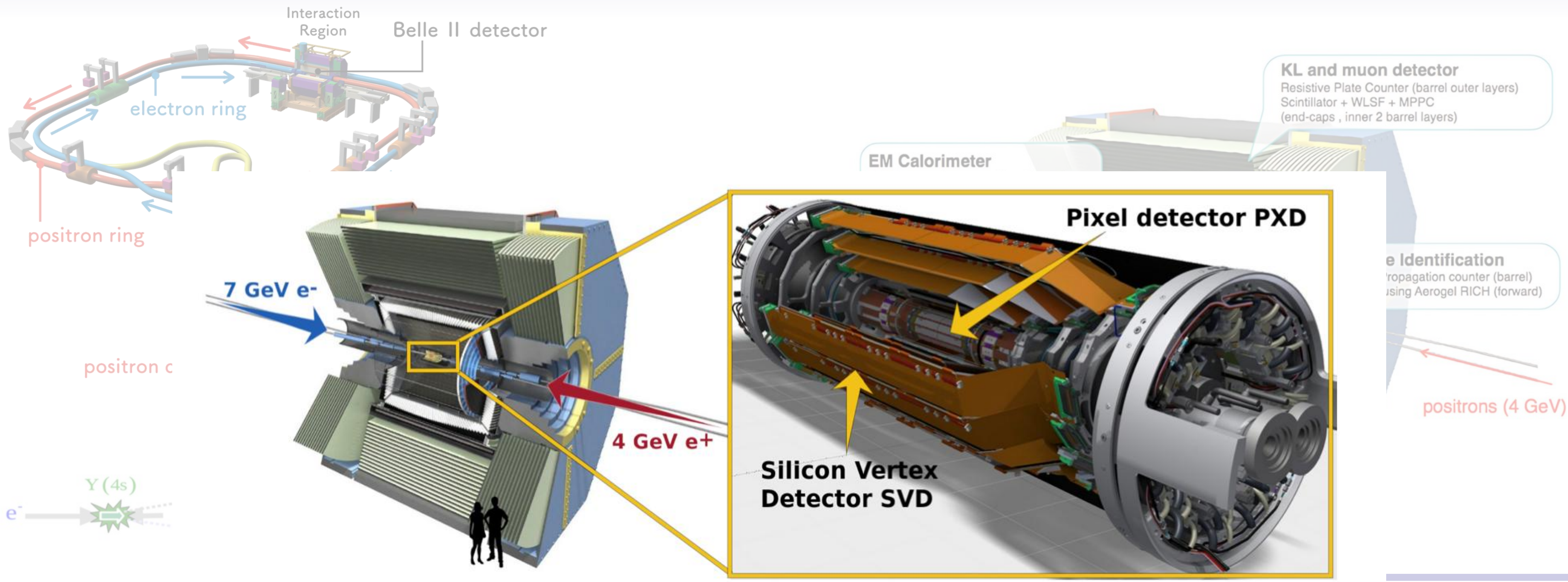




- Design integrated luminosity: 50 ab^{-1}
- Current integrated luminosity: 575 fb^{-1} (~1/2 Belle)
- Peak luminosity recorded: 5.1×10^{34} $cm^{-2}s^{-1}$
- Target peak $\mathcal{L}$: 6×10^{35} $cm^{-2}s^{-1}$

- e^+e^- collider with asymmetric beam energies
- E_{cm} ~ 10.58 GeV = B factory
- Regular data-taking since April 2019
- Restart data-taking in Nov 2025

SuperKEKB & Belle II



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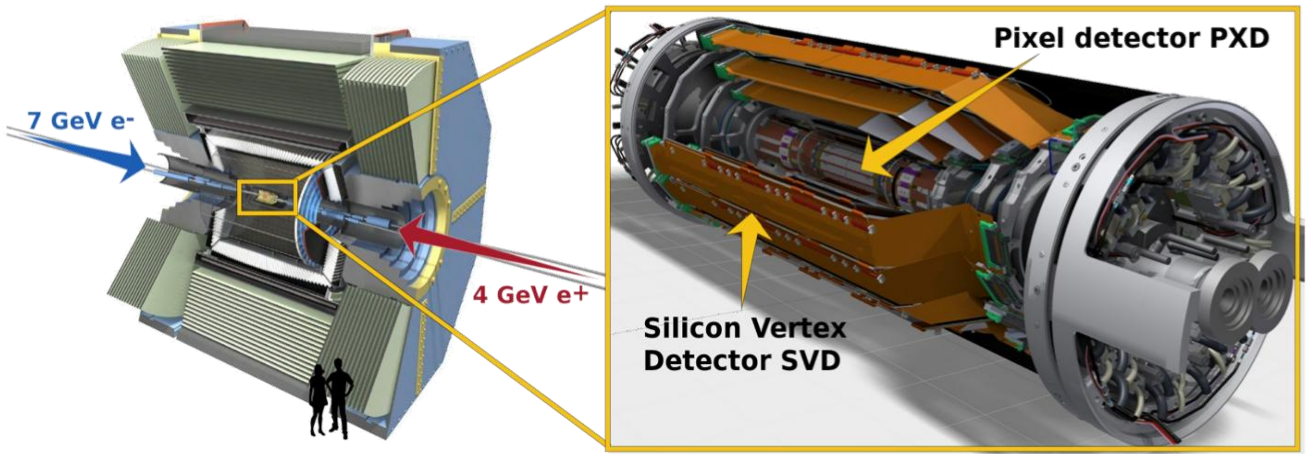
Vertex Detector (VXD)

Why VXD?

- Excellent vertexing and Tracking down to low p_t (<100 MeV/c)
- Close to the interaction point (inner layer only 14 mm away)
- Impact parameters resolution ~z < 20 μm
- Operate in high background environment
- Trigger rate 30 kHz



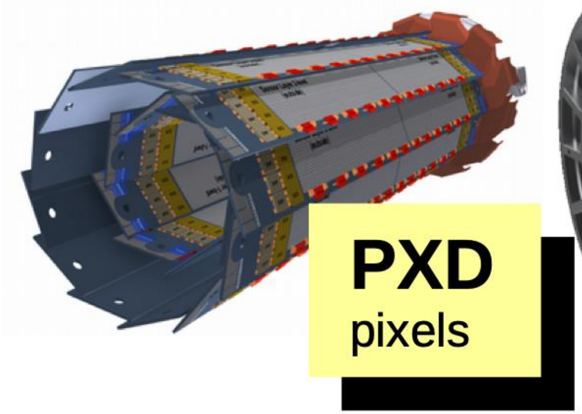
Two sub-systems:

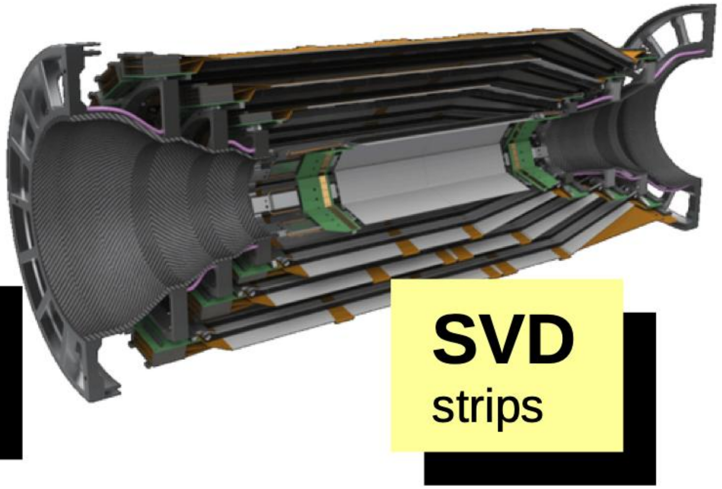
Pixel Vertex Detector (PXD)

- DEPFET sensors
- 2 Layers : 14, 22 mm radii
- PXD 1: 2019 – 2022 - incomplete 2-layer
- PXD 2: from 2024 - complete

Silicon Vertex Detector (SVD)

- Four layers double-sided silicon strips
- 39 - 135 mm radii



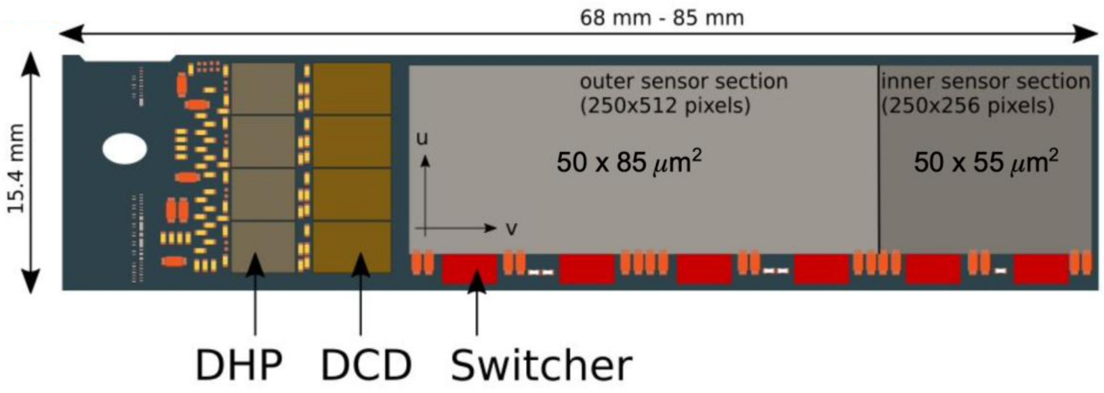


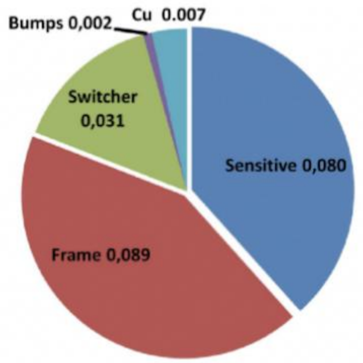
The Pixel Vertex Detector (PXD)

Depleted P-channel Field Effect Transistor (DEPFET)

(concept developed at Semiconductor Laboratory of the Max Planck Society (MPG HLL))

- Fast charge collection (~ns) into internal gate
- Lower power consumption and heat dissipation
- Modules: Self - supporting “all - silicon” structure
  - Support frame ~ 525 μm/450 μm thick
  - Monolithic active area 75 μm thick
- ASICs on module
  - Switcher:
    - Consecutive row selection for data readout
  - DCD: Drain Current Digitizer
    - Analog to digital conversion of signal
  - DHP: Data Handling Processor
    - Digital Processing, data formatting
- Low material budget (~ 0.21% average X_0)



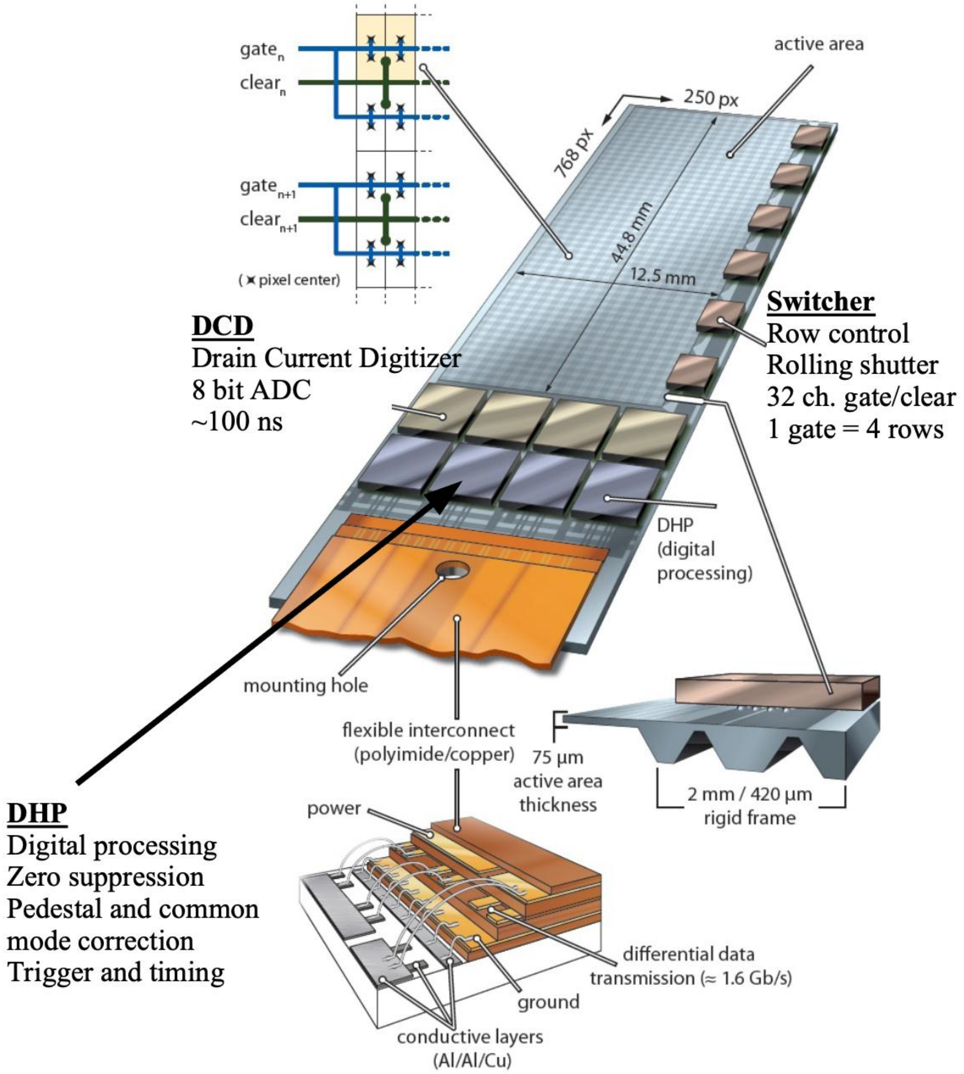


~0.21% X_0/ layer material budget

PXD: Readout and Reconstruction

Depleted P-channel Field Effect Transistor (DEPFET)

- Readout Scheme
  - Rolling shutter readout → low power
  - 192 gates, ~100 ns per gate → full frame ≈ 20 μs
- Design
  - 1% occupancy (Layer 1)
  - system limit ≈ 3% (DHP/DAQ/tracking)
- Sensor Scale
  - 40 sensors, each 250 × 768 pixels → ~8 Mpixel total
- PXD reconstruction uses high-granularity clustering (end-pixel positions for long clusters) and track-hit matching
- Achieves ~98-99% efficiency for low-p_t tracks despite background from the 20 μs integration time



PXD Design: Modules, Ladders, and Cooling

Module

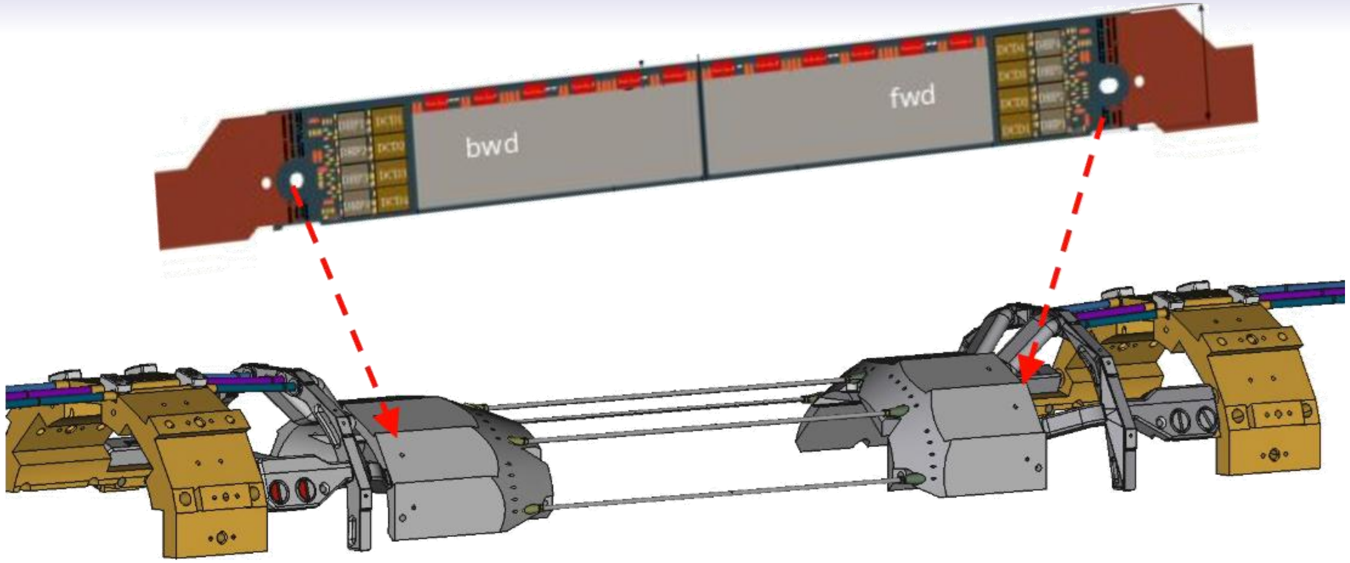
- 2 modules glued to one ladder
- 20 ladders in total (2 modules per ladder)

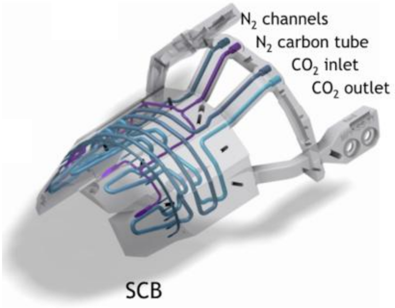
Ladders

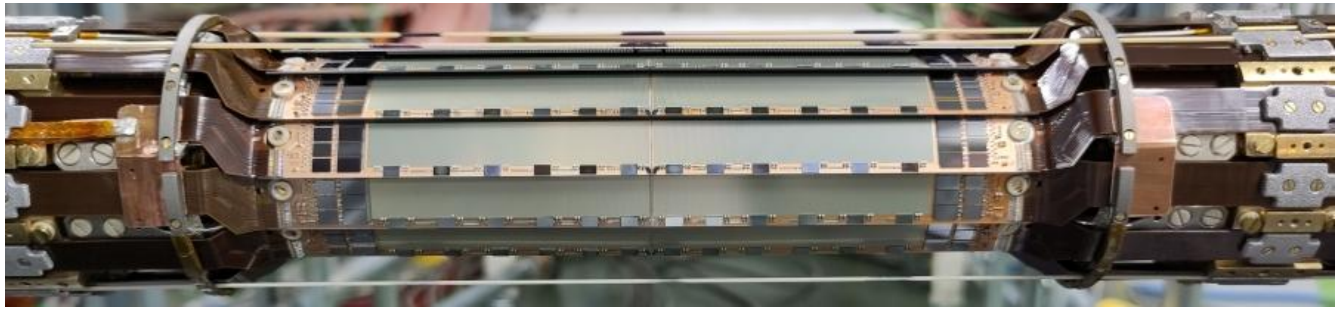
- 10 ladders – 1 half-shell
- Screwed on support colling block (SCB)
- Half-shell (HS) mounted on beam pipe

Cooling

- ~ 9 W per module = ~ 360 W for full detector
- 2-phase CO2: DHP + DCD (8 W)
- N_2 gas: Switcher + sensor (1 W)







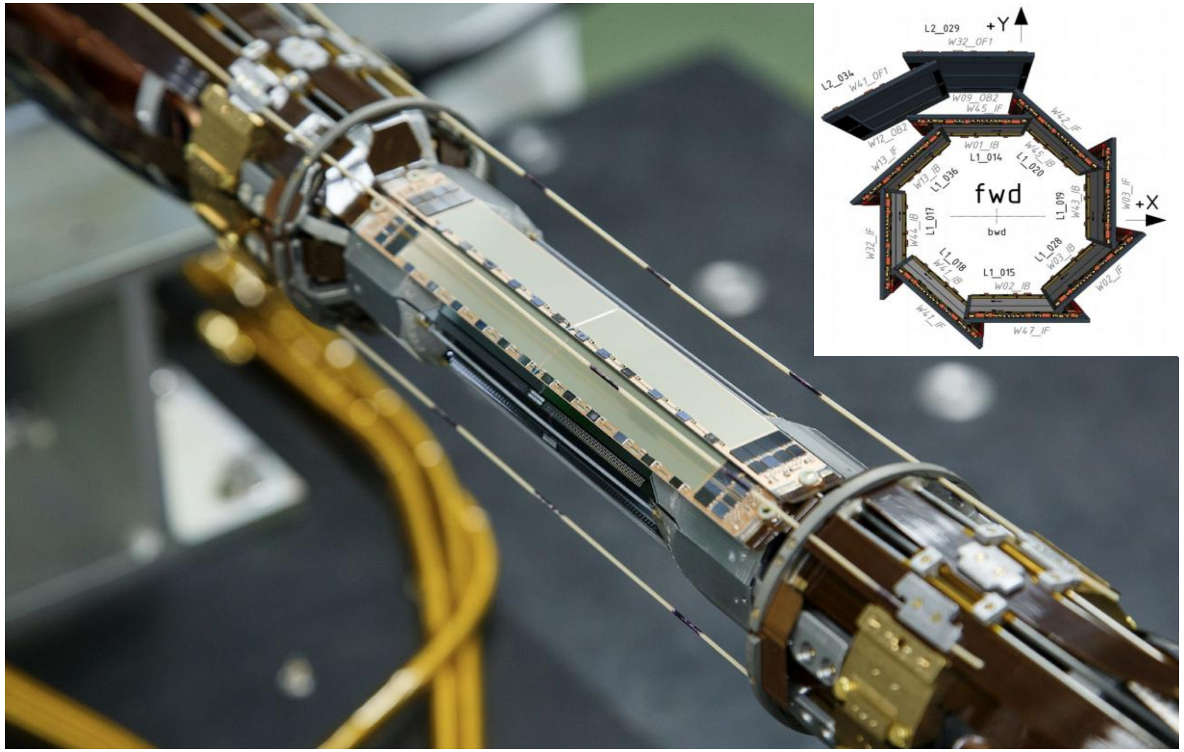
PXD 1: 2019 – 2022

Run 1 details

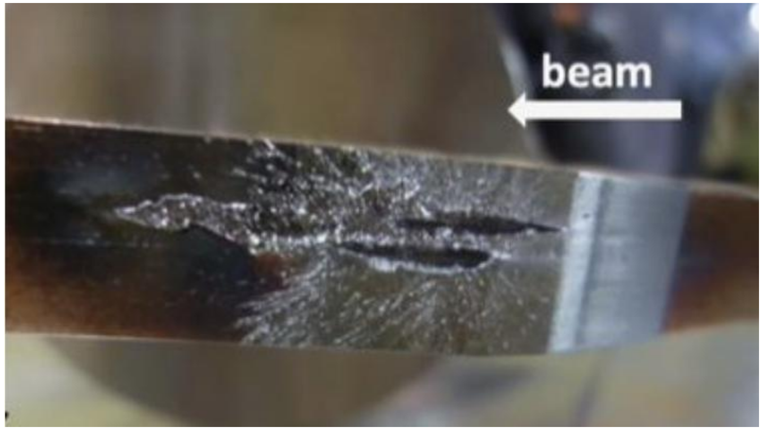
- from 2019 - 2022 with incomplete 2nd layer
- 8 ladder - inner layer (fully populated)
- 2/12 ladder - outer layer (incomplete)

PERFORMANCE

- Di - muon hit efficiency
  - ~ 99 % in fiducial region
  - ~ 96 % in tracking acceptance
  - Noise performance < 1 ADU (~200 e^-)
- Impact parameter resolution: ~1.5 - 2 times better than Belle



- The lower efficiency in Run 1 was largely due to damage from sudden beam losses (SBLs)



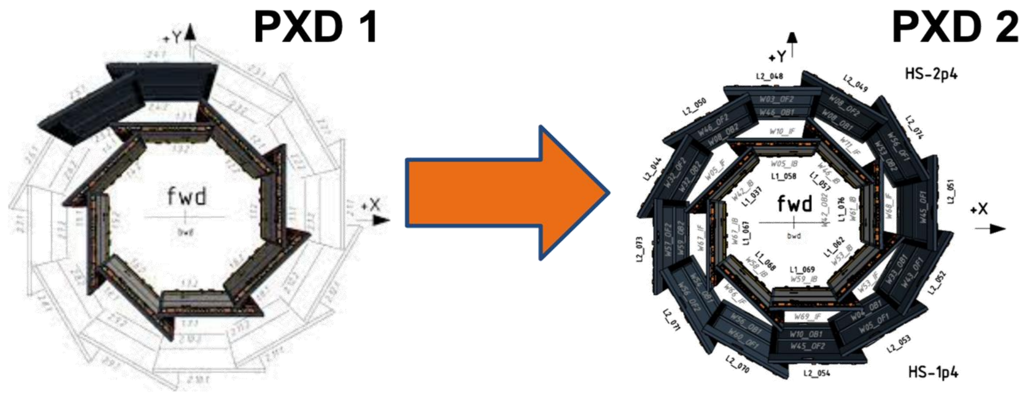
Sudden Beam losses:

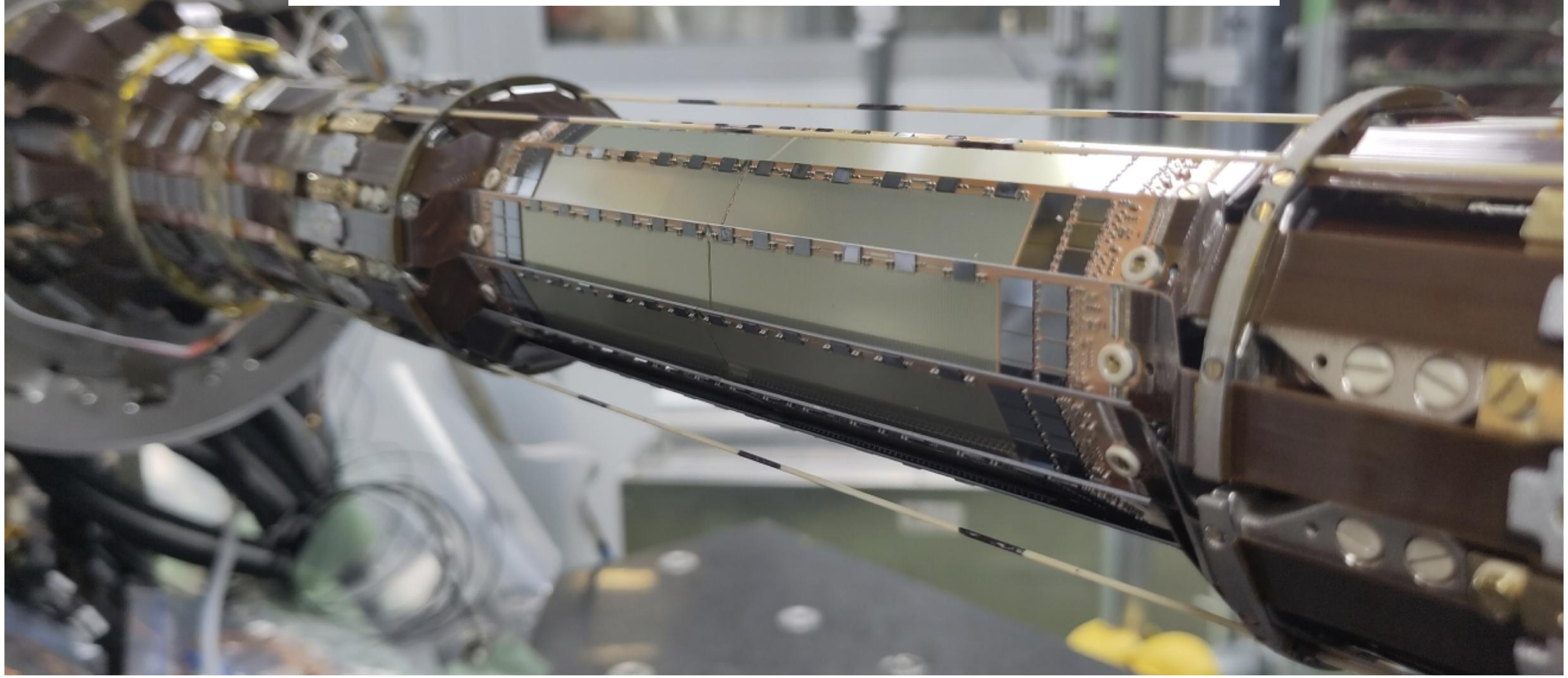
Causes: Most likely dust particles

High instantaneous radiation doses

Improve detection and PXD power shutdown

PXD 2: Installed in 2023 with completed 2nd layer

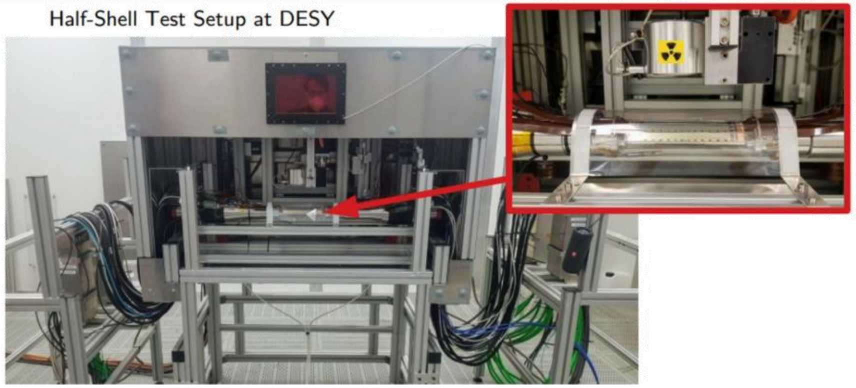


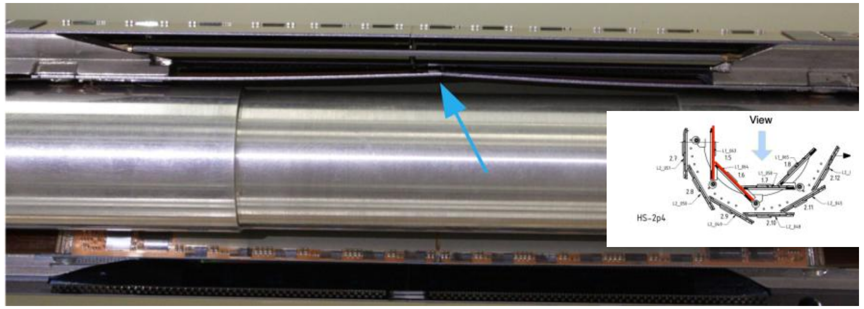


Commissioning of PXD 2 – From DESY to KEK Installation

Commissioning at DESY

- Conducted source scans and system tests on half-shell setups
- Tested power supply, DAQ, CO_2, and N_2 cooling with Aluminium dummy beam pipe
- Two ladders were damaged by glue joint failure, highlighting sensitivity to heating and bending
- The half-shell was repaired with ladder replacements and improved mounting, with careful monitoring of temperature and bending



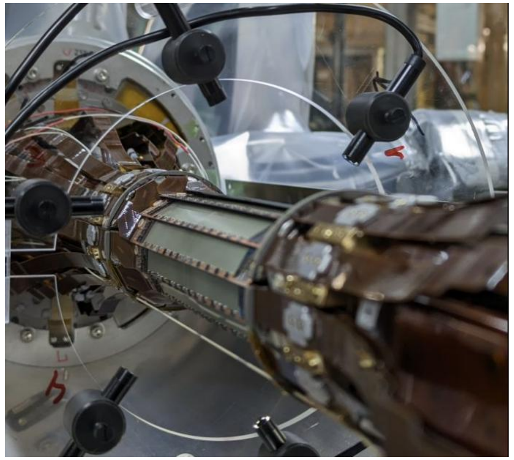


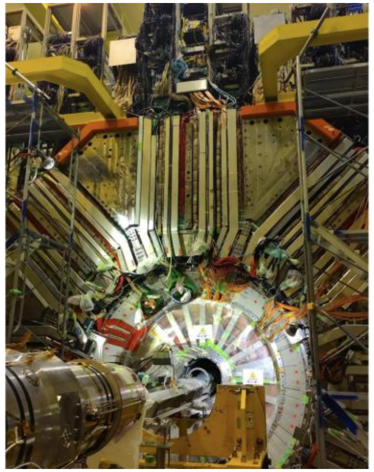
Commissioning at KEK

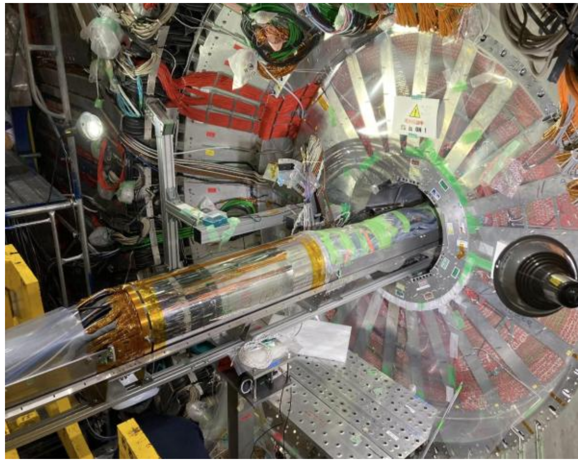
- First operation of full PXD 2
- Issue:
  - 2 ladders with significant bowing
  - One module with high noise

Installation in Belle II

- Attached SVD and installed in Belle II
- Perform cosmic runs to study bending more precisely



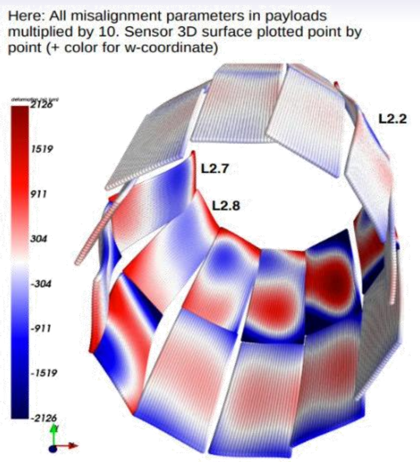


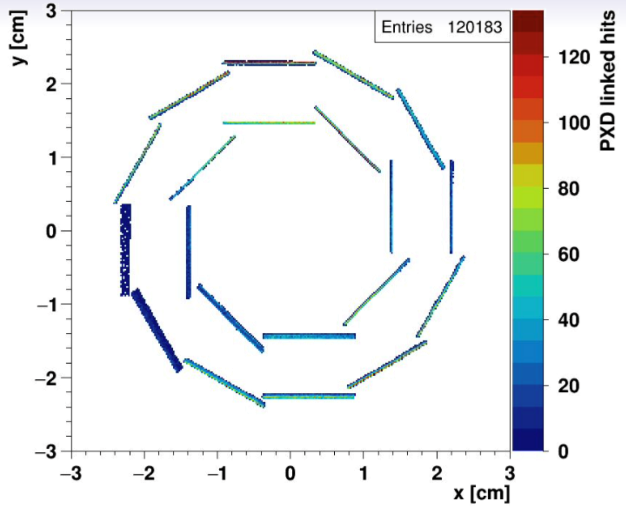


PXD 2 Cosmic Study and Operation Performance

PXD 2 cosmic data taking

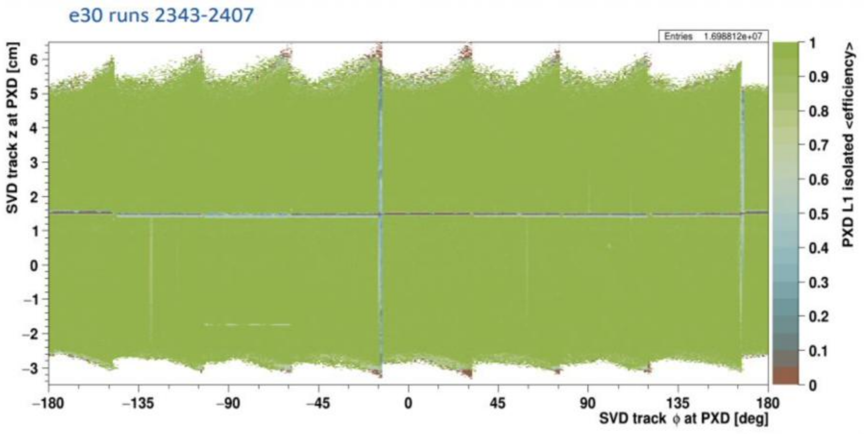
- Study ladder behaviour with cosmic data
  - › Test with different cooling setups
- Bending in 2 ladders (4 Modules):
  - › ~1 mm sagitta observed, smaller than the 2 mm, safe limit from endurance studies
- ✓ Decided to keep both ladders off during operation start



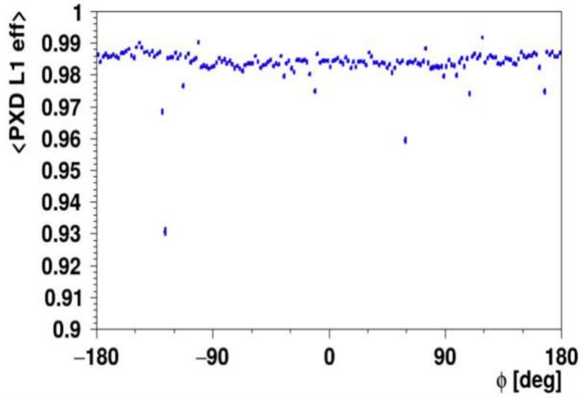


Operation Performance from March - April 2024

- Running with 35/40 modules:
  - › 4 Modules off because of bowing
  - › 1 Module off because of noise
- L1 and L2 efficiency > 98 % in fiducial region
- Operation temperature high but within limits
- Noise <1 ADU
- Smooth operation with minor down times



Efficiency map for the PXD Layer 1 modules



Efficiency as a function of the azimuth angle Φ

Sudden Beam Loss and Damages

Two beam loses with high dose in PXD

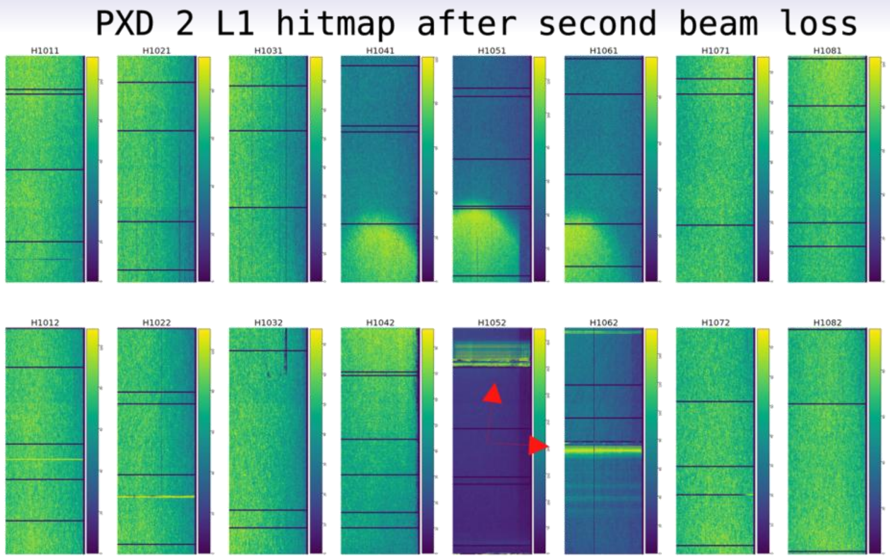
Possible Reason for SBL:

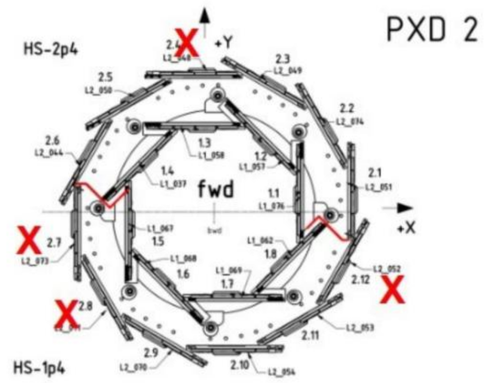
- Vacseal residue in the vacuum system
- Other sources of SBL likely exist

SBL effect on PXD

- SBLs damaged Switcher ASICs, causing ~2% PXD readout loss and increased currents
- After the 2nd SBL, three L2 modules were switched off for thermal safety, and PXD 2 was subsequently powered down
- PXD 2 remains functional with good performance, however, additional SBL events may cause further damage

Therefore, PXD 2 will be turned off during beam operations to prevent further damage





The PXD group is developing a fast-shutdown board to power down the Switcher ASICs rapidly (target <30 μs), to minimize the risk of SBL-induced damage

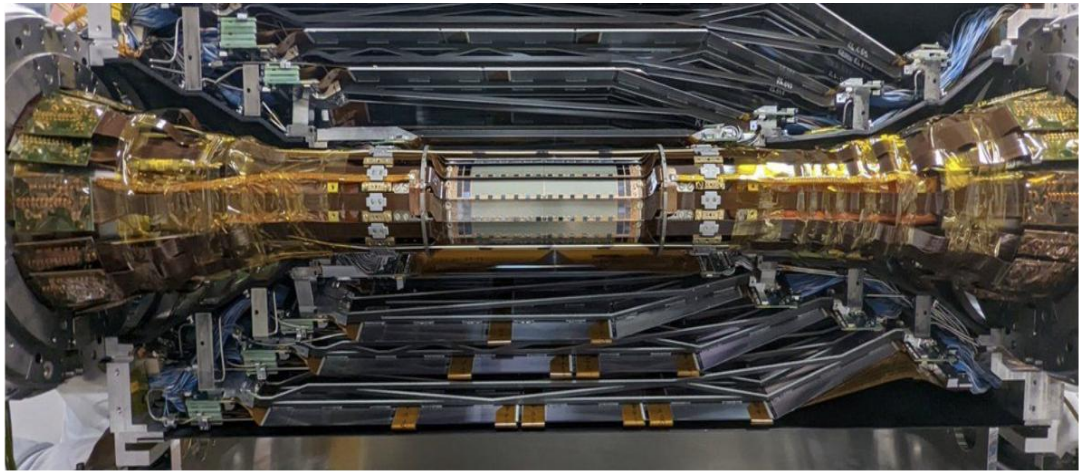
Current Status and Future Plan

Current status

- Belle II is the first particle physics experiment to use a DEPFET pixel vertex detector
- PXD 1 run from 2019-2022
- PXD 2 commissioned and installed in 2023
- PXD 2 data taking has been started in 2024
  - 35/40 modules in operation
  - Efficiency > 98 % in fiducial region
- Two major SBL events happened in 2024
- ~2% of PXD 2 readout affected

Future Plans

- Improving faster detection of beam instabilities earlier beam abort
- Decided to turn off PXD 2 for now to investigate
  - To optimize beam operation
  - To solve origin of SBL events

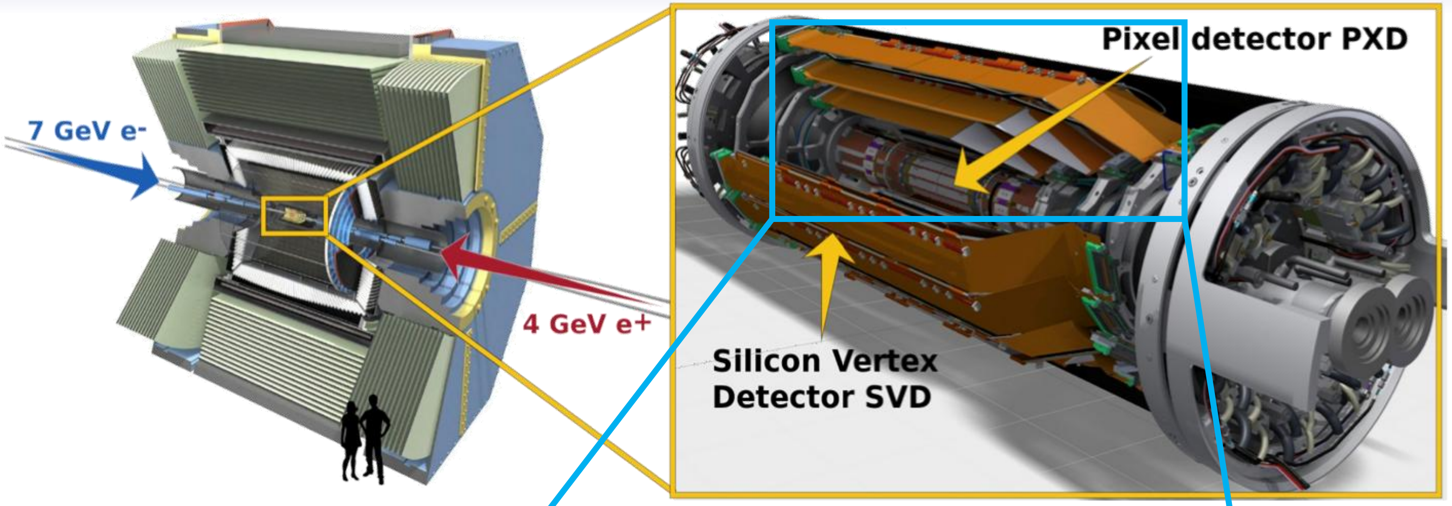


Silicon Vertex Detector (SVD)

ref: K. Adamczyk et al 2022 JINST 17 P11042

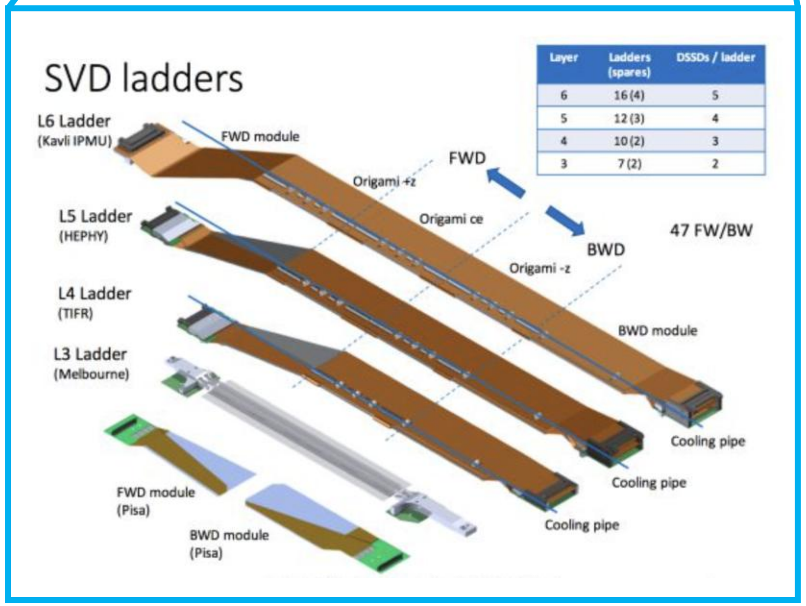
SVD Design

- 4-layers structure
- Double-sided Silicon Strip Sensor (DSSD)
- DSSD modules arranged in structurally and electrically independent unit called ladders
- Radii of 4 Layers: 39 -135 mm
- Low material budget: 0.7% X_0 per layer



What SVD can do?

- Standalone tracking for low momentum tracks and precise vertexing of B^0, K_s and Λ^0
- Extrapolate tracks to PXD
- Provide dE/dx information for charged-particle identification

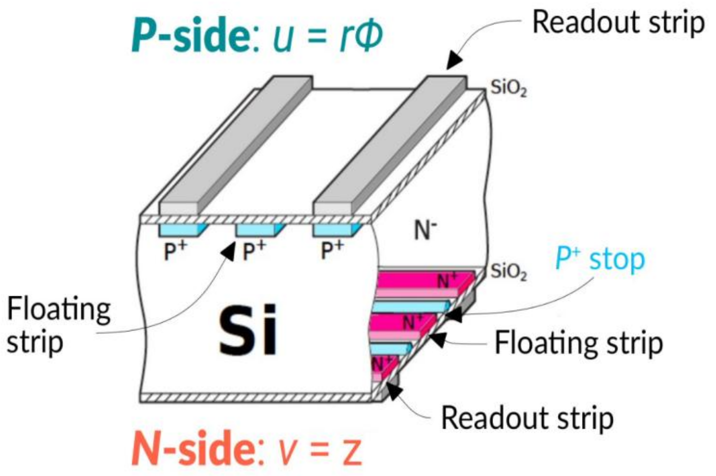


Layer	Ladders (spares)	DSSDs / ladder
6	16 (4)	5
5	12 (3)	4
4	10 (2)	3
3	7 (2)	2

SVD Sensor Design

Double Sided Silicon Strip Sensors (DSSD)

- 172 DSSD with area coverage 1.2 m^2
- Bias voltage: 100 V
- Perpendicular strips to provide 2D spatial info
- Depletion voltage: 20 - 60 V
- Strip pitch: 50/75 μm (r-ϕ) and 160/240 μm (z)
- Readout: APV25 chip, 50 ns shaping time
- Cooling: two-phase CO_2 system
  (-20° C with PXD1 and -25° C with PXD2)

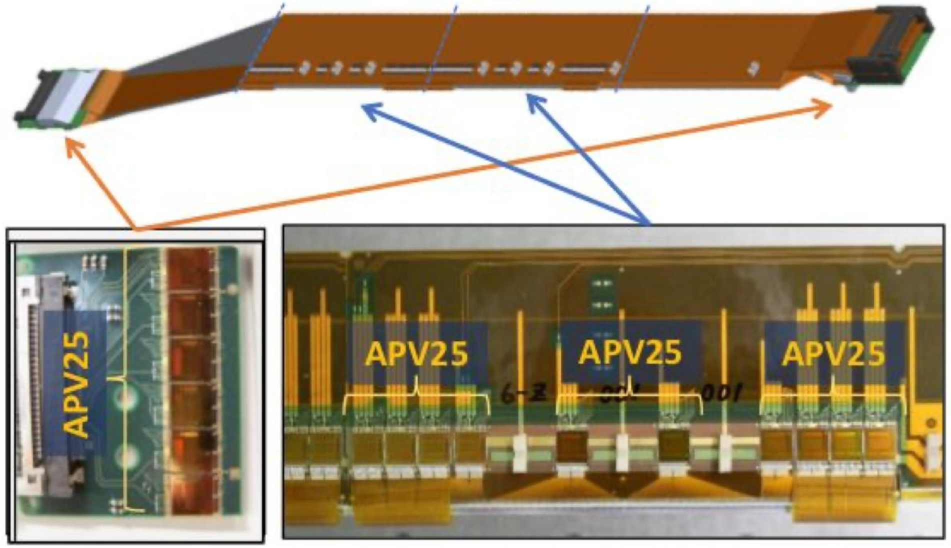


Front-end electronics : APV25 chip

A high background in Belle II requires short signal shaping time and a good radiation hardness.

› APV25 chip is a suitable solution for SVD
› Originally developed for the harsh radiation environment at the LHC

APV25 chips in ladder



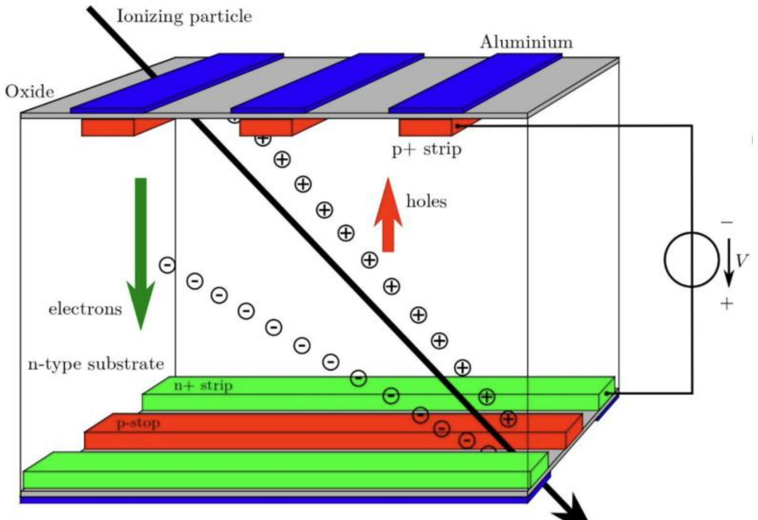
All 1748 APV25 readout chips functional

More information on SVD:
K. Adamczyk et al 2022 JINST 17 P11042

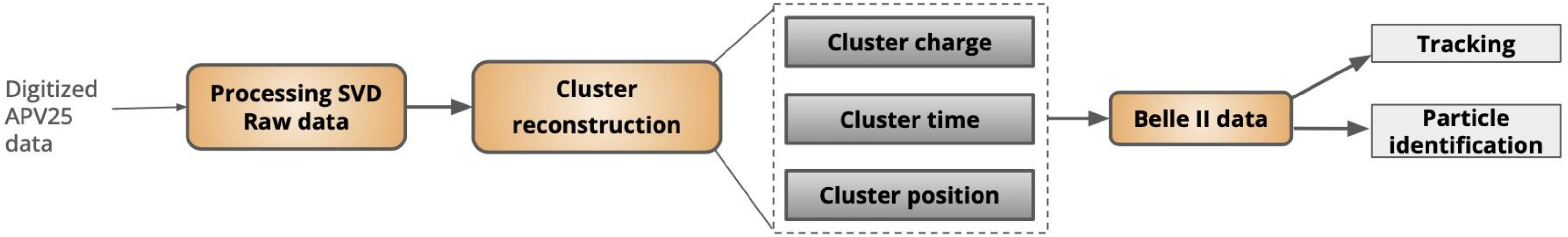
SVD Data Reconstruction

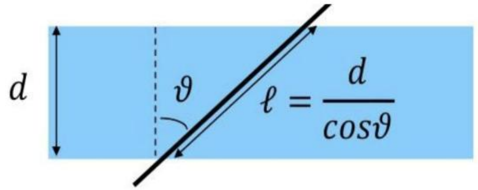
Charged particles passing through fully depleted sensors creates e-h pairs, which produces hits in the strips

- **Cluster**: Collection of strips with signal-to-noise ratio (SNR) above certain threshold
- A cluster has
  - **Charge**: Sum of the charges of each strip belonging to the cluster, depends on incident angle of the particle
  - **Time**: Charge-weighted average of strip times relative to trigger
  - **Position**: reconstructed from strip charges
  - **Noise**: Quadrature sum of noise of each strips



Charged particle passing DSSD





d ≡ 300 - 320 μm

SVD Operation during Run 1

Performance in Run 1 (March 2019 – June 2022)

Cluster charge

– Stable throughout and matching the expectation; 24ke$^-$ for a MIP passing through a ~320 µm thick silicon sensor

Cluster SNR

– Very good cluster SNR in all 172 sensors
– Small reduction in 2022 due to radiation damage

Position resolution

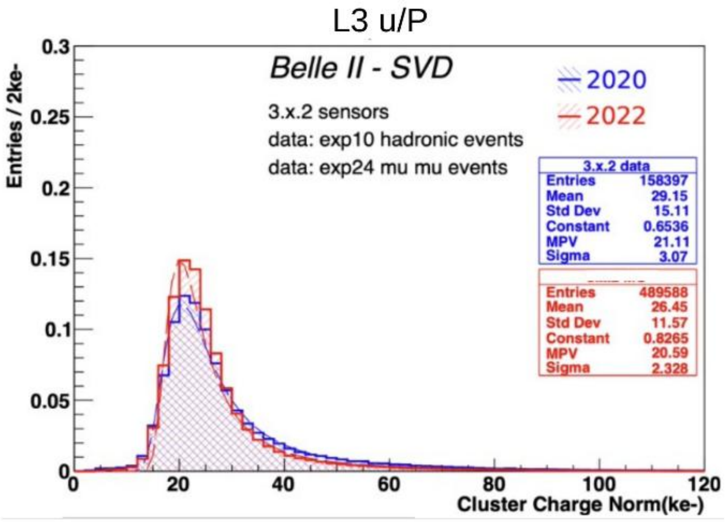
– Stable position resolution within 10–25 µm observed, as expected from strip pitches

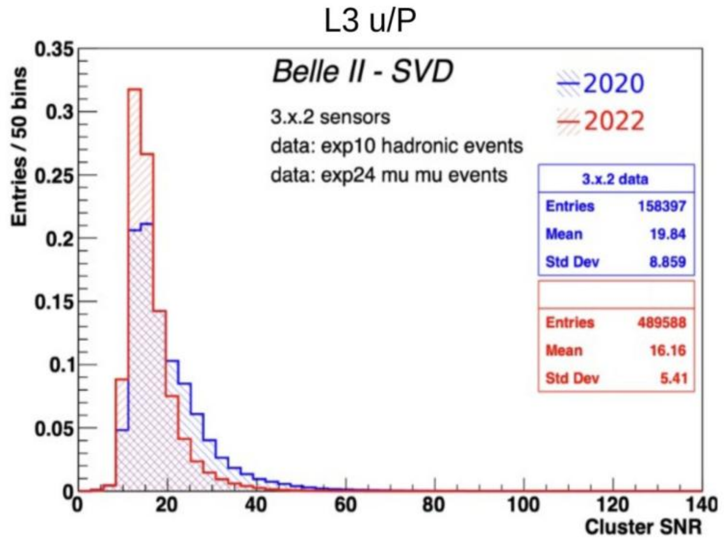
Hit efficiency

– Hit efficiency > 99% per sensor

Masked strips

– Total masked strips < 1%

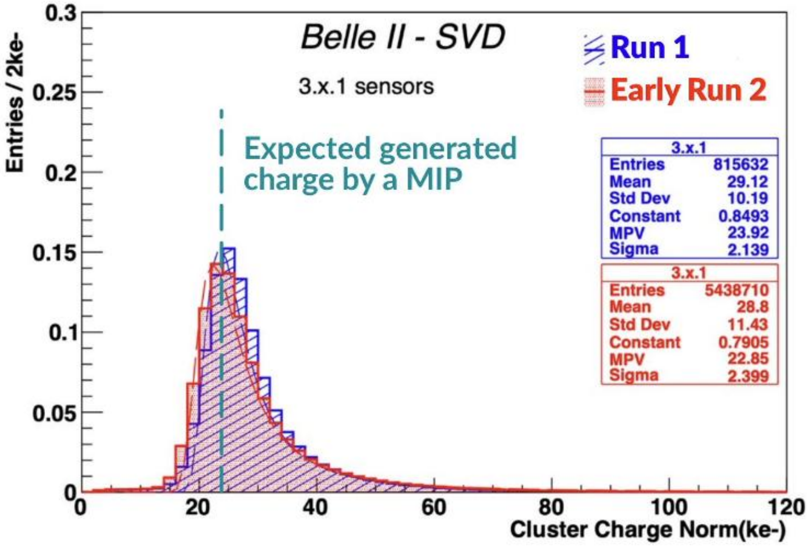


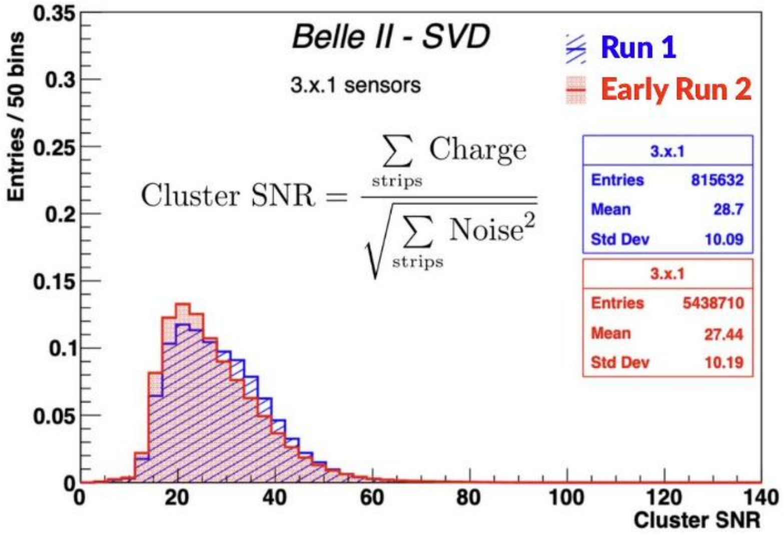


SVD Operation during Run 2

- SVD was extracted and reinserted during PXD 2 installation (LS1), making Run 2 performance crucial

Run 2: Feb – July 2024,
Oct – Dec 2024



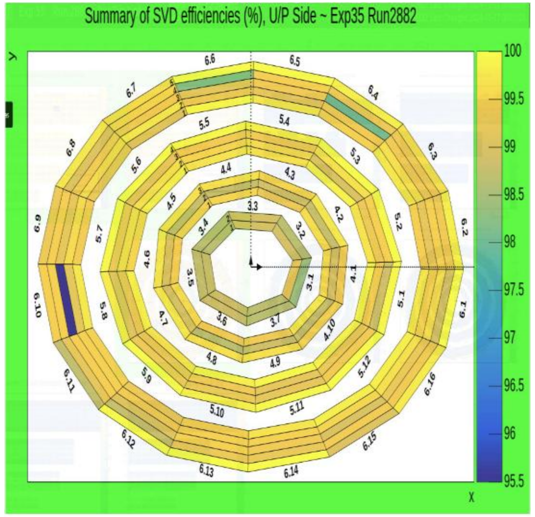


Cluster charge and SNR

- No significant changes in cluster charge and SNR

Sensor efficiency

- Sensor efficiency is very high (>99%) for most of the sensors
- Very stable over the whole period of data taking

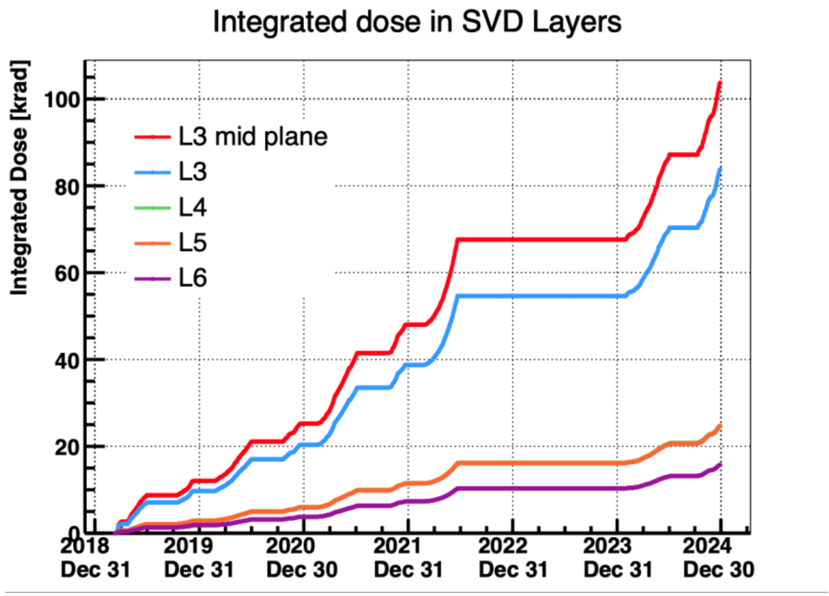


Occupancy during this run ~1%

Radiation and Beam Background Effects on SVD

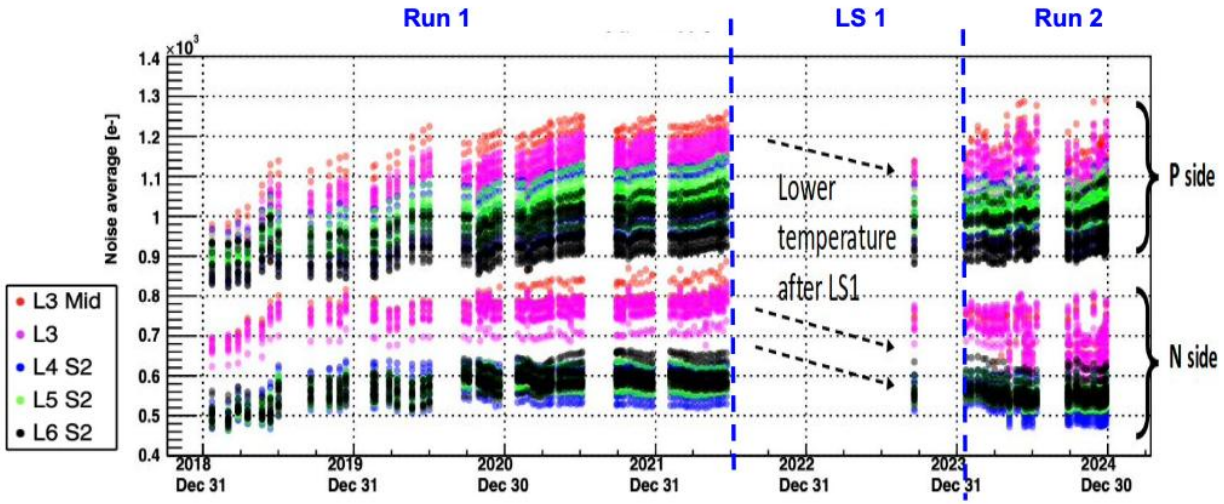
Beam Background Effects

- Sudden beam loss are a risk, but no pinhole defects observed in DSSDs during Run 2
- Integrated radiation dose can still degrade sensor performance: increased leakage current, strip noise, and reduced charge collection efficiency



Radiation Dose Measurements

- Total integrated dose on Layer 3 mid-plane: ~100 krad, equivalent to ~2.5×10^{12} n/cm^2 (measured via diamond detectors) with no observed performance degradation
- Sensor noise rose 10–35% in Run 1 (due to radiation)
- Partially recovered (10%) after LS1 (annealing + better cooling)



SVD Performance Resilience

- No significant degradation in SVD performance was observed
- Current SVD hit occupancy <1%, increased during Run 2 due to machine conditions
- Sensors still collect charge effectively after 10 Mrad from test campaign

Current Status and Future Aim

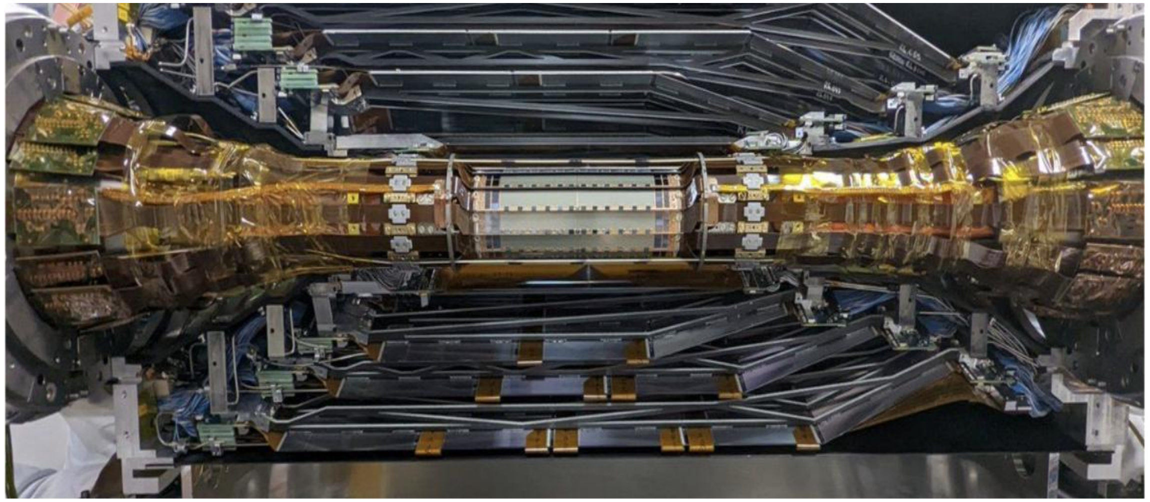
Current Status

- Smooth and stable operations
- Strict monitoring in place for SVD due to increase in beam current
- Occupancy and radiation damage remains below the critical threshold, SVD behaves as expected
- Excellent SVD hit-time performance: resolution < 3 ns for signals, while time range of beam-induced background is around 100 ns

Future Plan

- New algorithms use time resolution to suppress background and preserve tracking performance at high rates

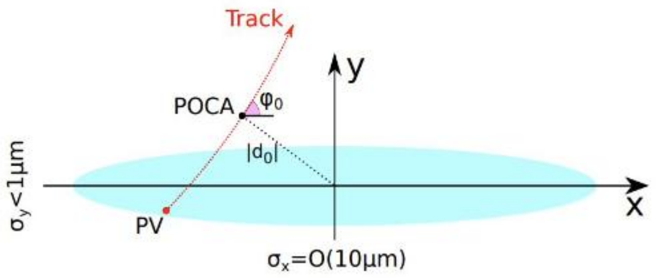
- Maintain SVD performance with higher occupancy anticipated with increased SuperKEKB luminosity



Impact of Vertex Resolution

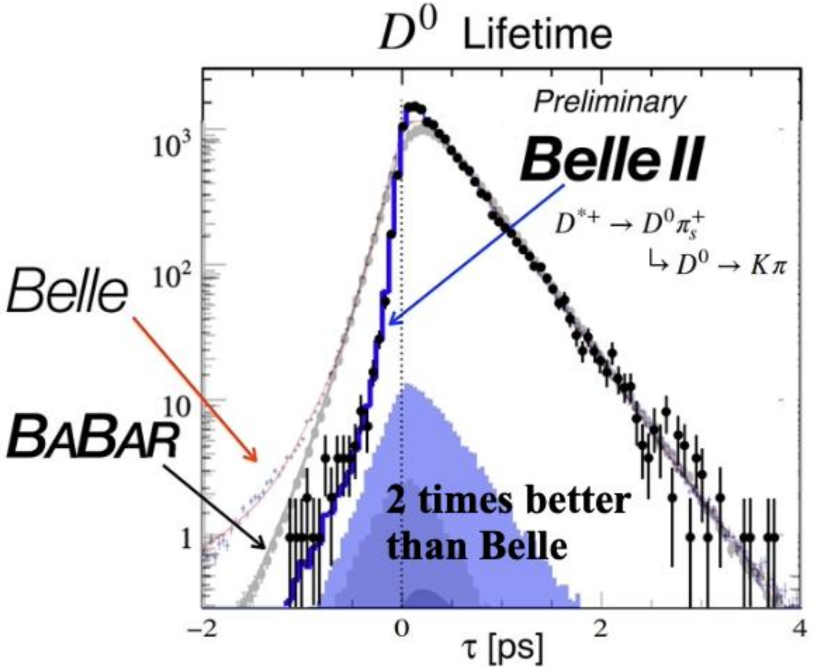
Vertex Resolution

- Vertex reconstruction essential for time-dependent CP violation and lifetime measurements, enabling precise decay-time resolution for B meson
- PXD and SVD play a key role
- Measuring the point of closest approach from particles from the interaction point in x, y
- Taking advantage of tiny interaction point with PXD at 14 mm
- d_0 resolution of 10-20 μm
- z_0 resolution of 20-40 μm



Belle II lifetime measurements that benefited from the excellent vertex resolution:

D_s^+: PRL 131, 171803 (2023)
B^0: PRD 107, L091102 (2023)
Ω_c^+: PRD 107, L031103 (2023)
Λ_c^+: PRL 130, 071802 (2023)
D_0/D^+: PRL 127, 211801 (2021)

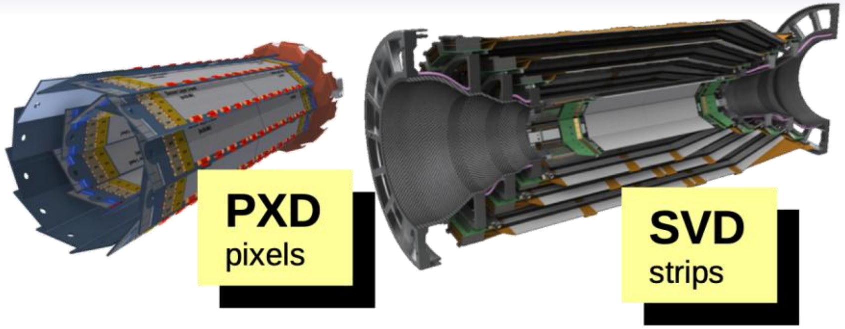


Impact of better vertex resolution

Vertex Detector Alignment

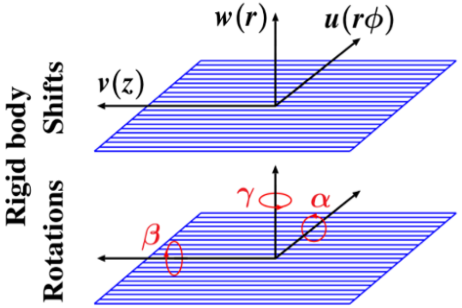
What is detector alignment?

- Calibration of the true spatial positions and orientations of detector sensors (PXD, SVD)
- Track reconstruction is matched with actual hit measurements using global track-based fits
- Minimizes track-to-hit residuals across thousands of events



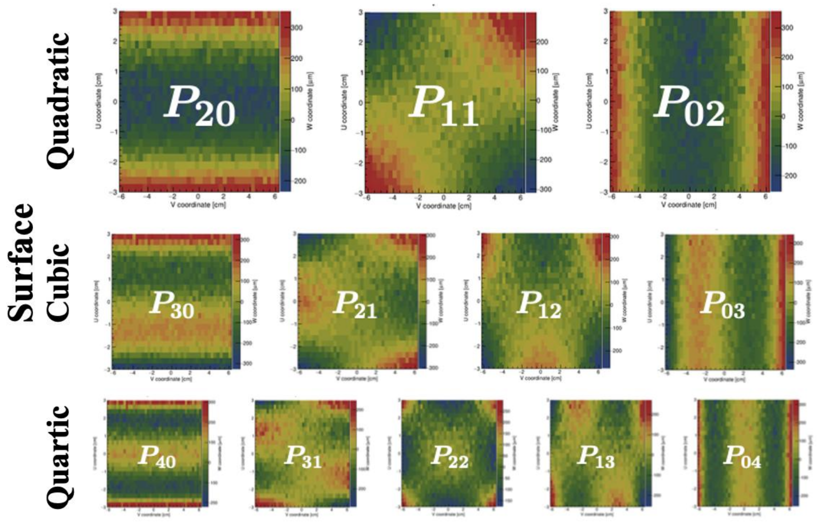
What do we align?

- VXD includes: 2 PXD half-shells, 4 SVD layers (~ 65 ladders)
- Each has 6 rigid-body DOFs (translations and rotations)
- Includes surface parameters (Legendre polynomials up to 4th order)
- In total >4000 parameters are solved using Millepede II



Why is alignment needed?

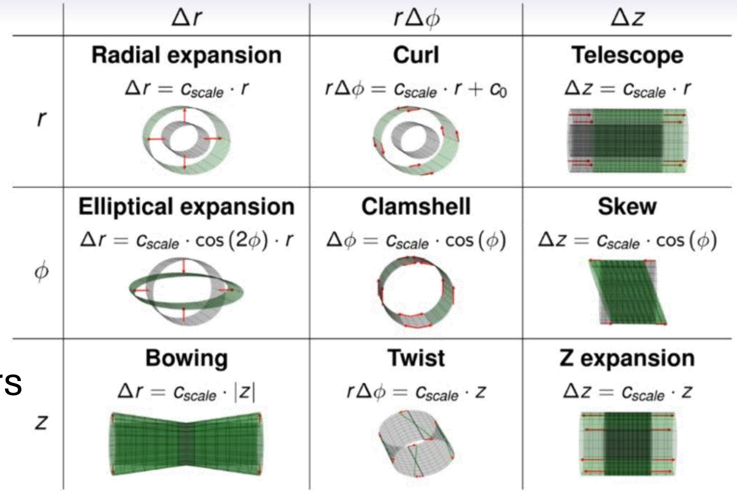
- Unaligned detectors show up to hundreds of μm shifts
  - Essential for maintaining vertex and tracking resolution required for Belle II physics
- Detector positions change due to vibrations, temperature fluctuations, and mechanical shifts



Alignment Monitoring and Results

Challenges

- Misalignments
- Weak Modes
- Deformations

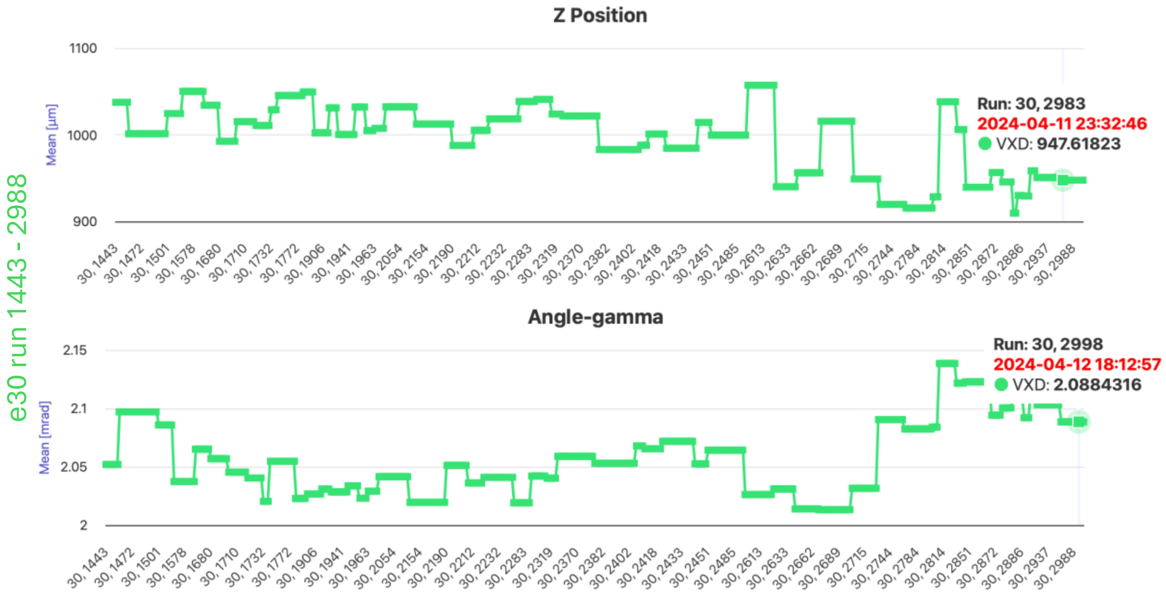


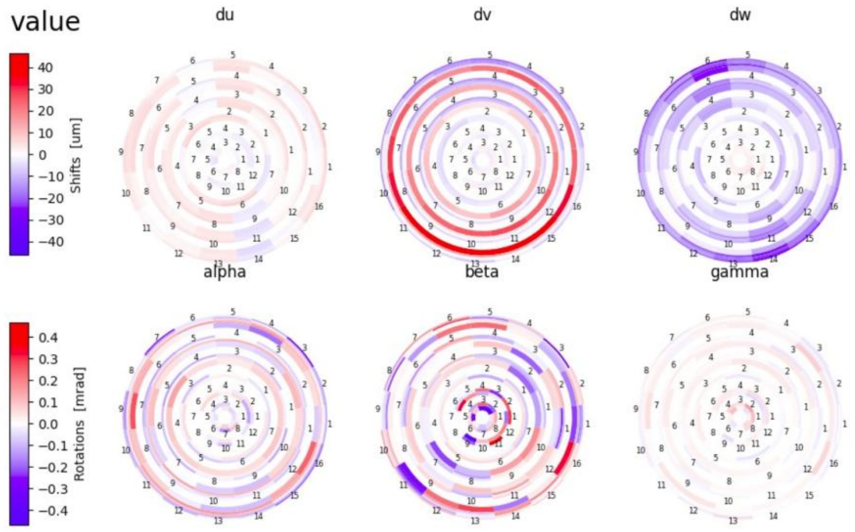
Track-based alignment method

- Performed using Millepede II and GBL track model
- Simultaneous global fit of rigid-body DOFs, surface shapes, and time-dependent parameters

Alignment data

- Cosmic-ray muons with B-field off/on
- Collision events: dimuons, hadronic events





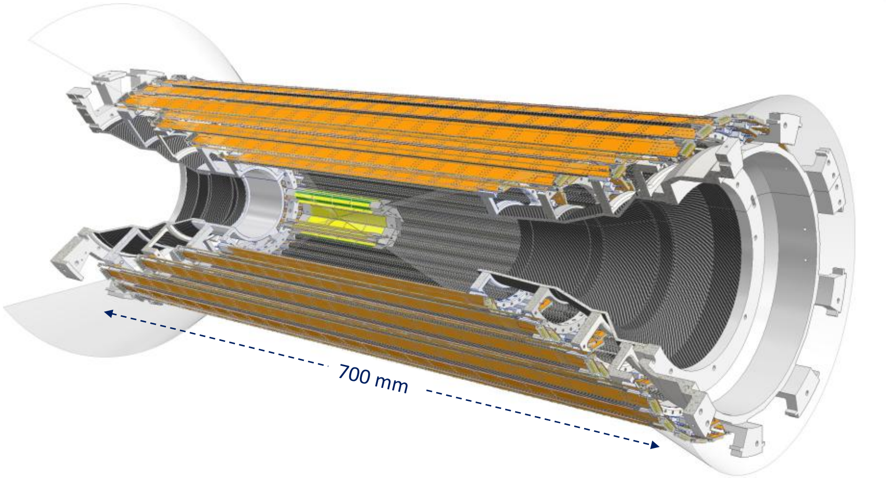
Upgrade Proposal VXD → VTX

ref: arXiv:2406.19421

Why upgrade of the Belle II detector is required:

To Aim towards:
$\mathcal{L} = 6 \times 10^{35} \text{cm}^{-2}\text{s}^{-1}$
$\int \mathcal{L} dt = 50 \text{ ab}^{-1}$

- Handle increased backgrounds and occupancy at target luminosity
- Improve radiation tolerance and ensure long –term detector performance
- Adapt to possible new interation region re-design

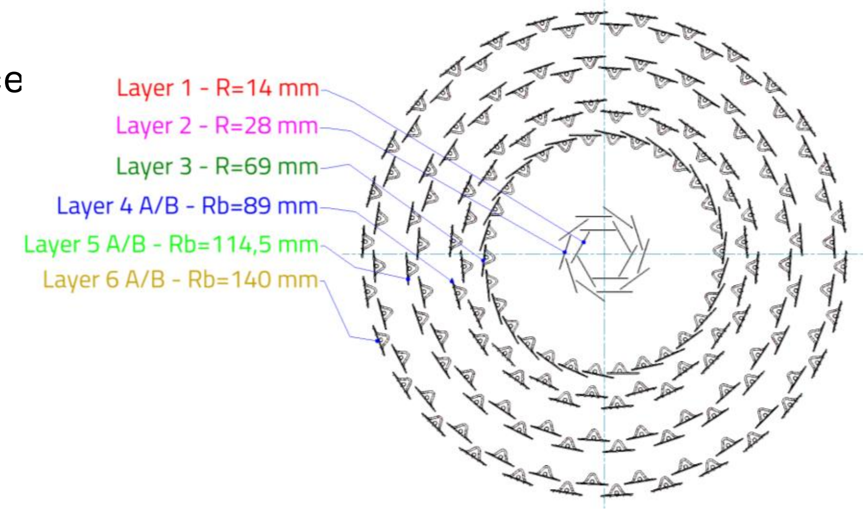


A new vertex detector concept VTX is proposed

- A new fully pixelated CMOS detector to replace the VXD
- Improved tracking resolution and space-time granularity
- Reduced material budget ≈ 3% X_0 instead of 3.8% X_0 (sum of all layers)
- 6 straight layers with Depleted Monolithic Active CMOS Pixel Sensors (DMAPS) proce

VTX Design

- L1 and L2 (iVTX): Inner layers
- L3 to L6 (oVTX): Outer layers

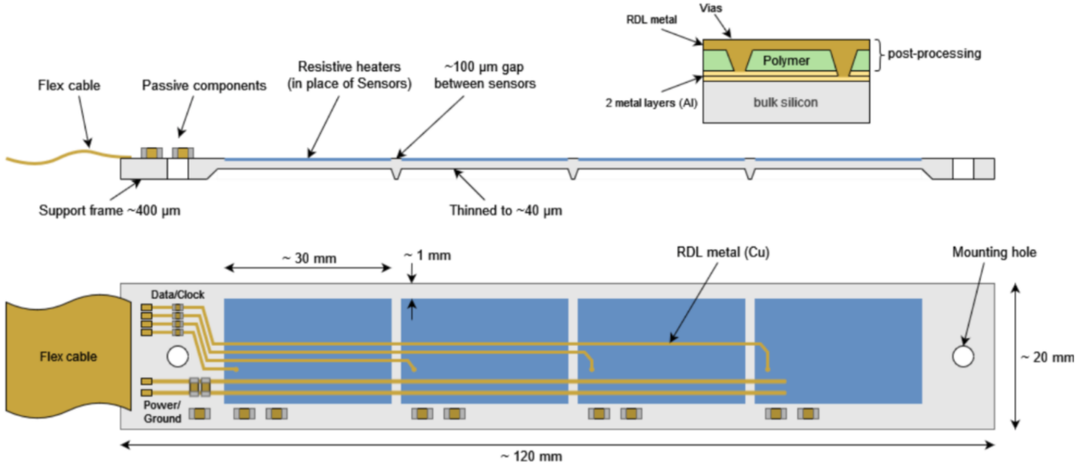


Installation of the upgraded detector is targeted during the upcoming long shutdown planned in 2032

Structure and Layer Information

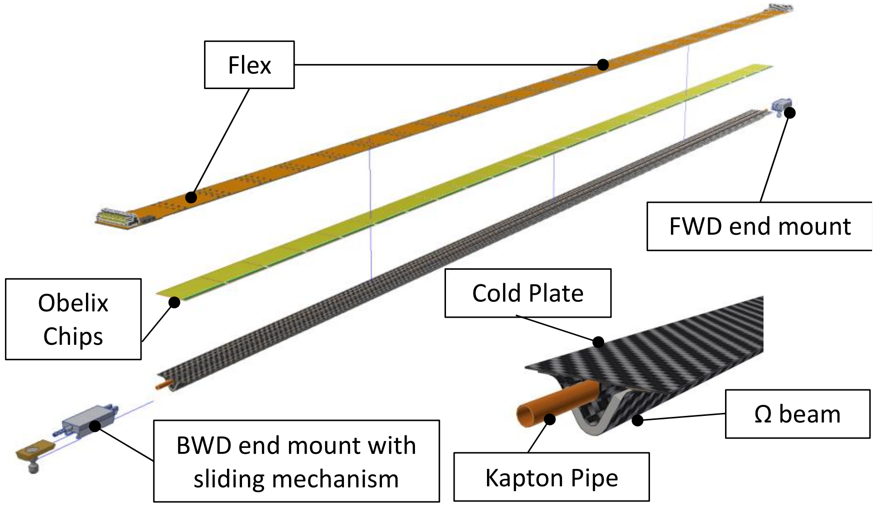
iVTX Inner Layers Concept

- 4 contiguous sensors diced as a block from the wafer
- Flex print cables
- Redistribution layer for interconnection
- Heterogeneous thinning for thinness and stiffness
- Several cooling options under evaluation: thermal conduction with thermal pyrolytic graphite, liquid cooling in Al -thin pipes



oVTX Outer Layers Concept

- Ladder structure design inspired by ALICE ITS2, composed of:
  - Carbon Fiber support structure
  - Cold – plate with pipes for liquid coolant circulation
  - Chip and Flex circuit for power and signal glued on top



	L1	L2	L3	L4	L5	L6	Unit
Radius (mm)	14.1	22.1	62.5/69.0	82.5/89.0	108/114.5	133.5/140	mm
# Ladders	6	10	30	36	48	60	
# Sensors per ladder	4	4	12	16	20	24	per ladder
Mat budget (% X0)	0.3	0.3	0.6	0.6	0.6	0.6	% X0
Expected hit rate* (MHz/cm2)	21	9	0.68	0.45	0.25	0.17	MHz/cm2

**Large uncertainty on BG extrapolation/possible changes in IR region*

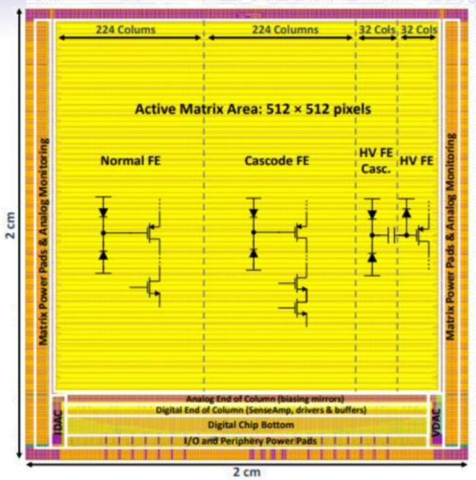
A same monolithic CMOS pixel sensor chip for all layers : Optimized Belle II pIXel sensor (OBELIX)

VTX Sensors: TJMP2 & OBELIX Overview

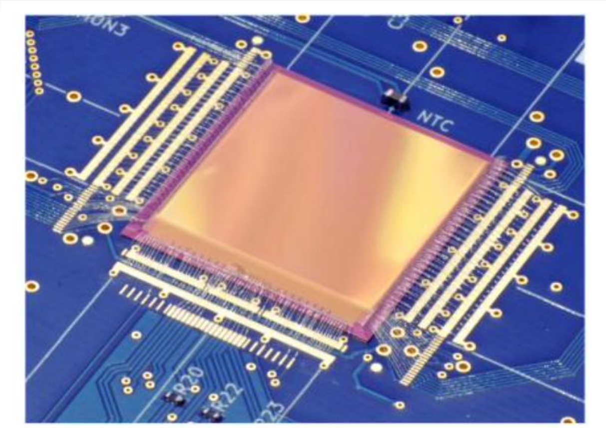
TJ-Monopix2 (TJMP2)

Developed for the ATLAS ITK as a DMAPS using Tower 180 nm CMOS, modified for rad-hardness & faster readout (good at high fluence at low temps), FE derived from ALPIDE

- Pixel & Matrix Specs:
  512×512 pixels (2×2 cm^2), pitch 33.04×33.04 μm^2, 7-bit ToT, 3-bit threshold tuning, thicknesses ~30 μm (epi/CZ-bulk)
- Readout Architecture:
  Column-drain R/O for >120 MHz/cm^2, triggerless in TJMP2, 25 ns integration.
- Front-End Flavors:
  4 variants in amplifier & coupling (AC/DC) for rad environments



Layout of TJMP2 sensor: divided in 4 regions with different FE



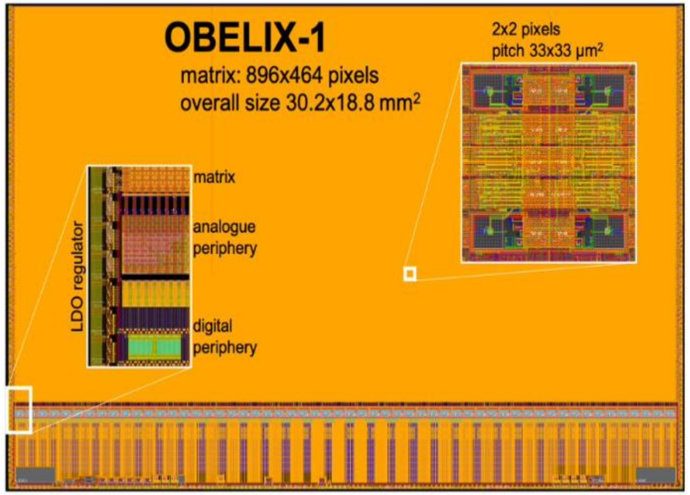
TJM2 sensor bonded on a test board

OBELIX

Optimized Belle II pIXel sensor

- Based on Tower Semiconductor 180 nm CMOS & TJMP2 design + new digital periphery
- Designed for high hit rates (120 MHz/cm^2) with strong radiation tolerance (TID 100 MRad, NIEL 5×10^{14} n_{eq}/cm^2)
- High performance with <15 μm spatial resolution, <200 - 300 mW/cm^2 power consumption, for hit rate from few to 120 MHz/cm^2 and <50 ns time stamping

First full-scale prototype (OBELIX-1) targeted for submission in **Winter 2025**



Current Status and Future Plan

Current Status

- Multiple beam tests (2022–2025) with 3–5 GeV electrons at DESY confirmed expected performance of non-irradiated and irradiated TJMP2 sensors

Irradiation Study (March 2025)

- Tested 3 p-irradiated and 1 e^--irradiated chips at NIEL fluences up to 5×10^{14} n_{eq}/cm^2
- Efficiency degrades with temperature, especially for AC-coupled FE
- DC-coupled remains > 99% efficient up to ~40 °C, AC-coupled dropped faster with temperature

Future Plans

- Continue testing and validation of TJMP2 and OBELIX sensors
- Finalize OBELIX design and production
- Aiming submission of first version of OBELIX sensor in winter 2025
- Continue R&D and engineering activities on cooling and ladder prototypes.
- Prepare technical design report in 2027
- Goal to integrate and commission the upgraded detector for high luminosity operation after long shutdown 2 in ~2032

Conclusion

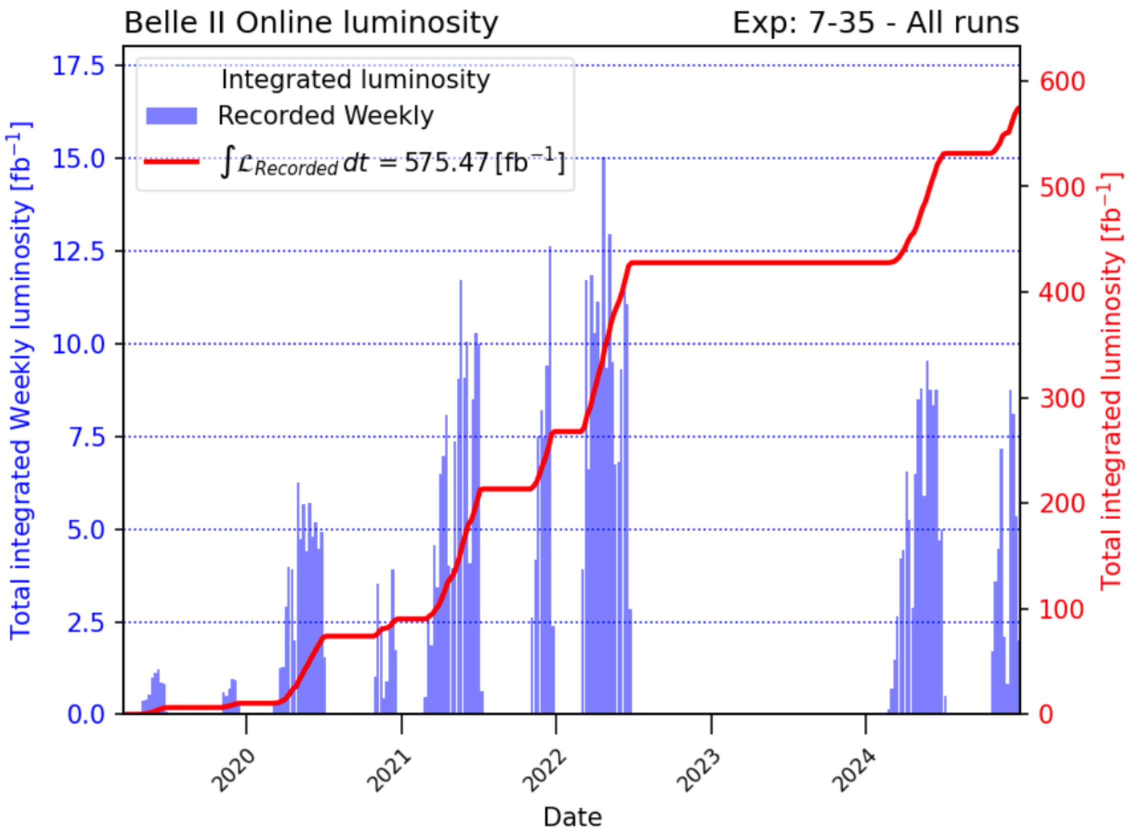
Current Status

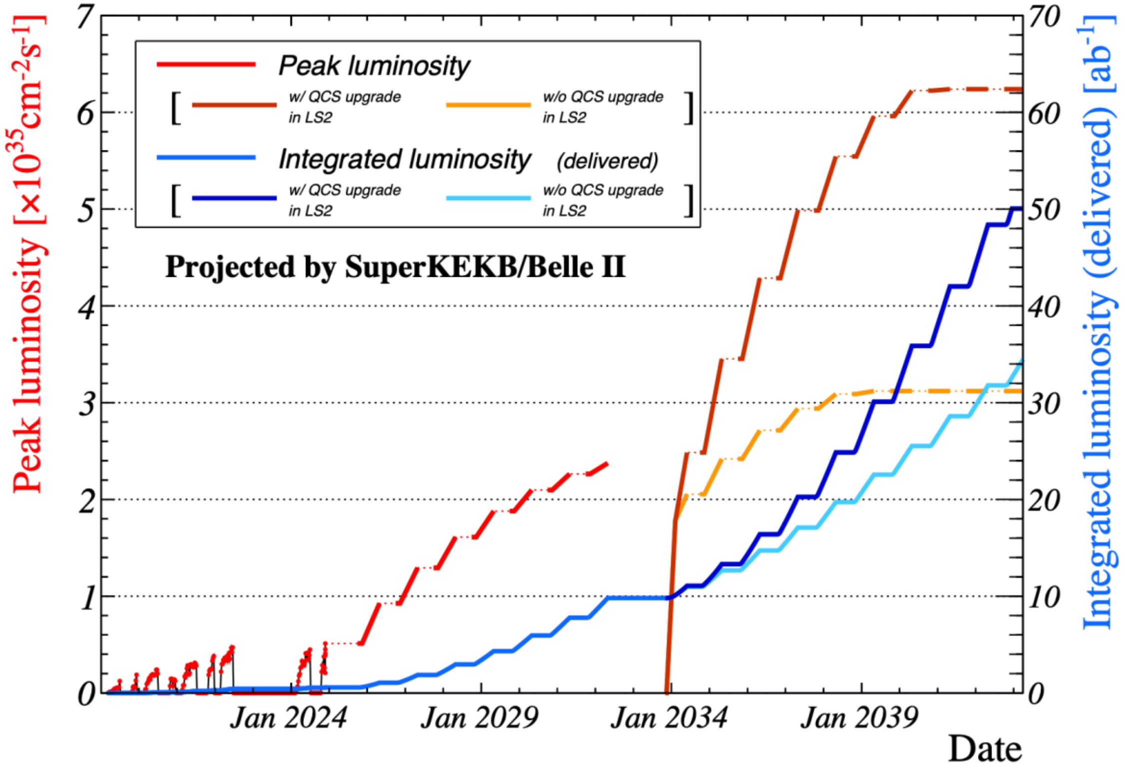
- Belle II is the only high energy/particle physics experiment to use a DEPFET-based pixel vertex detector
- PXD 1 running successfully (2019–2022) and PXD 2 showing stable performance in 2024, before sudden beam loss (SBL) events
- SVD continues to perform with >99% sensor efficiency, excellent signal-to-noise ratio, and minimal radiation-related degradation over multiple runs.
- Alignment systems and monitoring procedures ensure optimal vertex resolution for precise CP violation and lifetime measurements.
- VTX: Beam test and irradiation studies confirm that TJMP2 and OBELIX sensor designs meet performance expectations

Future plan

- Investigate sudden beam loss (SBL) events and implement enhanced fast-shutdown systems to safeguard the PXD
- Maintain and optimize the SVD performance under increased luminosity by developing new algorithms
- Complete the OBELIX sensor design, submit the first full-scale prototype by winter 2025
- Prepare for the major Belle II upgrade around 2032, featuring a fully pixelated CMOS-based vertex detector, VTX

Luminosity status

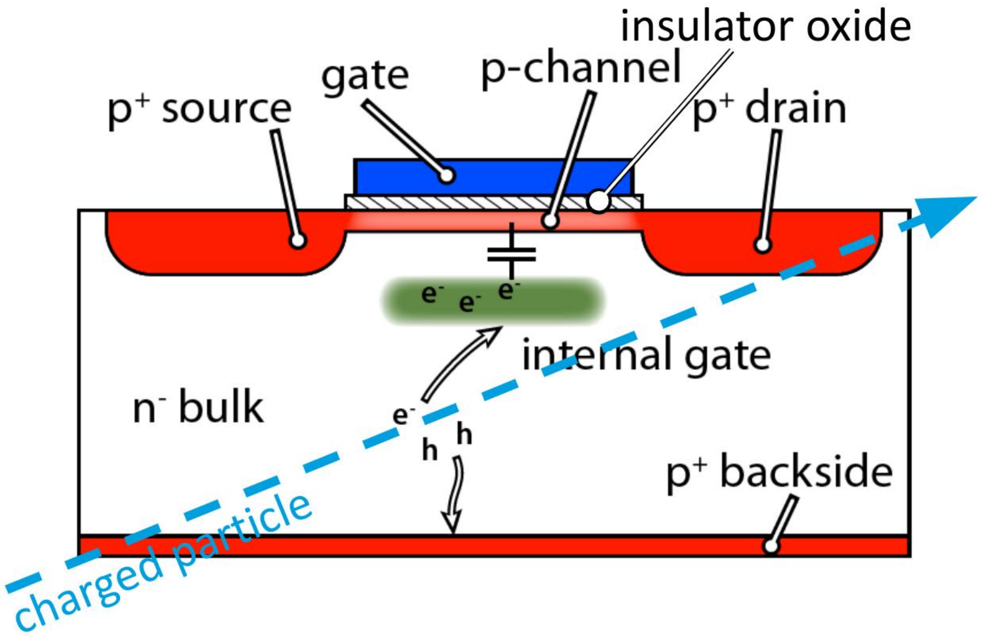




DEPFET sensor principle

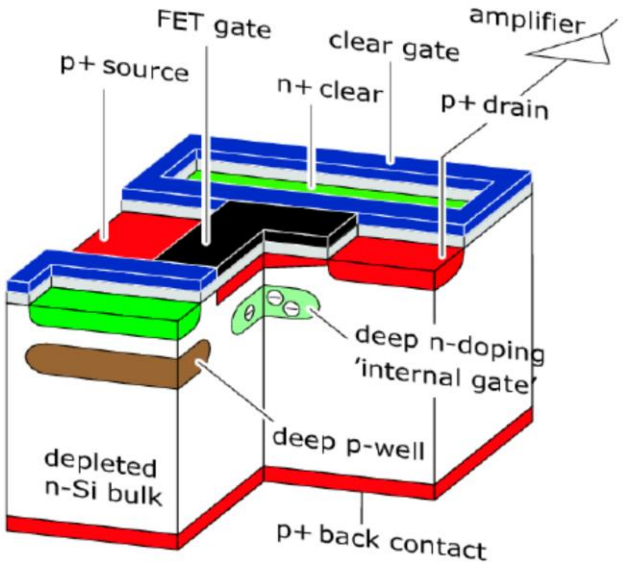
How it works

- A Field Effect Transistor (FET) is built directly into a fully depleted silicon bulk.
- The internal gate (a deep n-implant beneath the channel) collects signal electrons, which in turn modify the source–drain current.
- After readout, the stored charge is removed through an n+ implant using a punch-through reset mechanism.



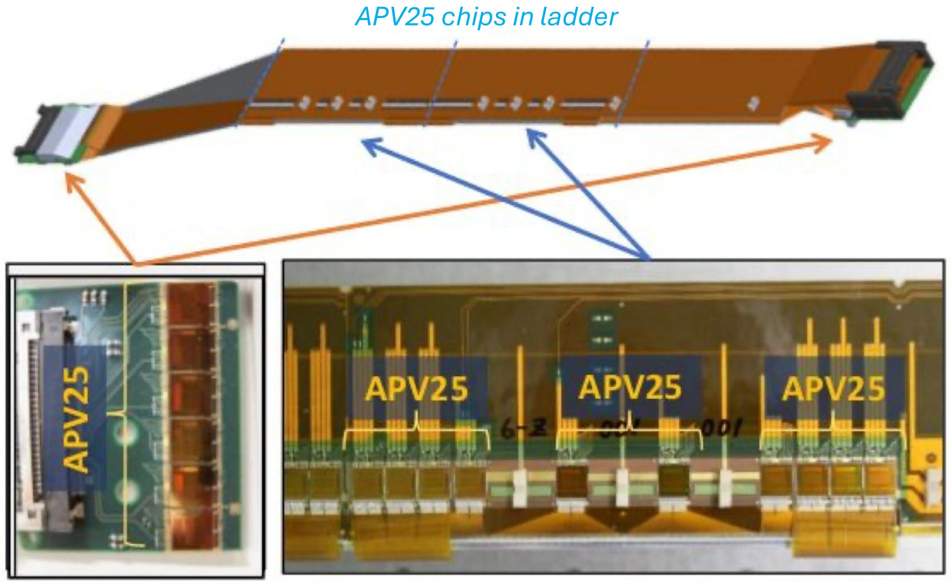
Why it's Important

- Fast response
  - charges are collected within nanoseconds
- ensuring excellent signal-to-noise performance
- Low power and low mass
  - with only ~75 µm active thickness, the sensor adds minimal material to the tracker
- Non-destructive readout

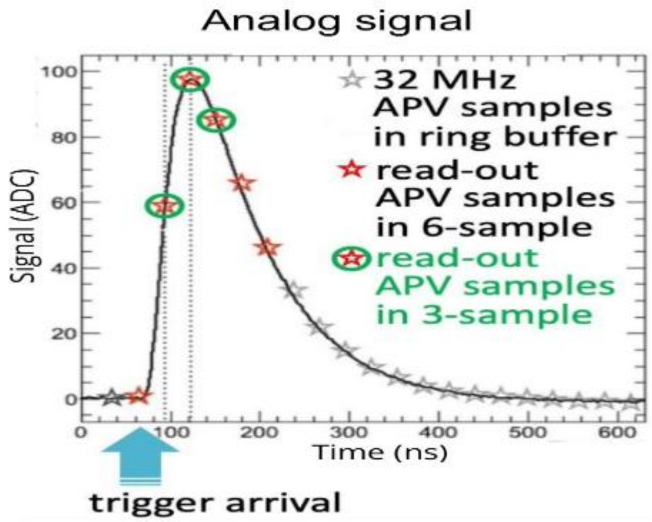


SVD Principle

- **APV25 readout Architecture**
  - 50 ns shaping time
  - 192-cell analog pipeline / 128 channels
  - 40 MHz clock, >100 Mrad tolerance, 0.4 W power

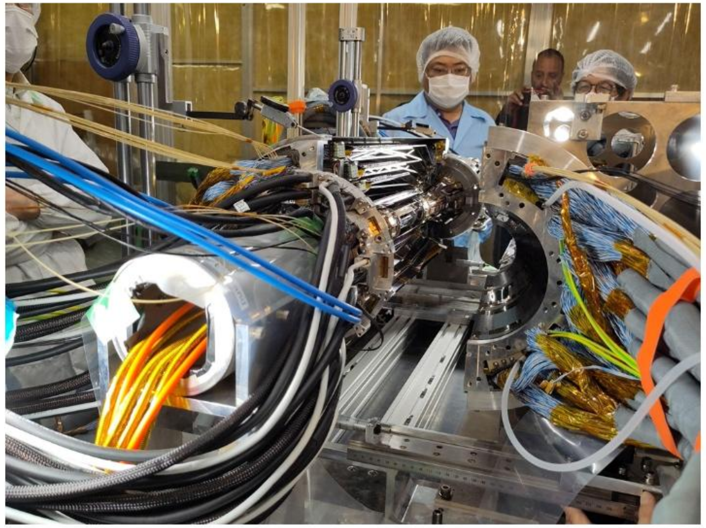


- **Operation mode**
  - Operated in multipeak mode @32 MHz (⅛ of SuperKEKB bunch crossing frequency of 254 MHz)
  - By default 6 samples of analog output are recorded to reconstruct output waveform
  - Alternative 3/6 mixed mode tested for high-luminosity to reduce data size

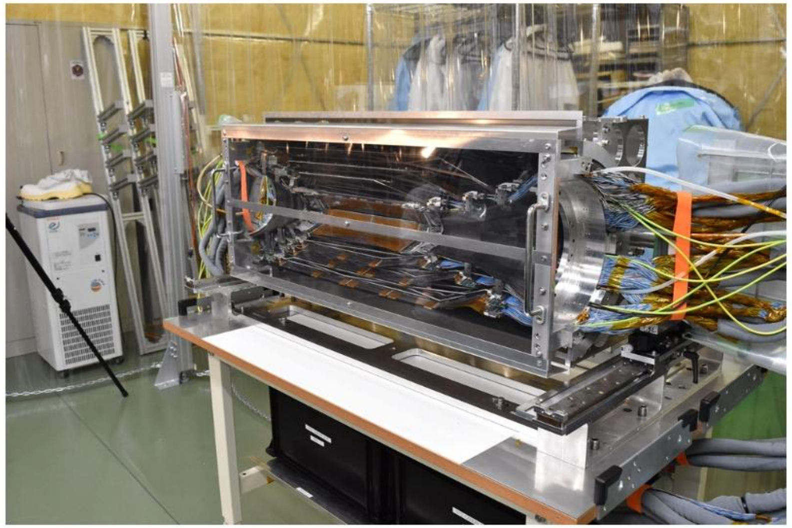


SVD During long shutdown

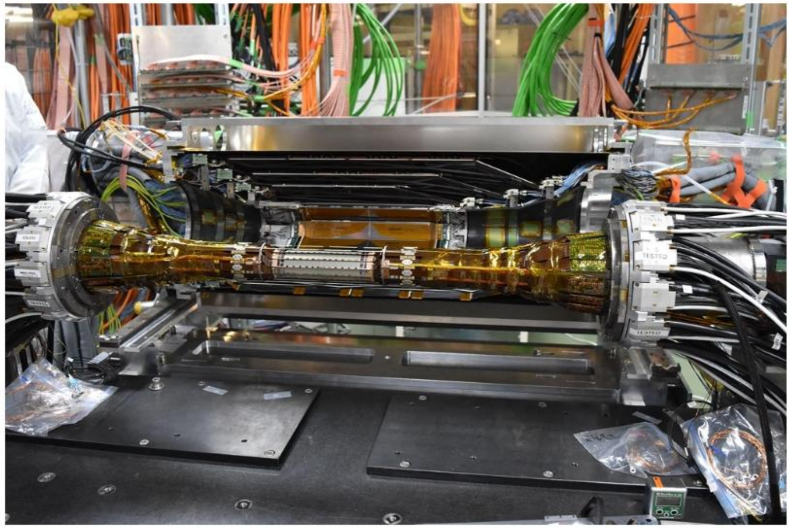
Opening the VXD



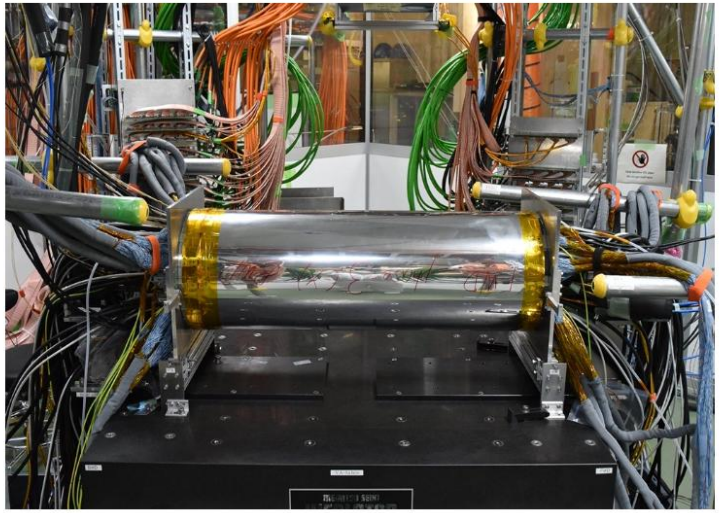
SVD Half



PXD insertion



Completed VXD



Towards Belle II

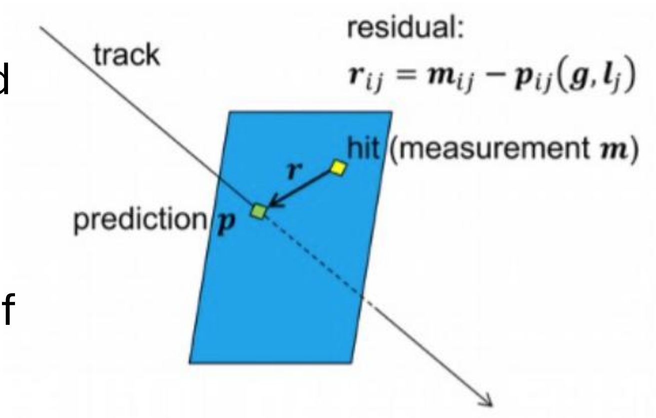
Reinstalling

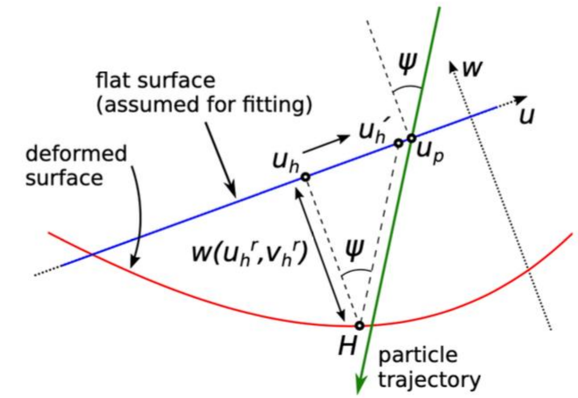
Misalignment Procedure

- The procedure uses residual between measured and expected positions of hits:

$$r_{ij}(\boldsymbol{\tau}_j, \boldsymbol{a}) = u_{ij}^m - u_{ij}^p(\boldsymbol{\tau}_j, \boldsymbol{a})$$

- τ_j is vector of track parameters and *a* is vector of alignment parameters.





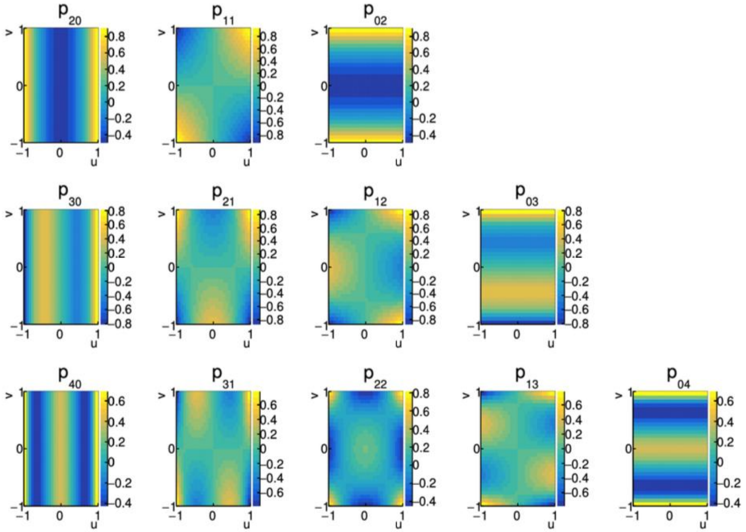
A charged track crosses the real deformed sensor surface

- For alignment purpose χ2 function is defined as:

$$\chi^2(\boldsymbol{\tau}, \boldsymbol{a}) = \sum_j^{\text{tracks}} \sum_i^{\text{hits}} \left(\frac{r_{ij}(\boldsymbol{\tau}_j, \boldsymbol{a})}{\sigma_{ij}} \right)^2$$

$$\approx \sum_j^{\text{tracks}} \sum_i^{\text{hits}} \frac{1}{\sigma_{ij}^2} \left(r_{ij}\left(\boldsymbol{\tau}_j^0, \boldsymbol{a}^0\right) + \frac{\partial r_{ij}}{\partial \boldsymbol{a}} \delta \boldsymbol{a} + \frac{\partial r_{ij}}{\partial \boldsymbol{\tau}_j} \delta \boldsymbol{\tau}_j \right)^2$$

- **Millepede II** algorithm: Minimizes χ^2 with respect to alignment and track parameters simultaneously.

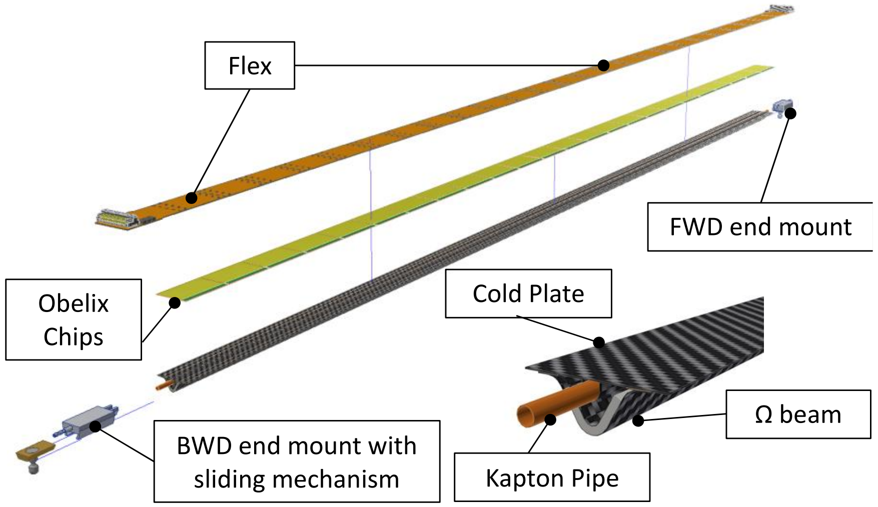


Base 2D Legendre polynomials corresponding to the decomposition coefficients and alignment parameters pij

VTX Design and Performance Details

VTX Design Specifics

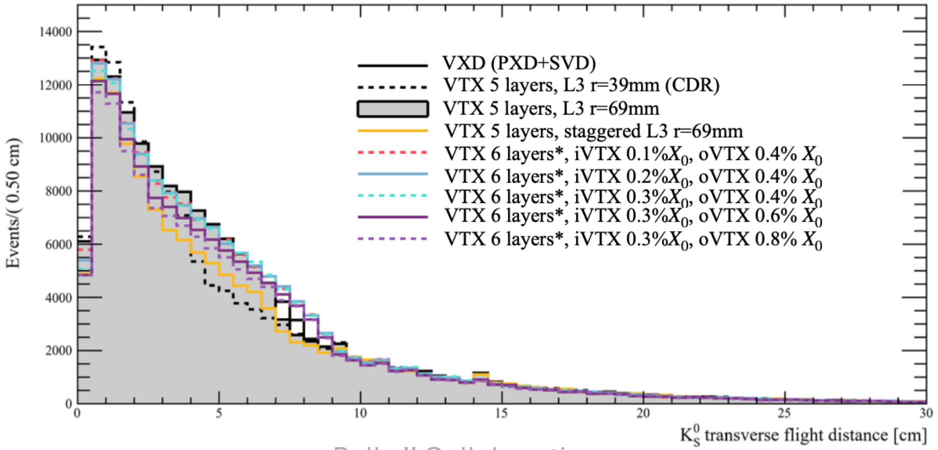
- **iVTX (L1-L2)**
  - All-silicon module with 4 OBELIX sensors diced as a block (50 μm thin, ~400 μm border for stiffness)
  - Cooling
    - liquid cooling in Al-pipes ~0.4% X_0/ladder
    - thermal conduction with Thermal Pyrolytic Graphite ~0.3% X_0/ladder
- **oVTX (L3-L6)**
  - ladder design (carbon fiber Ω-beam + liquid-cooled cold-plate)



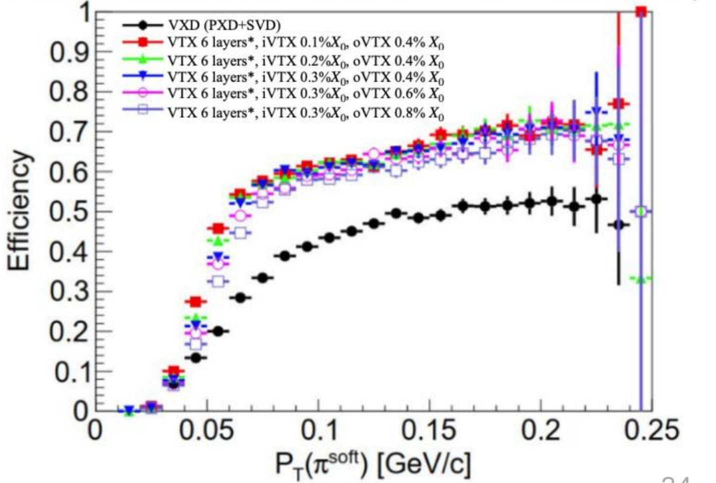
Studied reconstruction efficiency (K_S and slow π):

- Improved tracking efficiency
- Enhanced vertex resolution

K_S^0 reconstruction efficiency (from $B^0 \rightarrow J/\Psi + K_S^0$)



Soft π reconstruction (from $B^0 \rightarrow (D^0 + \pi^-) + \mu^+\nu_\mu$)



TJMP2 beam tests (2022–2024) with 3–5 GeV

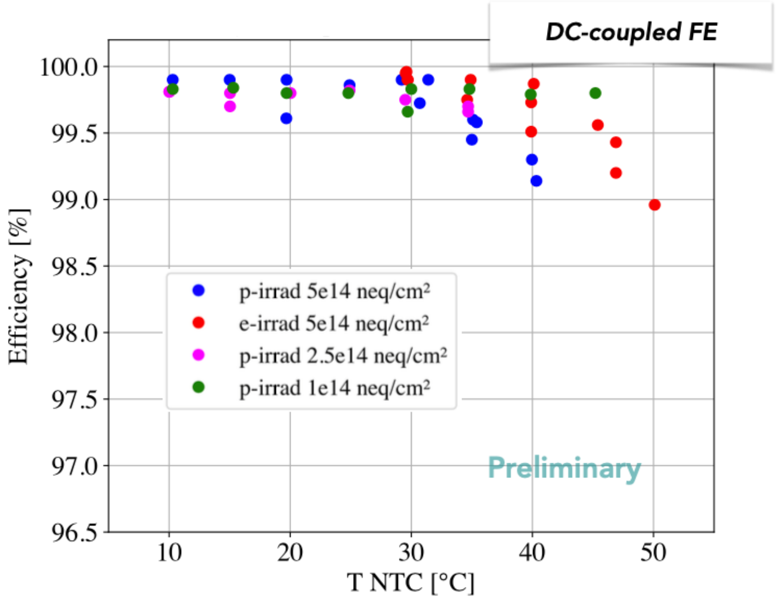
- **2022**: non-irradiated sensors achieved ~99% efficiency, ~9 μm resolution
- **2023**: irradiated (5×10^{14} n_{eq}/cm^2 protons): >99% efficiency (DC-coupled 99.99%, AC-coupled 98-99%).
- **2024**: high fluence/TID, DC-cascode >99.5% efficiency. threshold/noise rises above 40°C, e^--irradiation less damaging, tuning less effective at high temps

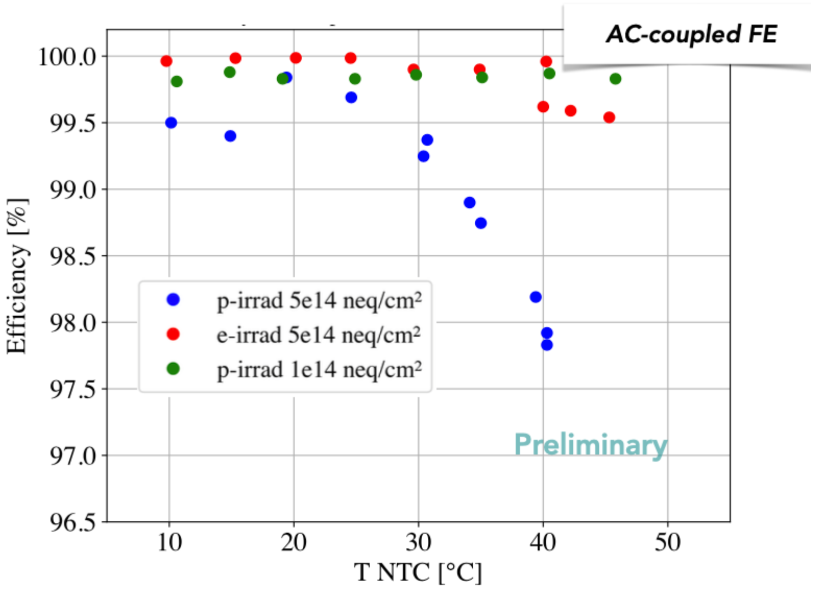
TJMP2 Test Beam 2025

- Efficiency degrades with temp, especially for AC-coupled FE, DC-coupled remains >99% efficient up to T_{NTC} ~40 °C
- Operation above 40 °C is challenging due to increased leakage current and noise

TJMP2 Test Beam 2025

$T_{Chip} \sim T_{NTC} + 7°C$





Efficiency vs Temperature for same FE settings