



Aug 28, 2025

FERMILAB-SLIDES-25-0198-CMS

# Precision timing in CMS at the HL-LHC

## *Current progress on validation and production*

**Murtaza Safdari, for the CMS MTD Collaboration**

Vertex 2025: 33rd International Workshop on Vertex Detectors

[Link to Indico](#)



U.S. DEPARTMENT  
of **ENERGY**

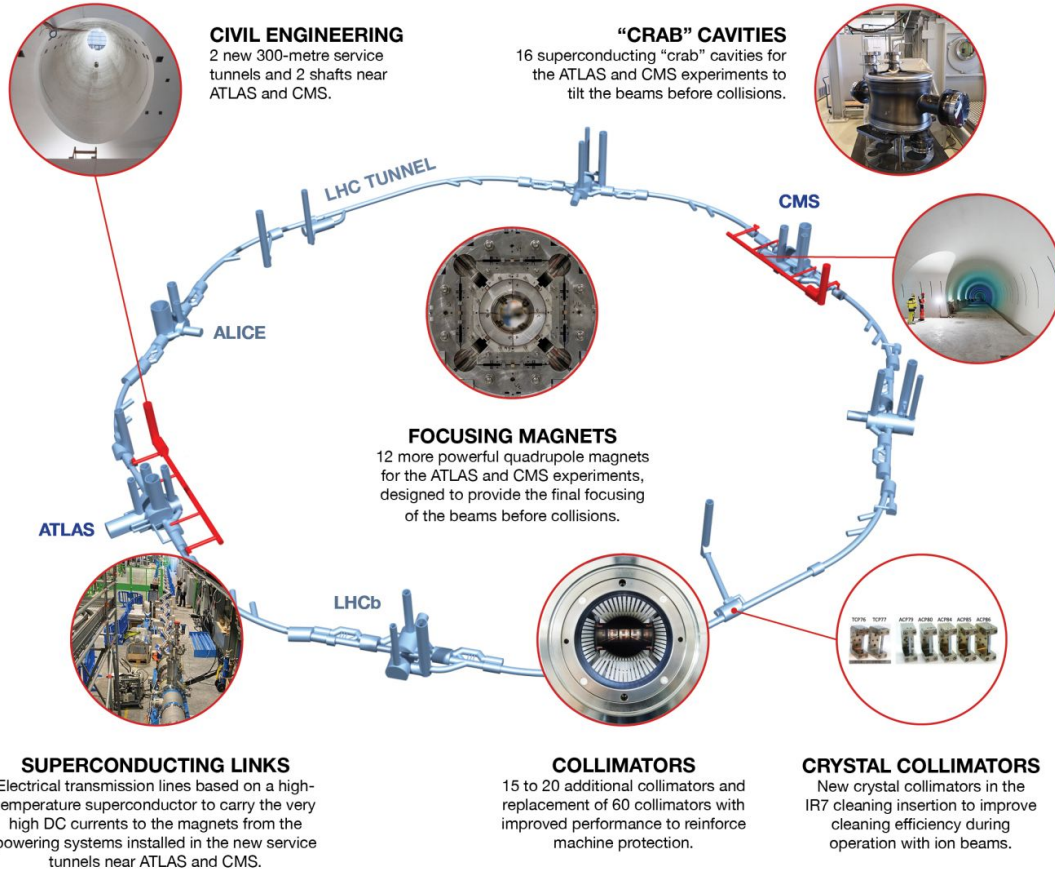
Fermi National Accelerator Laboratory is managed by  
FermiForward for the U.S. Department of Energy Office of Science



# The Need for Precision Timing at the HL-LHC

## How do we handle up to 200 interactions per bunch crossing?

### NEW TECHNOLOGIES FOR THE HIGH-LUMINOSITY LHC



Source

**Trigger/HLT/DAQ**

- Track information in L1-Trigger
- L1-Trigger: 12.5  $\mu$ s latency – output 750 kHz
- HLT output 7.5 kHz

**Barrel ECAL/HCAL**

- Replace FE/BE electronics
- Lower ECAL operating temp. (8 °C)

**Muon Systems**

- Replace DT & CSC FE/BE Electronics
- Complete Muon coverage in region  $1.5 < \eta < 2.4$

**New Endcap Calorimeters**

- High granularity
- 3D capable

**New Tracker**

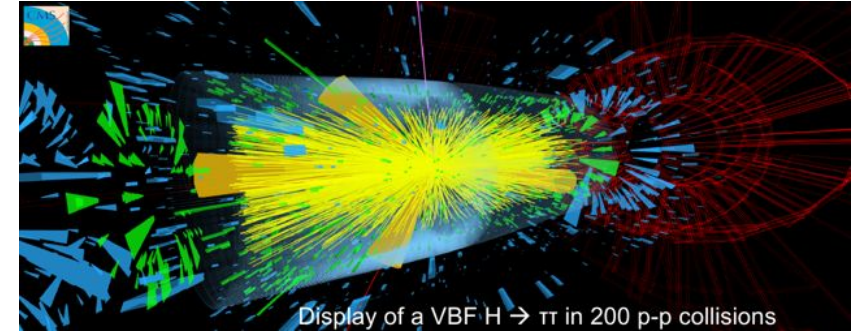
- Rad. tolerant – high granularity – significant less material
- 40 MHz selective readout ( $p_T > 2$  GeV) in Outer Tracker for L1-Trigger
- Extended coverage to  $\eta=4$

**New Precision Timing Detector**

- Barrel: Crystal +SiPM
- Endcap: Low Gain Avalanche Diodes

Source

Source

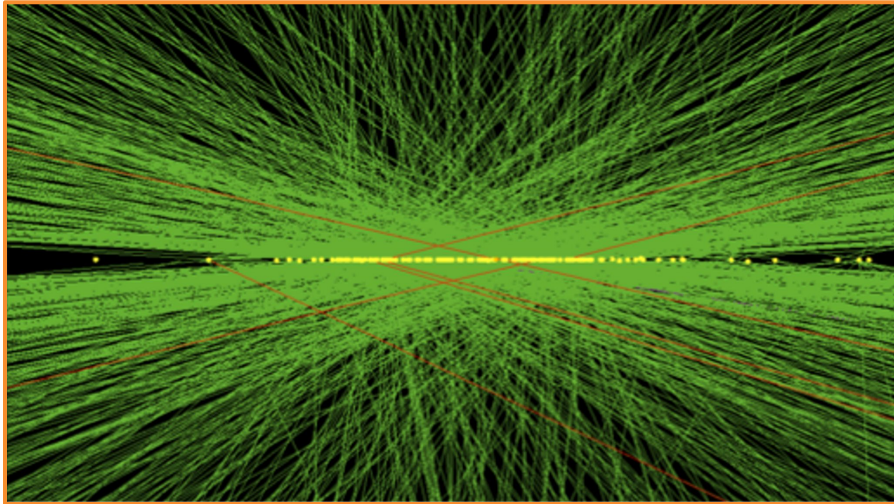


CERN February 2024



# The Need for Precision Timing at the HL-LHC

How do we handle up to 200 interactions per bunch crossing?



High Luminosity LHC comes with 4-5x more PU interactions per bunch crossing

Overlapping vertices in space will present limitations for PU track identification

**Trigger/HLT/DAQ**

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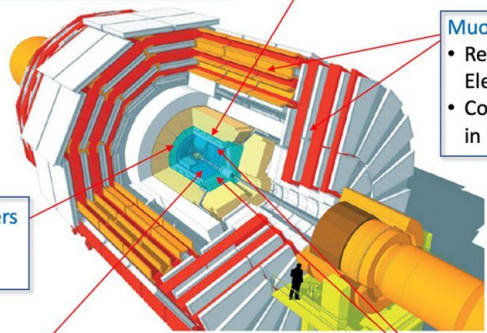
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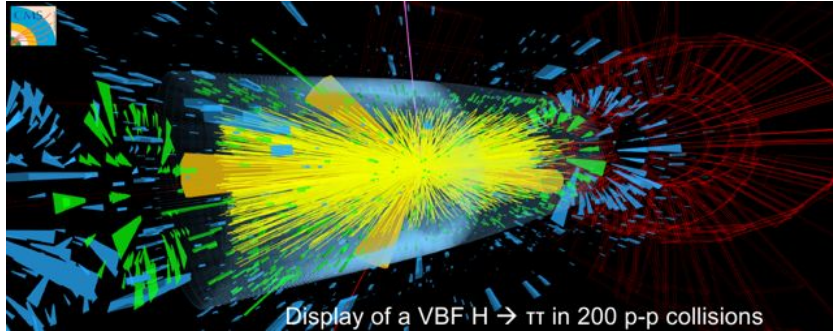
**New Precision Timing Detector**

- Barrel: Crystal +SIPM
- Endcap: Low Gain Avalanche Diodes



Source

Source

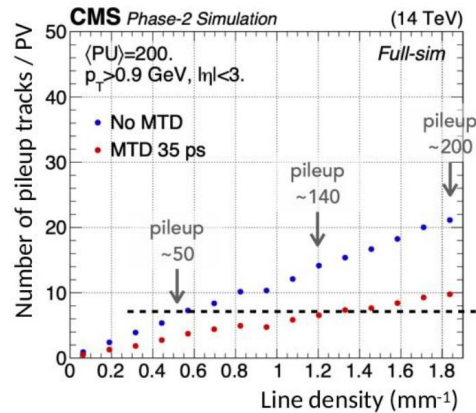
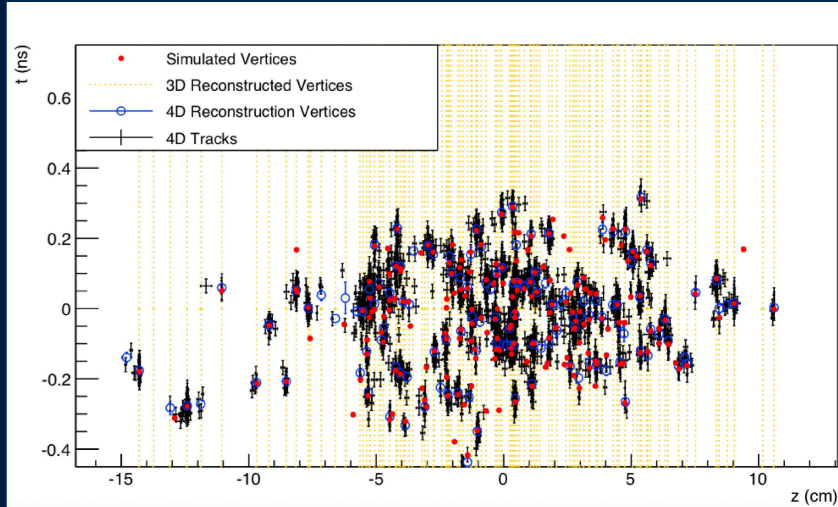


Display of a VBF  $H \rightarrow \pi\pi$  in 200 p-p collisions



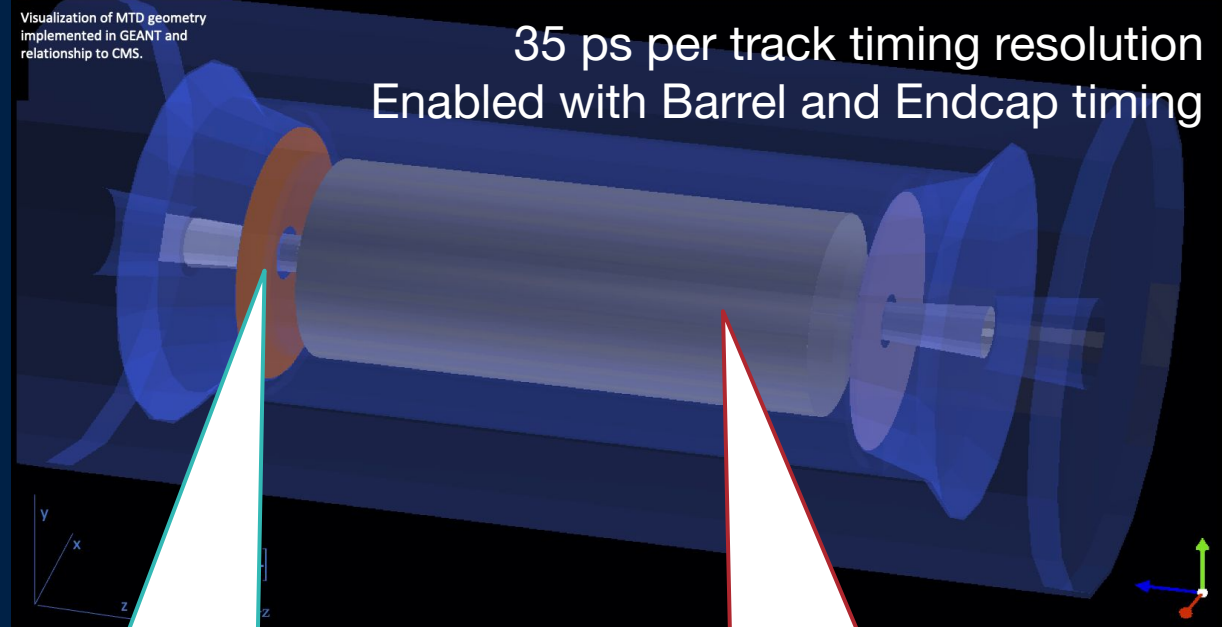
# CMS Minimum Ionizing Particle Timing Detector

First generation timing detector being deployed at the HL-LHC



The MTD will exploit timing information to reduce pile-up to current LHC level in both the forward and barrel regions.

[CMS-TDR-020](#)



## Endcap Timing Layer (ETL)

### Si with internal gain (LGAD):

- On the CE nose:  $1.6 < |\eta| < 3.0$
- Radius:  $315 < R < 1200$  mm
- Position:  $z = \pm 3.0$  m
- $1.3 \times 1.3$  mm<sup>2</sup> pixels
- Area **14 m<sup>2</sup>**: 8.5M channels
- Fluence: max **2E15 n<sub>eq</sub>/cm<sup>2</sup>**

## Barrel Timing Layer (BTL)

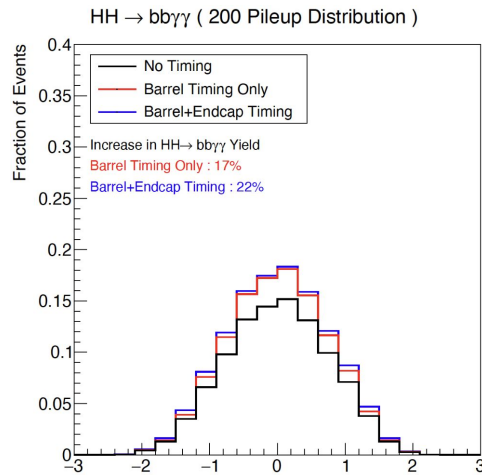
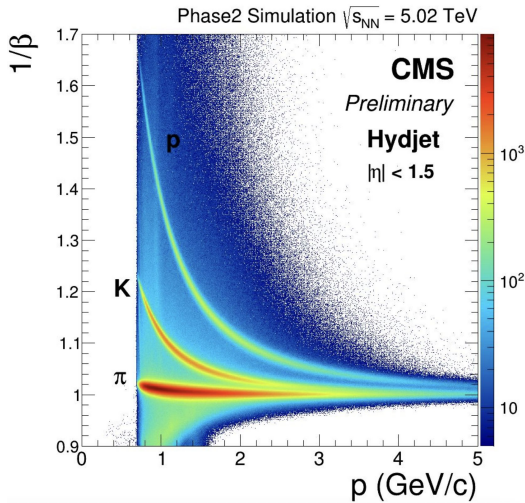
### LYSO:Ce bars + SiPM readout:

- TK/ECAL interface:  $|\eta| < 1.45$
- Inner radius: 1148 mm
- Thickness: 40 mm
- Length:  $\pm 2.6$  m along z
- Area **38 m<sup>2</sup>**: 332k channels
- Fluence: max **2E14 n<sub>eq</sub>/cm<sup>2</sup>**

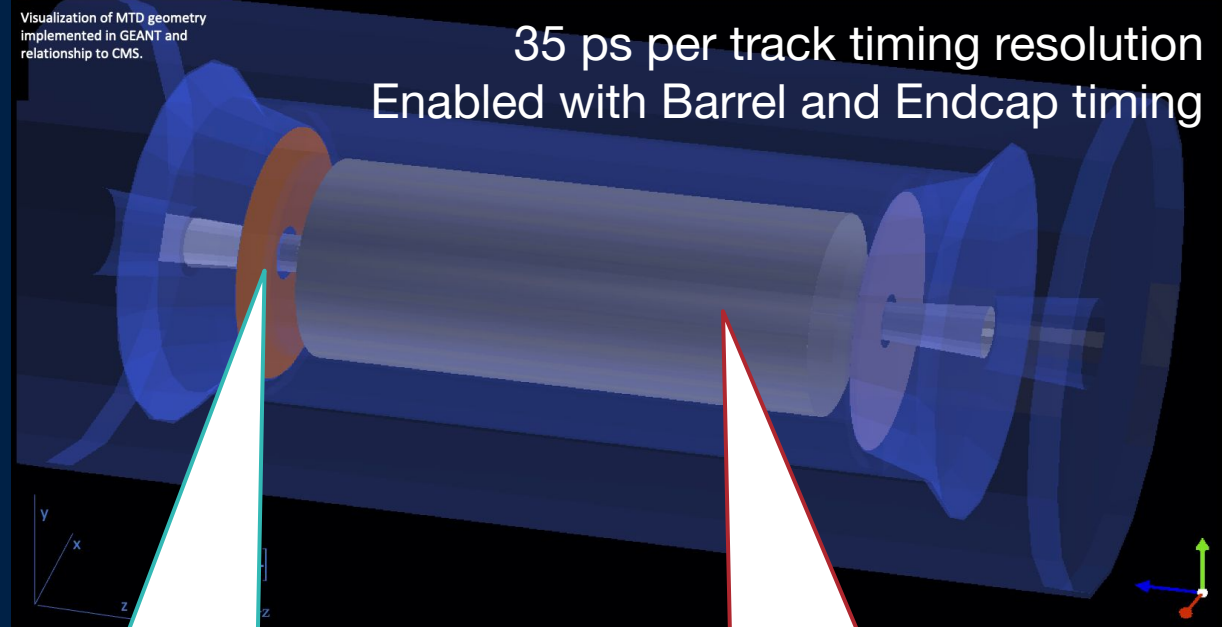


# CMS Minimum Ionizing Particle Timing Detector

First generation timing detector being deployed at the HL-LHC



CMS-DP-2022-025<sup>y<sub>HH</sub></sup>



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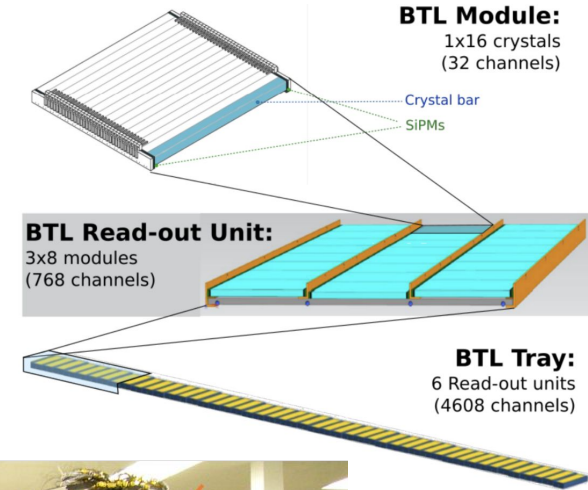
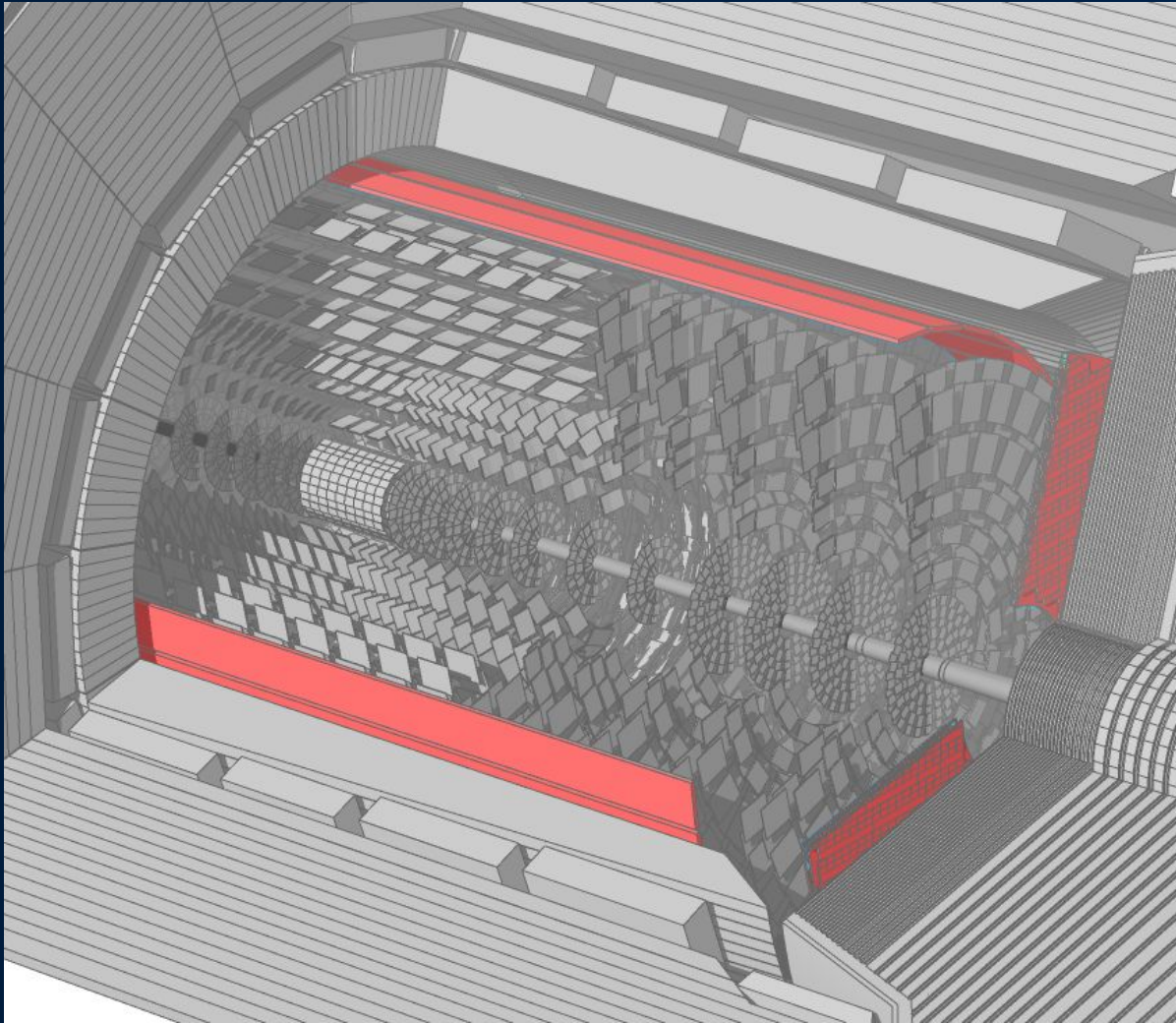
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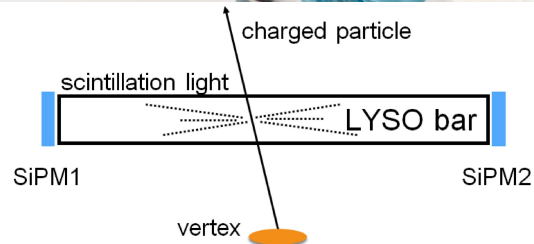
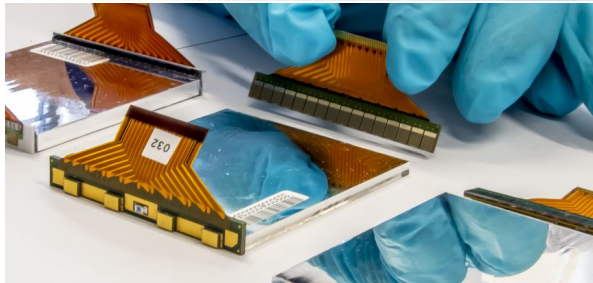
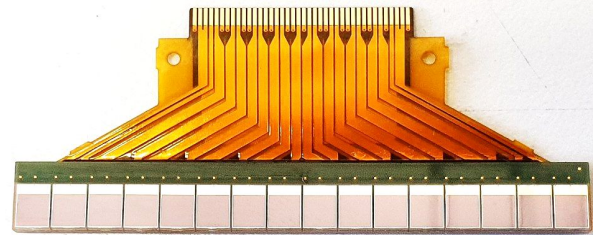
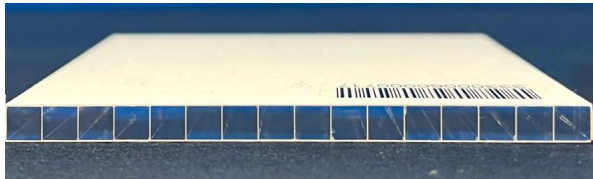
Inner R: 1.148 m, Depth: 40 mm, L:  $\pm 2.6$  m along z,  $|\eta| < 1.45$ , 38 m<sup>2</sup>:  $\sim 332$ k channels





# CMS Barrel Timing Layer

## Sensor and ASIC



(Lutetium-Yttrium Oxyorthosilicate doped with Cerium) **LYSO:Ce** crystals as scintillator

- Excellent radiation tolerance
- Bright (40k ph/MeV)
- Fast rise time  $O(100\text{ps})$ , decay time  $\sim 40\text{ ns}$

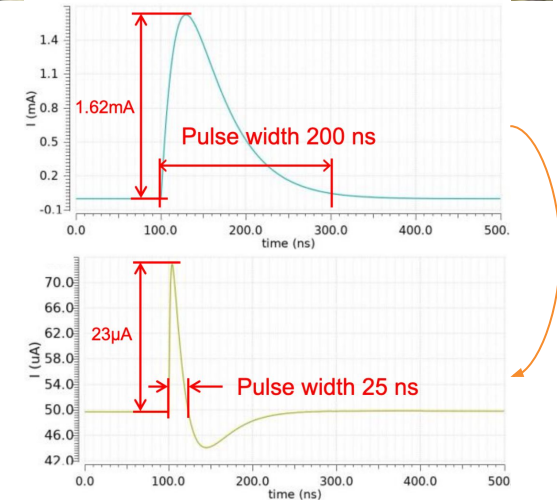
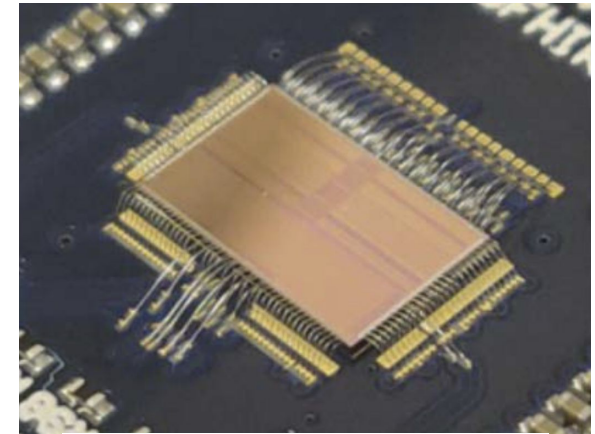
**Silicon Photomultipliers** as photo-sensors

- Compact, insensitive to B fields, fast
- High dynamic range, rad tolerant, good photo detection efficiency

Dedicated readout **TOFHIR2** ASIC, builds upon TOFPET ASIC with significant redesign for HEP in 130nm CMOS withstanding 3 MRad

Key feature is a noise suppression filter

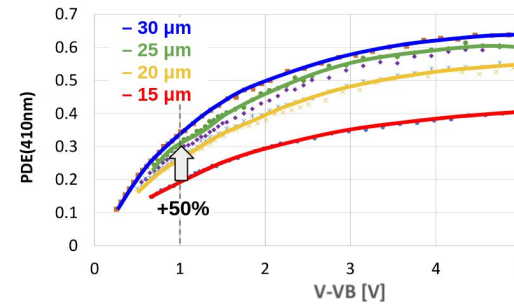
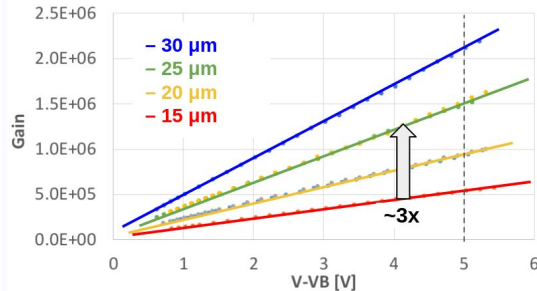
- Inverted and delayed pulse subtraction (**Differential Leading Edge Discriminator**)
- Restores baseline at the rising edge.
- Improves time resolution by about a factor 3 at end of life of the detector.





# CMS Barrel Timing Layer

Optimize signal amplitude, rise time, dark count rate for timing performance



$$\sigma_t = \sigma_t^{ele} \oplus \sigma_t^{phot} \oplus \sigma_t^{DCR} \oplus \sigma_t^{clock}$$

Electronic Noise term goes as rise-time/SNR  
 Photostatistics term goes as 1/root(amplitude)  
 Dark Count Rate term goes as root(DCR)/amplitude

**LYSO:Ce** bar geometry minimizes SiPM area wrt crystal volume:  $3.12 \times 3.75 \times 54.7 \text{ mm}^3$

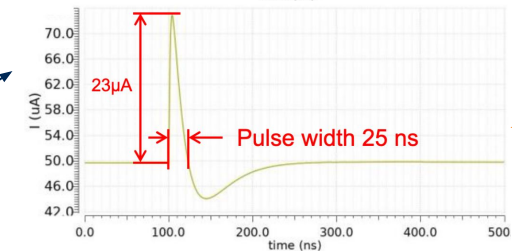
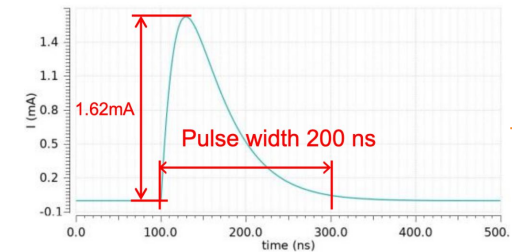
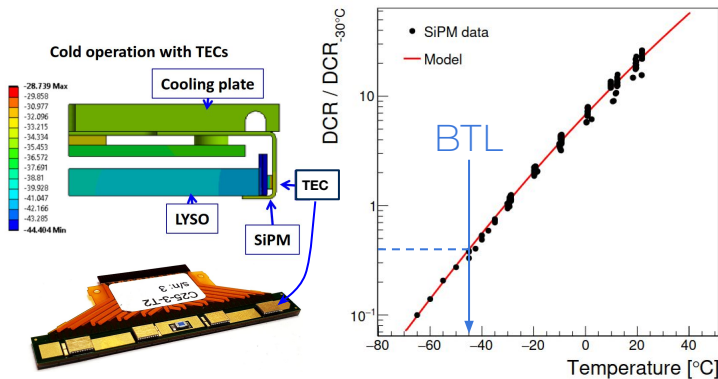
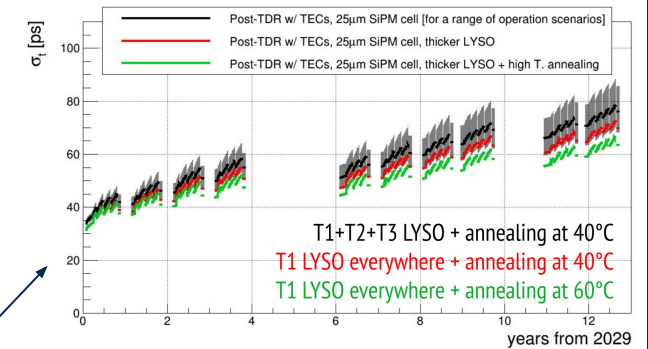
- **Thick** crystals used across the full BTL detector
- Optimized wrapping for improved light collection

**SiPM** gain, photodetection efficiency, and speed increased by using **25 μm cell size**

- **Operate at -45 C** (dual-phase CO<sub>2</sub> + Thermoelectric Cooling) to minimize DCR
- High temp **annealing at 60 C** to heal radiation damage over 3 ab<sup>-1</sup>

**TOFHIR2 Differential Leading Edge Discriminator** designed to reduce DCR from SiPM

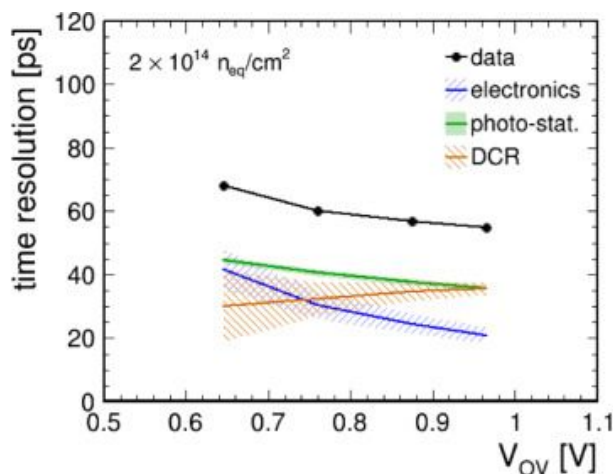
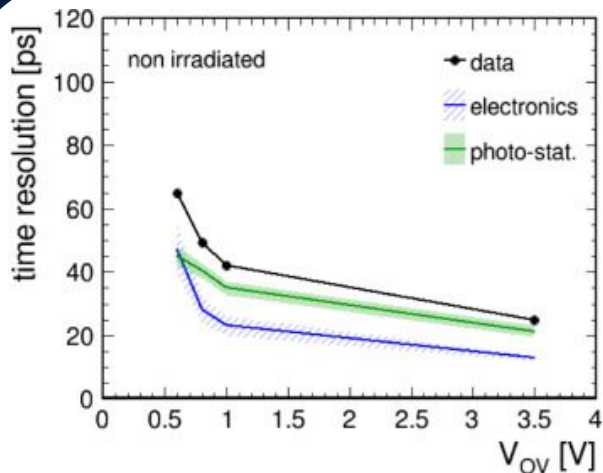
Increased preamp gain minimizes electronics noise





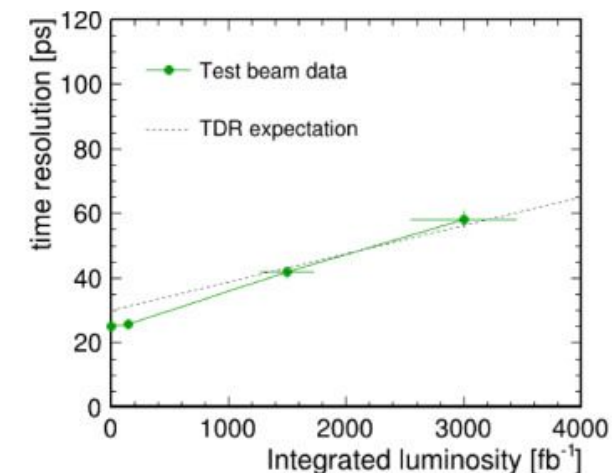
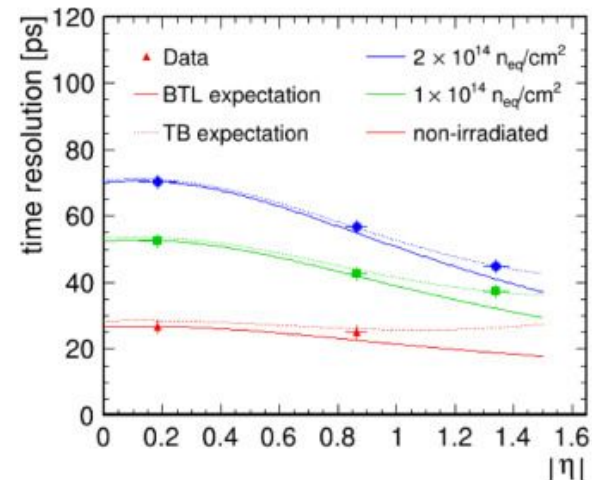
# CMS Barrel Timing Layer

## Beam Test Validation



- Test beams with modules before and after irradiation help validate the optimizations to LYSO:Ce, SiPM, and TOPHIR2
- DCR component becomes a significant factor after irradiation at end of life levels

- Scans with modules irradiated to different levels to simulate various stages of BTL aging during HL-LHC operations upto  $3 ab^{-1}$
- **Confirms operational requirement of BTL timing resolution 30-60 ps over the lifetime of the detector**



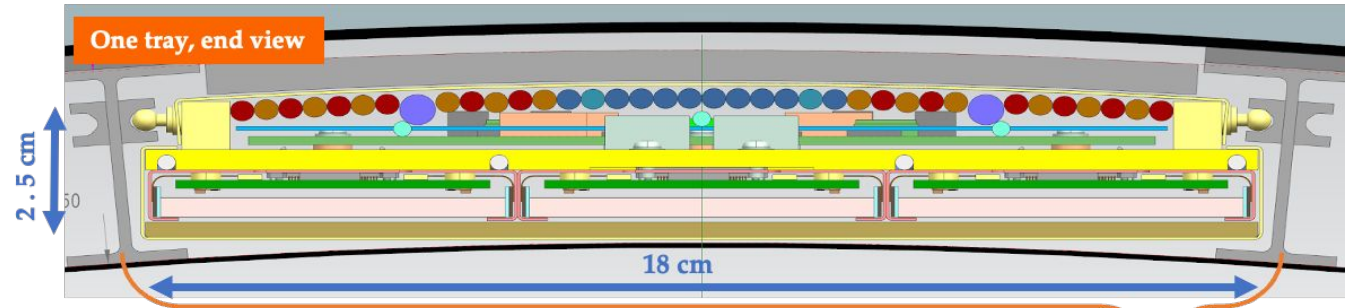


# CMS Barrel Timing Layer

Inner R: 1148 mm, Depth: 40 mm, L:  $\pm 2.6$  m along z,  $|\eta| < 1.45$ , 38 m<sup>2</sup>:  $\sim 332$ k channels

ToA for  $> 0.7$  GeV MIPs with  $\sim 30 - 60$  ps precision  
Thin, large area detector covering central region  
Needs to survive  $\sim 2 \times 10^{14}$  n<sub>eq</sub>/cm<sup>2</sup> irradiation dose

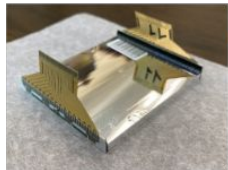
$\sim 10$ k BTL Modules, each w/ 16 scintillating **LYSO:Ce** bars and two 16-channel SiPM photodetector arrays  
Read out with custom **TOFHIR2 ASIC**  
Mounted on CO<sub>2</sub> cooled trays and installed on inner surface of BTL Tracker Support Tube



72 trays covering the surface  
○ total of 10 368 SMs  
○ total of 331 776 channels

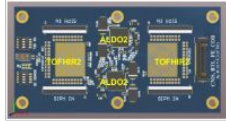


LYSO+SiPM  
Sensor Modules



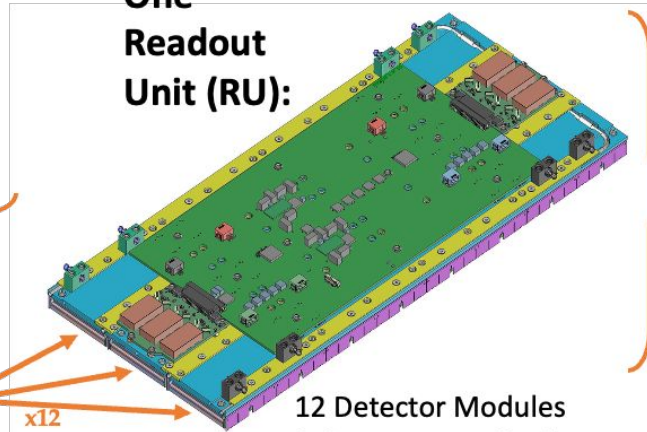
x2

FE Boards housing  
TOFHIR ASICs



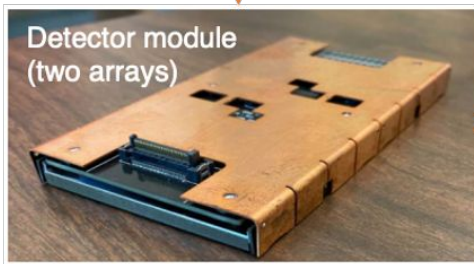
+

One  
Readout  
Unit (RU):



x6

12 Detector Modules  
1 Concentrator Card  
2 Power Converter Cards

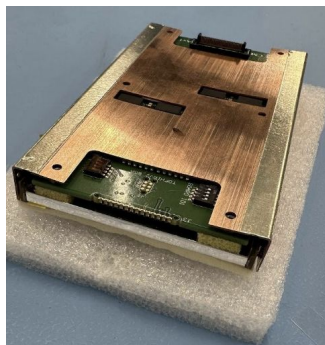


x12



# CMS Barrel Timing Layer

## Production Underway!



Module and Tray production underway at BTL Assembly Centers in **Caltech, U. Virginia, Milano-Bicocca, Peking U.**

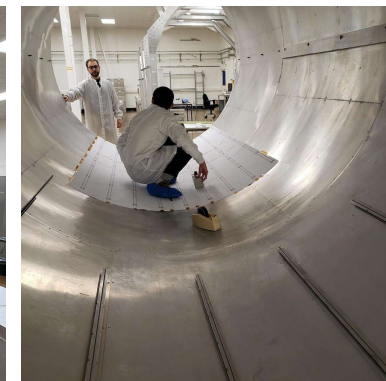
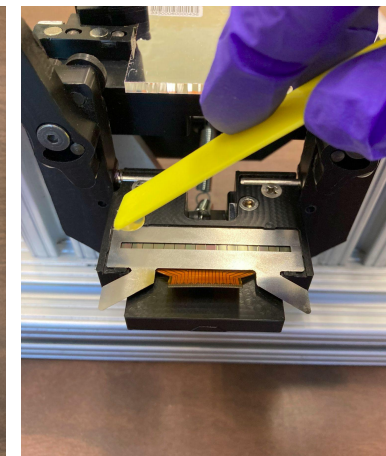
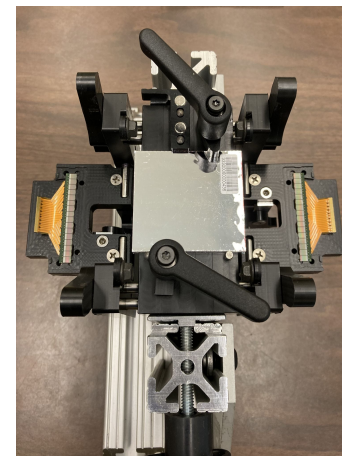
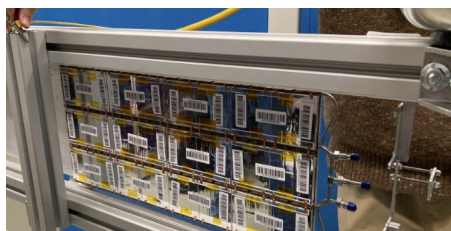
Production kicked off with first tray in March. Targeting 2 Trays / Month / Center assembled & shipped to CERN

100% of crystals and SiPMs qualified.  
80% sensor mod. + 50% of detector mod.  
10% of trays assembled and tested.

Tray production completion - February 2026

Tray integration in **BTL Tracker Integration Facility at CERN**, with installation in **BTL Tracker Support Tube**, second half of 2025

Installation in CMS in early 2029

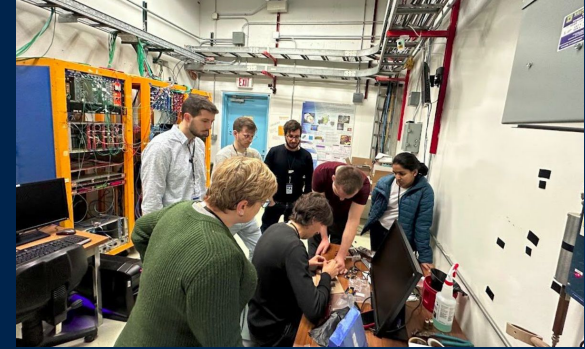


[...More details on QA/QC from FAST2025](#)



# CMS Barrel Timing Layer

Production Underway!

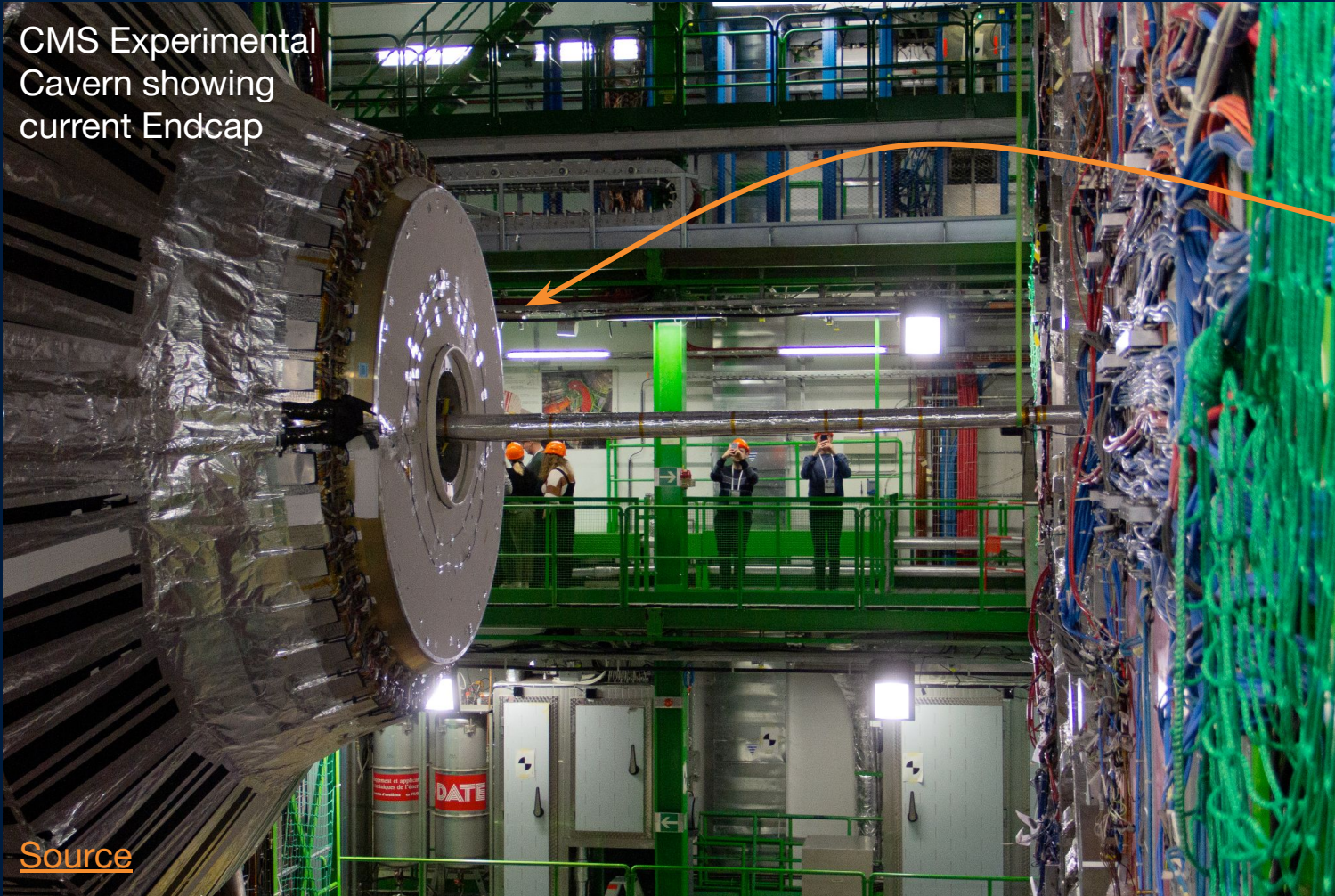




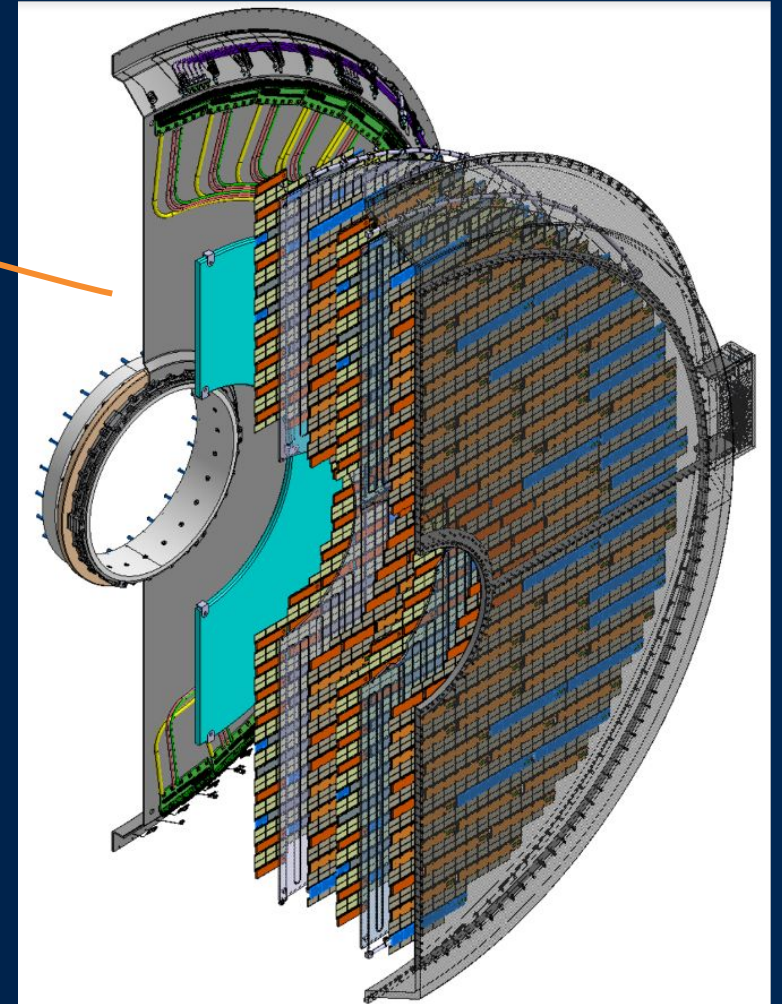
# CMS Endcap Timing Layer

$315 < R < 1200$  mm,  $z = \pm 3.0$  m,  $1.6 < |\eta| < 3.0$ , 1.3mm pixels, 14 m<sup>2</sup>: 8.5M channels

CMS Experimental Cavern showing current Endcap



[Source](#)

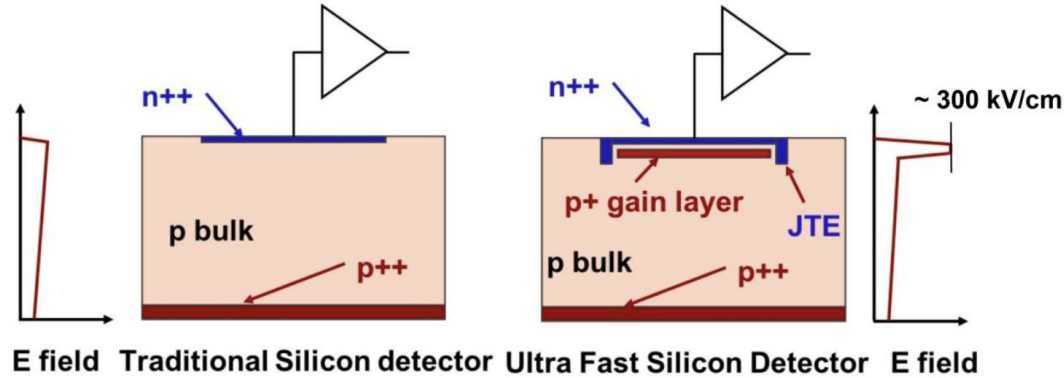




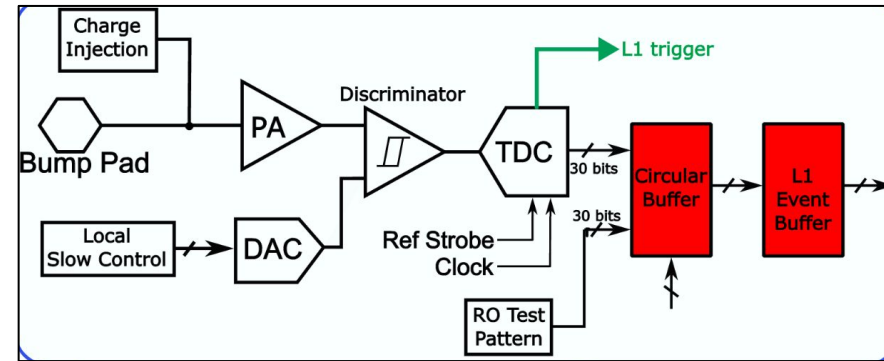
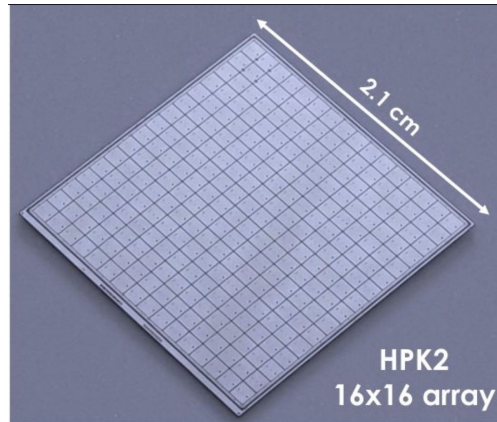
# CMS Endcap Timing Layer

## Fundamentals of the detector

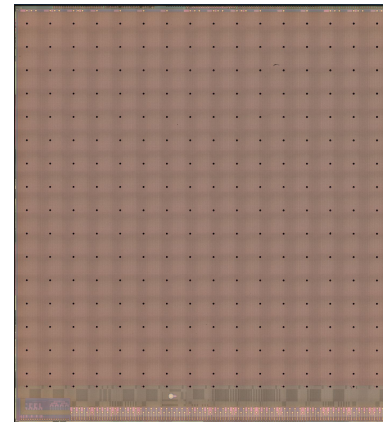
N Cartiglia et al



- Low Gain Avalanche Detector (LGAD)
- n on p sensor with p-type mult. layer
  - Low gain ( $G \sim 10$ ): improve signal slope
  - [Developed](#) at CNM Barcelona
  - [Proposed](#) for timing by UCSC/Torino
  - [~15 year development cycle](#) from idea to production in first-gen detectors



- Custom ASIC design in 65nm CMOS for the ETL LGAD readout (ETROC)
- Low noise, low power
  - Radiation hard to 100 MRad
- ~7 year development cycle so far from the start of the ETROC project

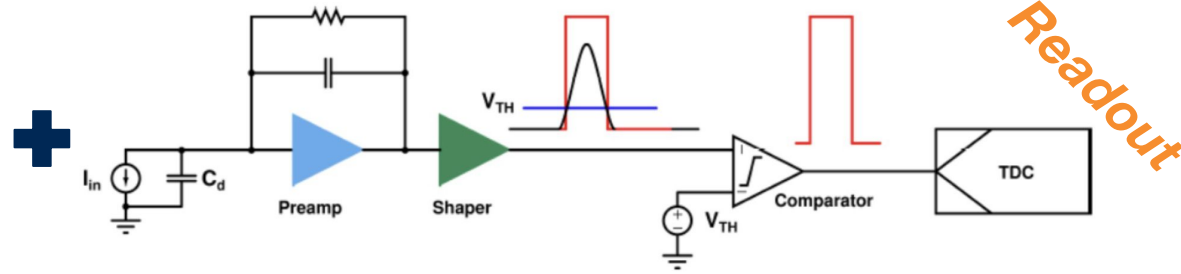
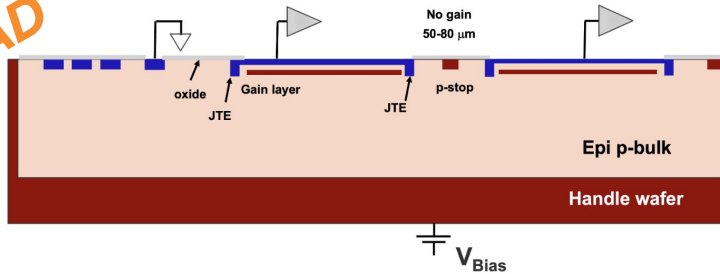




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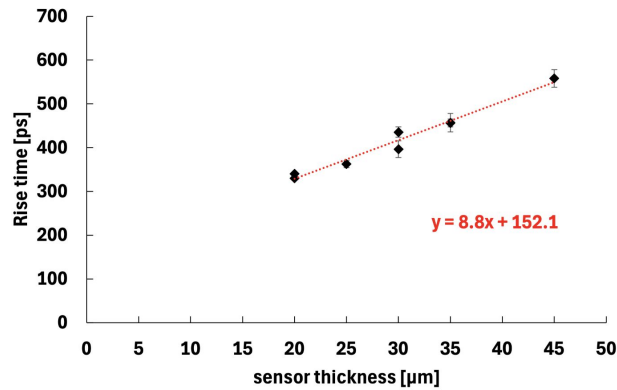
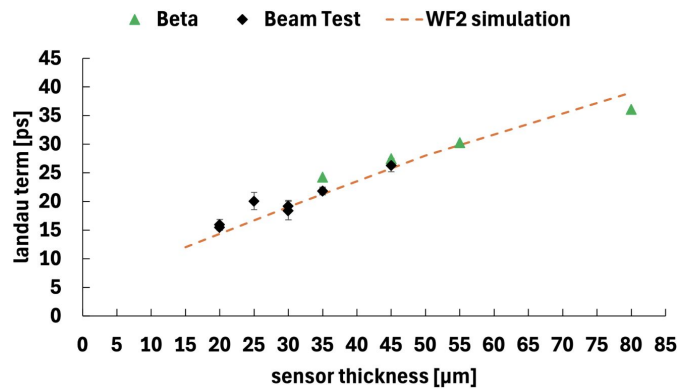
## Hybrid Pixel Model - Basics of Time Resolution

LGAD

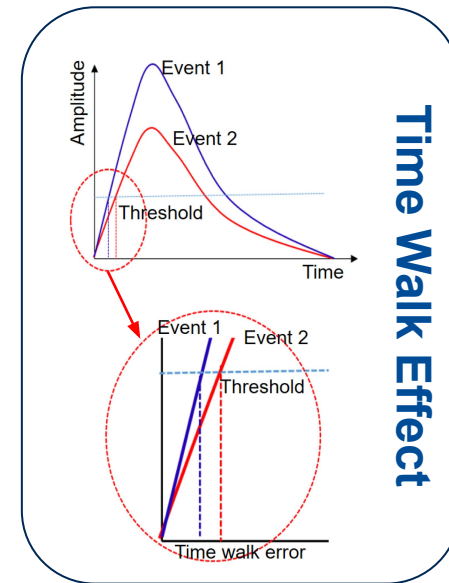


$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{timewalk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

V Sola at FAST2025



$$\frac{t_{rise}}{S/N}$$



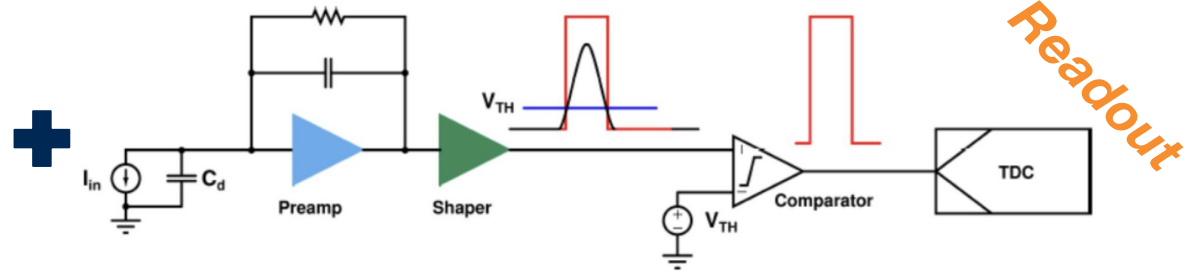
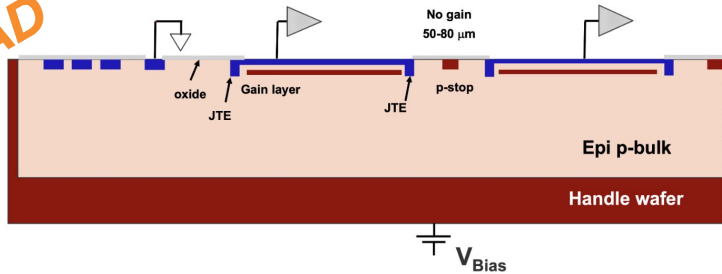
Time Walk Effect



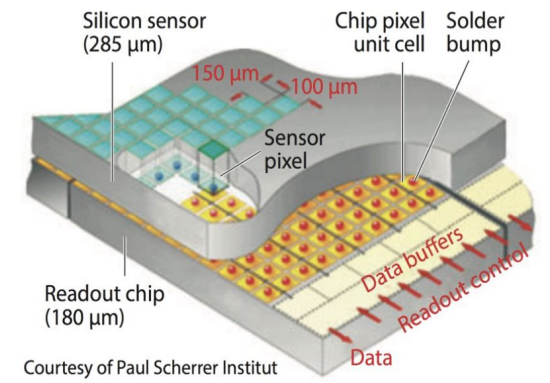
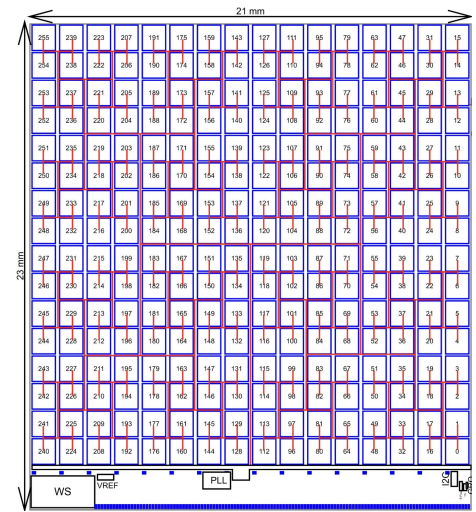
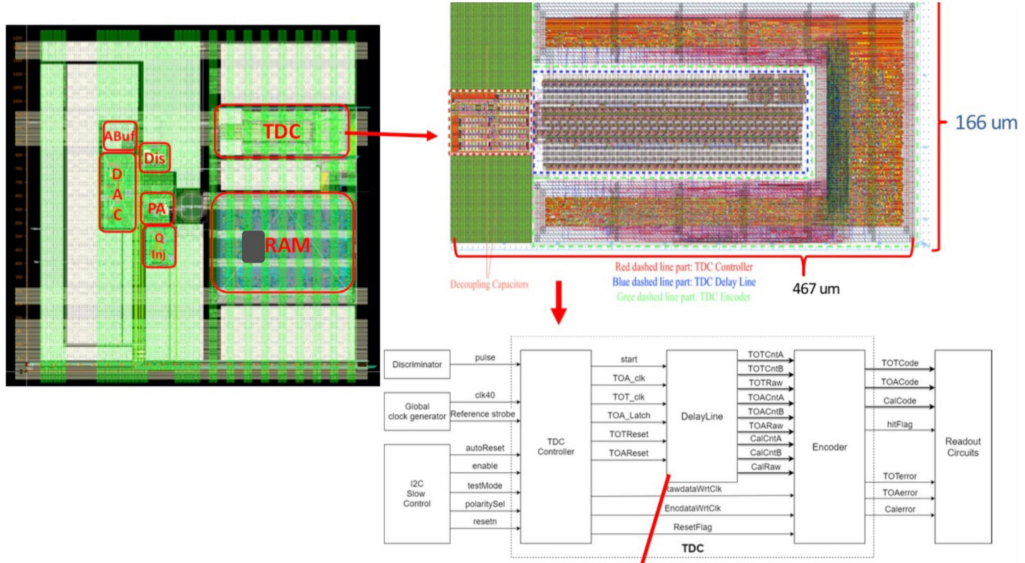
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## Hybrid Pixel Model - Basics of Time Resolution

LGAD



$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{timewalk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$



Courtesy of Paul Scherrer Institut

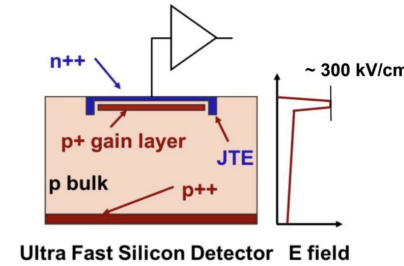


# CMS Endcap Timing Layer

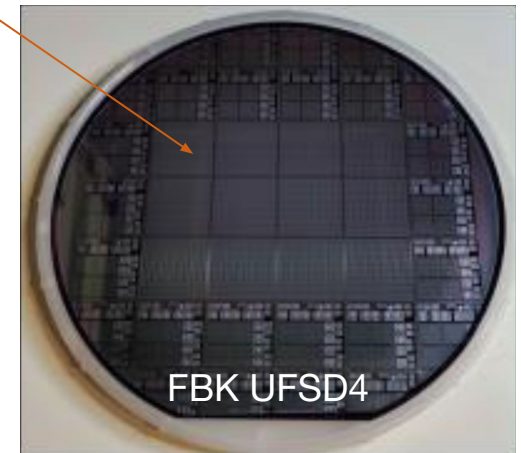
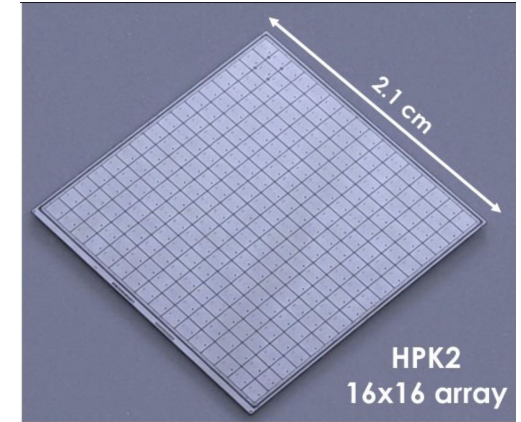
## Low Gain Avalanche Detectors

< 30-50 ps contribution from the sensor, limits active depth to 50um with a gain of 10-30 and pad size ~ mm<sup>2</sup> to minimize pad capacitance

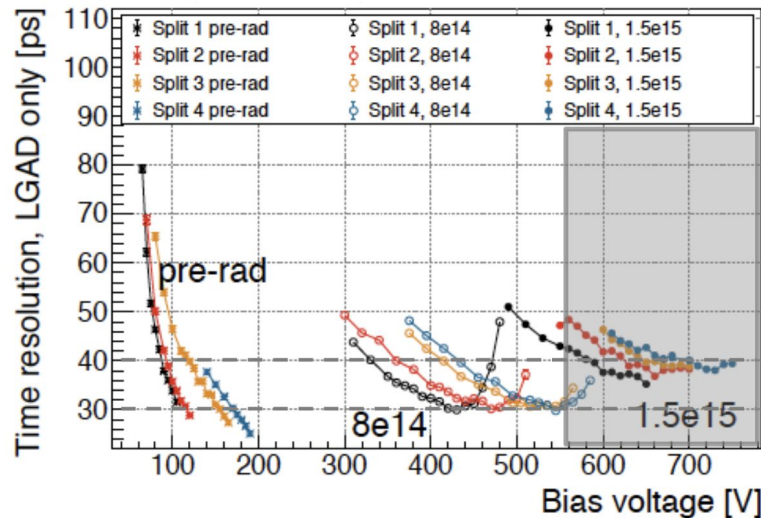
Need to withstand  $2 \times 10^{15} n_{eq}/cm^2$  in the innermost region over  $3 ab^{-1}$ , still deliver 8-10 fC for readout at the end of life



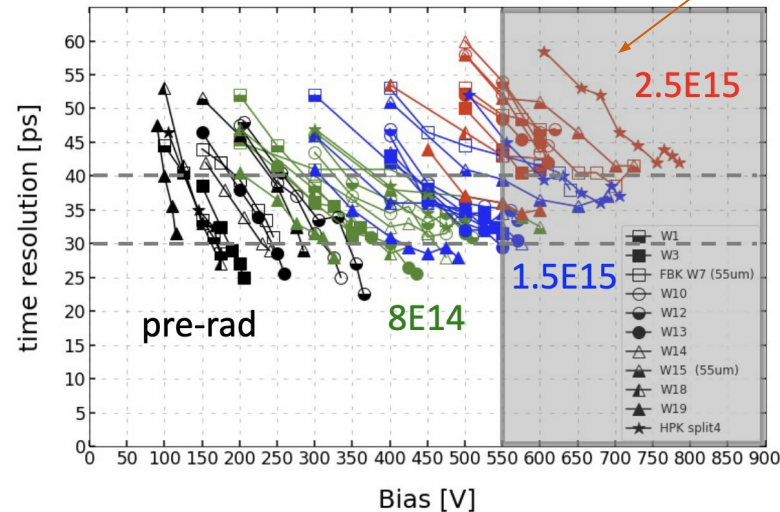
*Carbon Co-implants in Gain Volume*



HPK2 – Beta source



FBK UFSD3.2 – Beta source



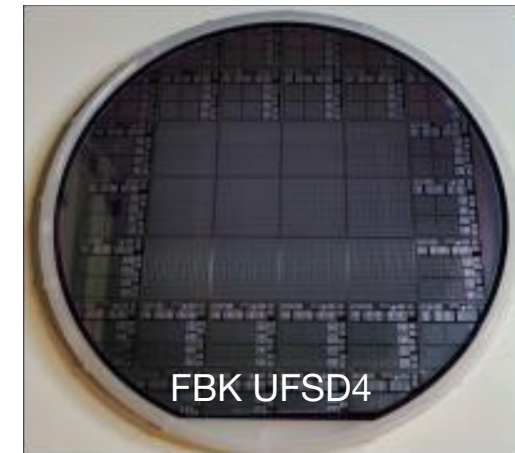
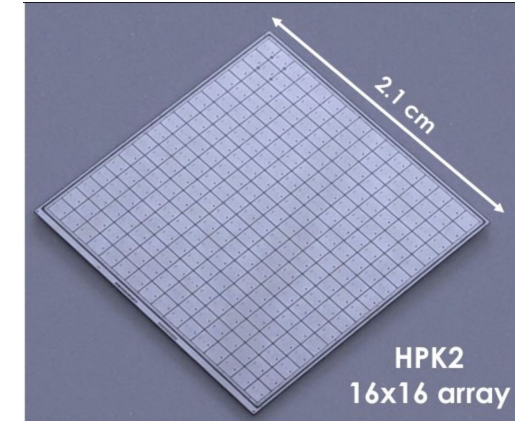
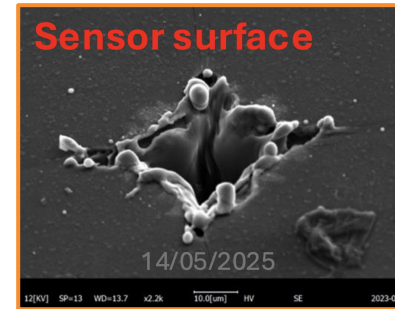


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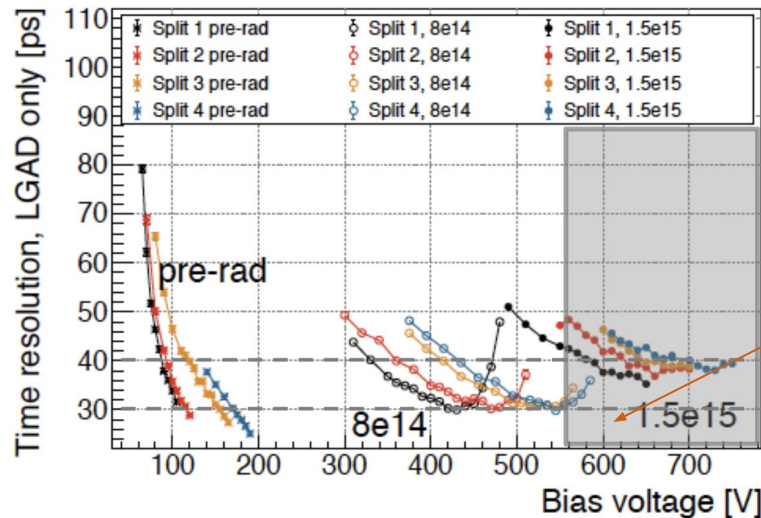
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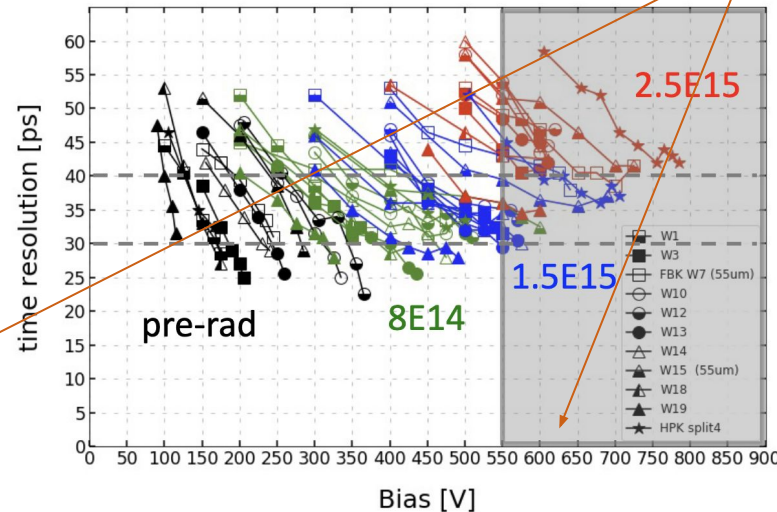
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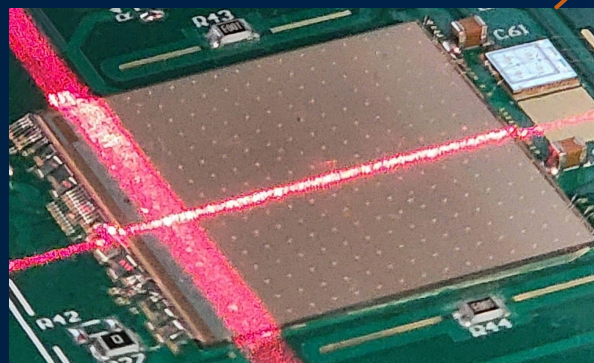
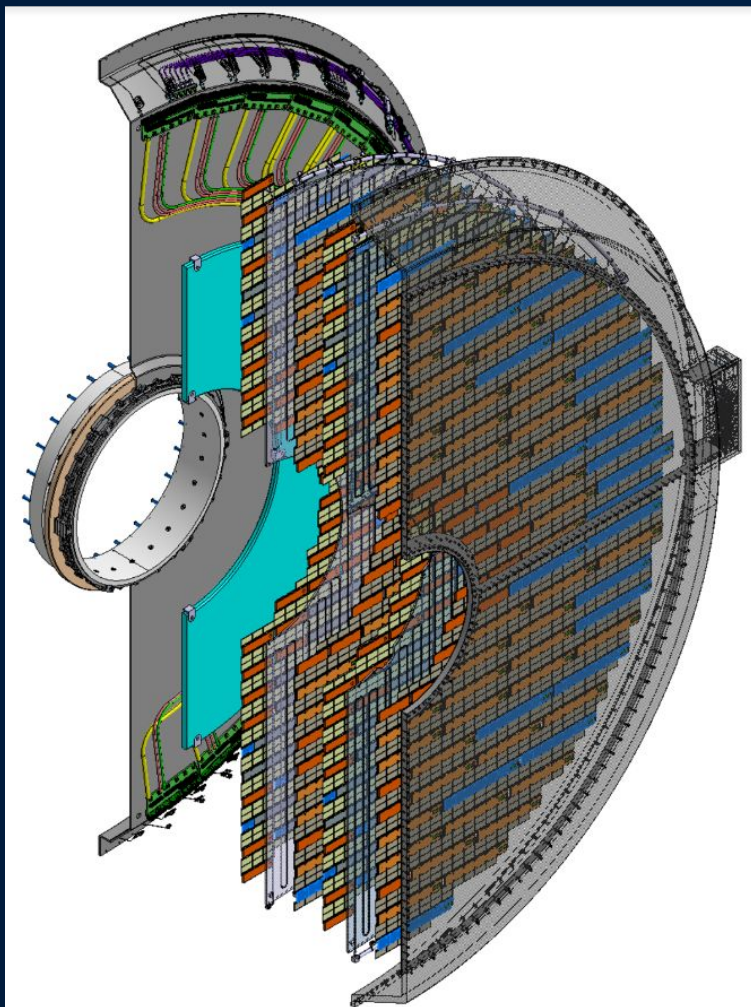




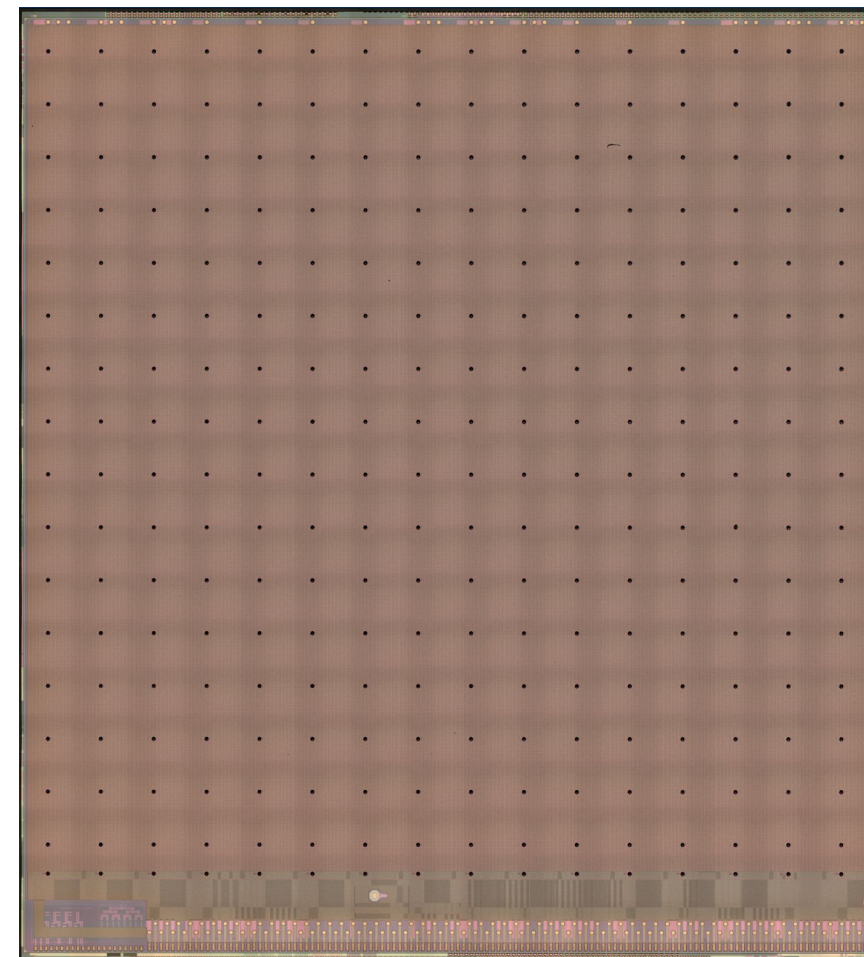
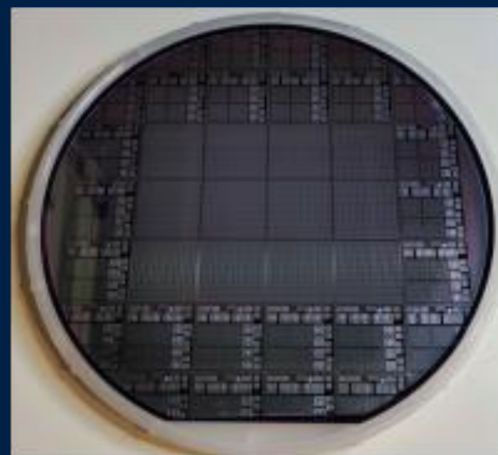
# CMS Endcap Timing Layer

~33k chips, 2.3 x 2.1 cm chips, 1.3 mm pixels, 16x16 px

ETL Read Out Chip (ETROC)



+





# CMS Endcap Timing Layer

2 hits per track, 50 ps res. per hit, 35 ps res. per track

What are the main constraints on this design?

## 1. Low Noise

- This is crucial! 30 ps intrinsic (Landau) resolution from LGADs also limits ASIC contribution < 40 ps

## 2. Low Power

- Thou shall not fry your detector! Cooling capacity limits power consumption to < 1W per chip, 4 mW per pixel, 240 mW/cm<sup>2</sup>

## 3. Radiation Hardness

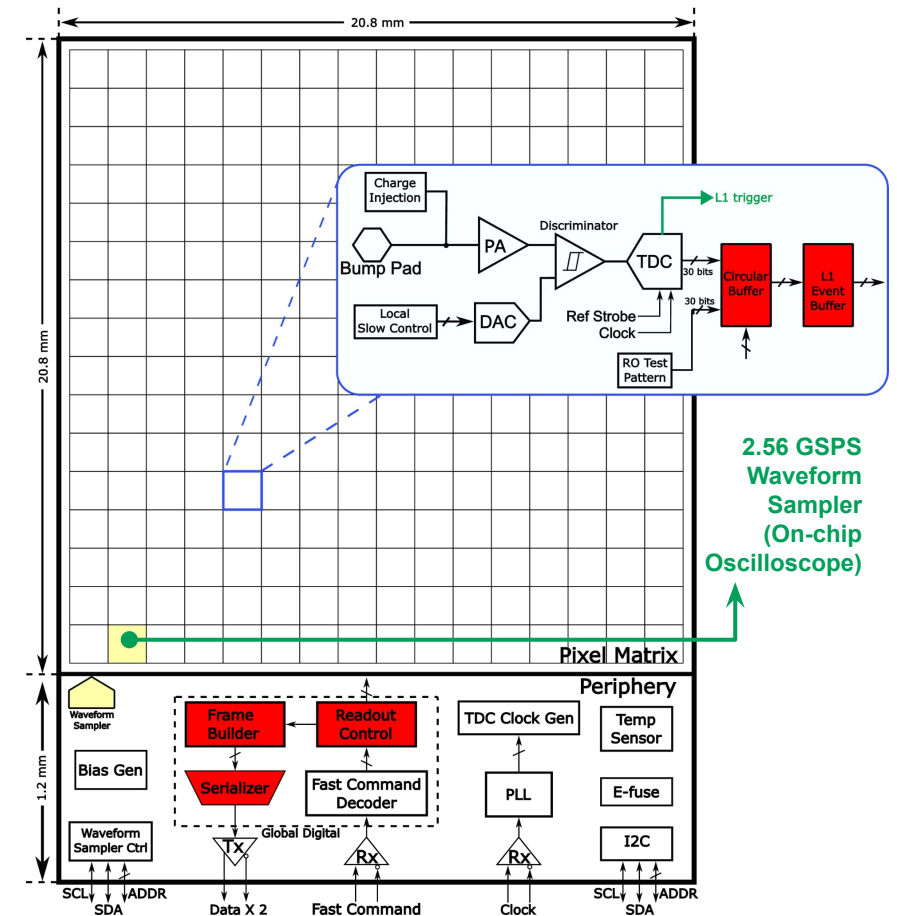
- Must withstand 100 MRad over the 3 ab<sup>-1</sup> of HL-LHC

## 4. Sensitive to small LGAD signals

- Around 10 fC per MIP towards end of lifetime of LGADs in ETL

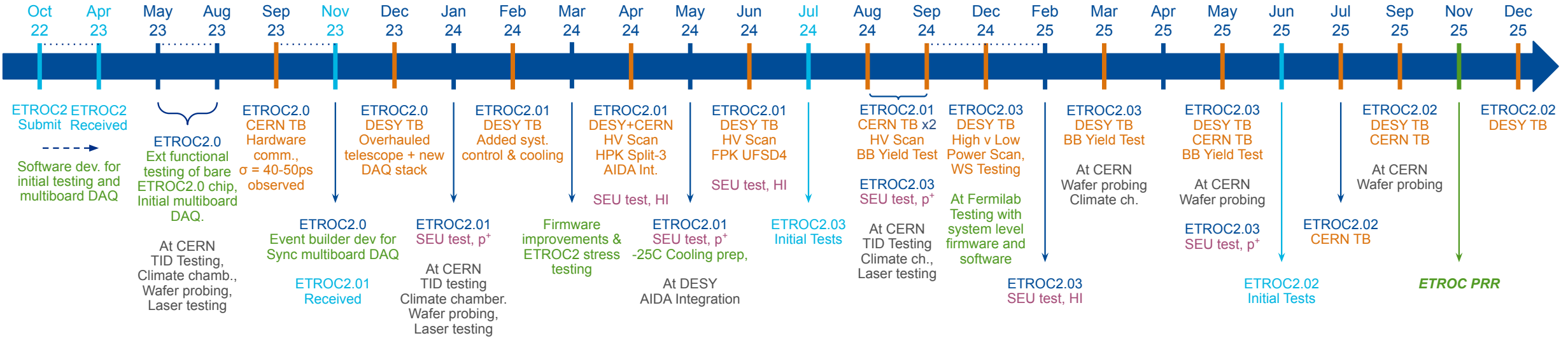
## 5. Synchronized precision timing over ~33k chips, ~8.5M channels...

## ETL Read Out Chip (ETROC)



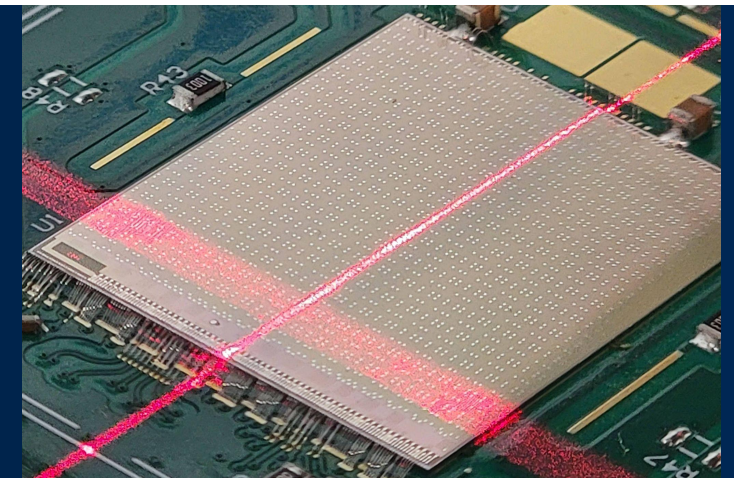
# CMS ETL - ETROC2 + LGAD Validation

## Extensive Characterization Campaign with the full sized ETROC2 chip



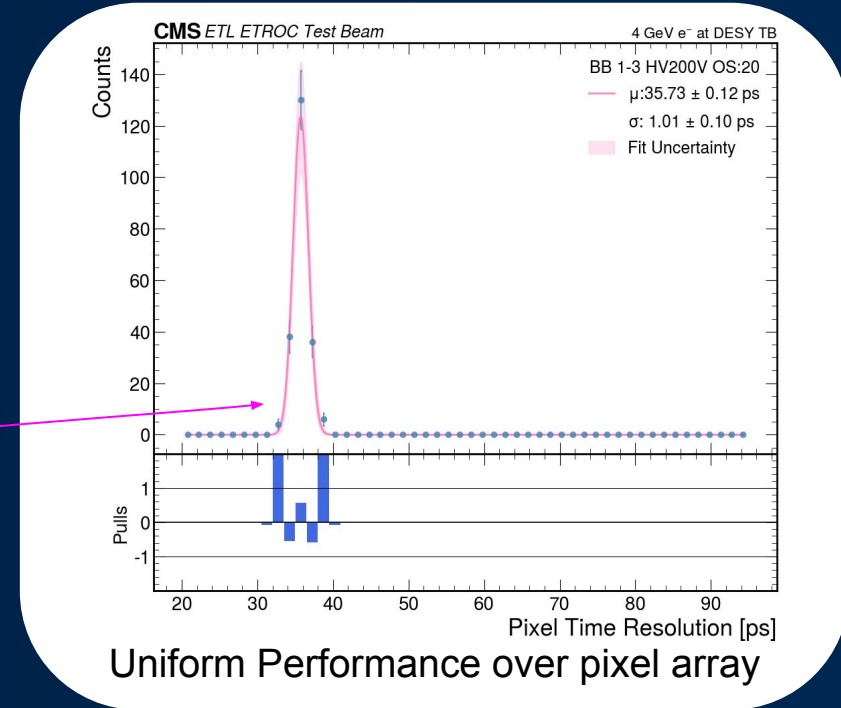
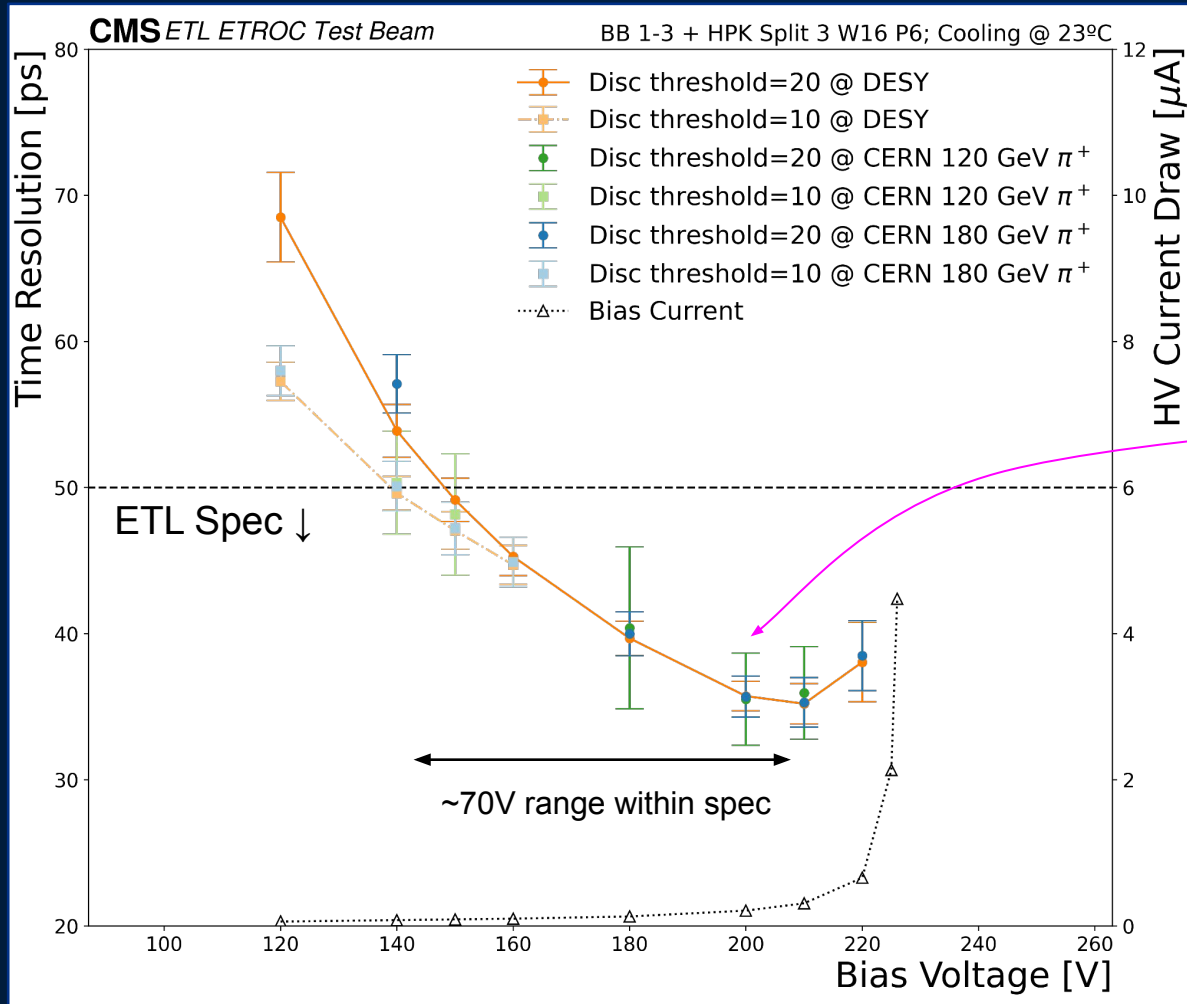
Aggressive heterogeneous campaign to validate the performance of the ETROC2 hybrids

Testing has enabled quick identification and fixes for ASIC and Sensor design for enhanced timing and robust operations





# CMS ETL - ETROC2 + LGAD Validation

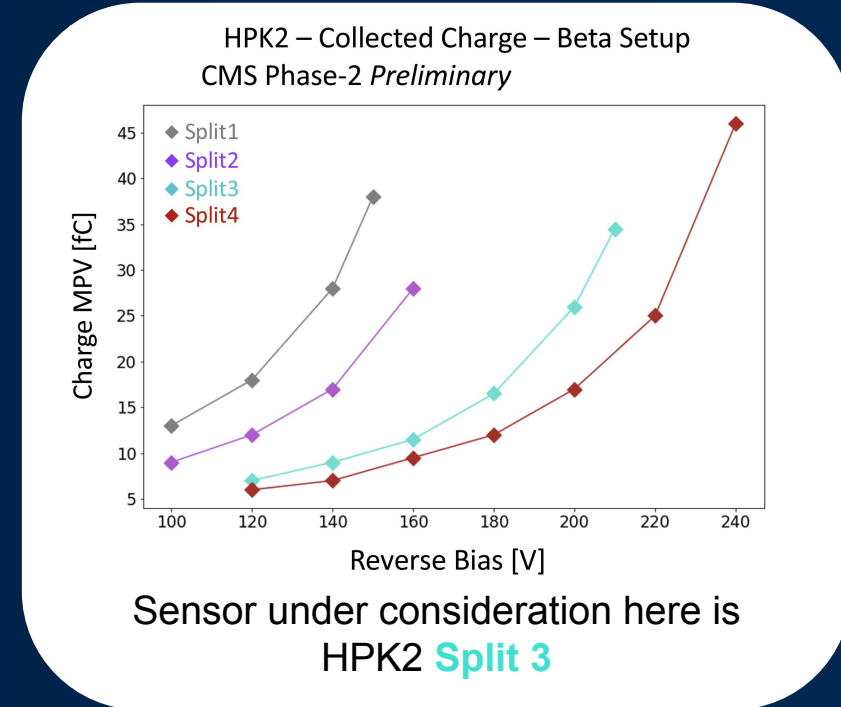
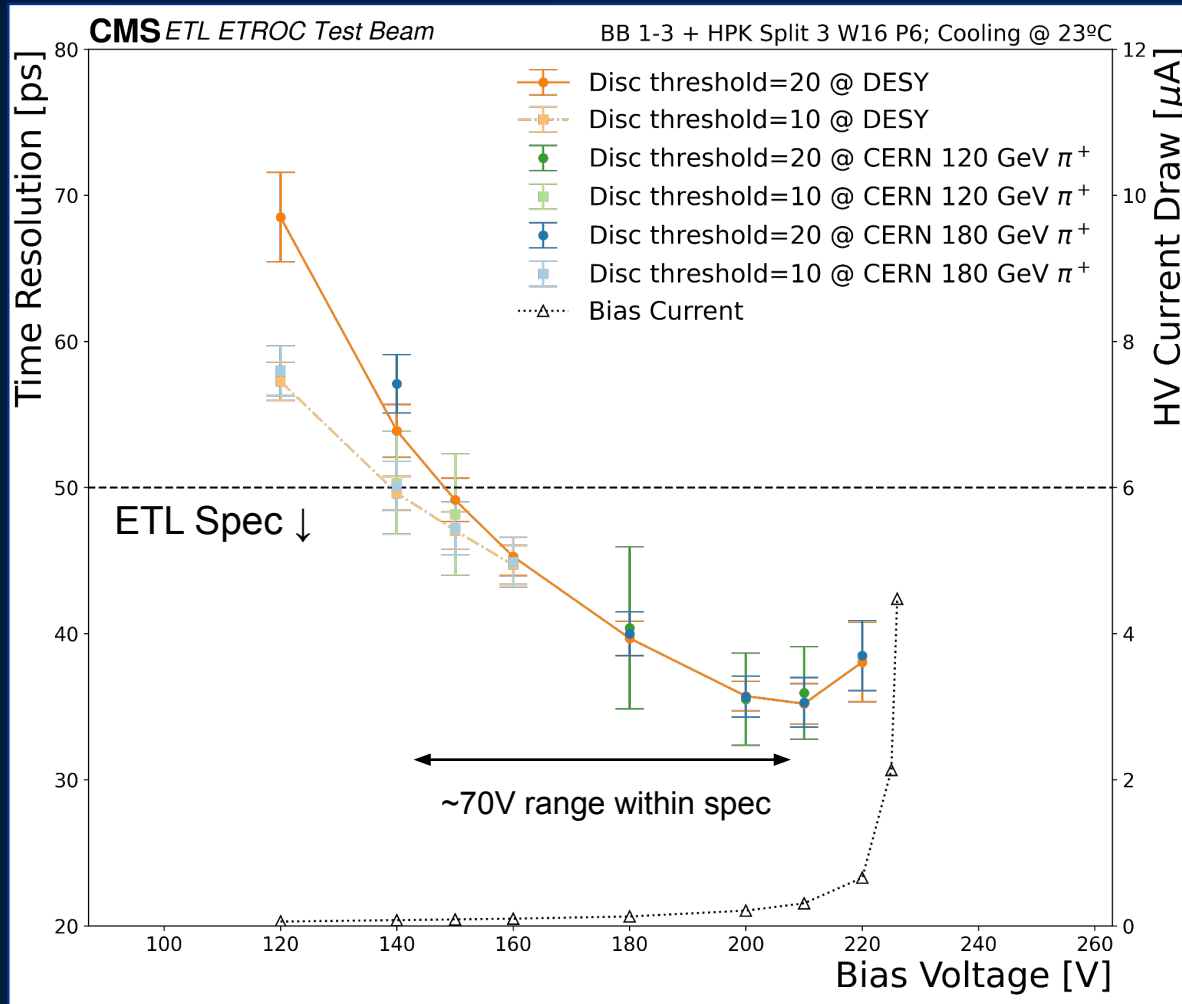


**Successfully reproduced ~35ps res.** with this board. Results from CERN 120-180 GeV  $\pi^+$  agree with those from DESY 4 GeV  $e^-$  beam

**Total typical chip power consumption is below 800 mW, well within the design constraints on the ETROC**



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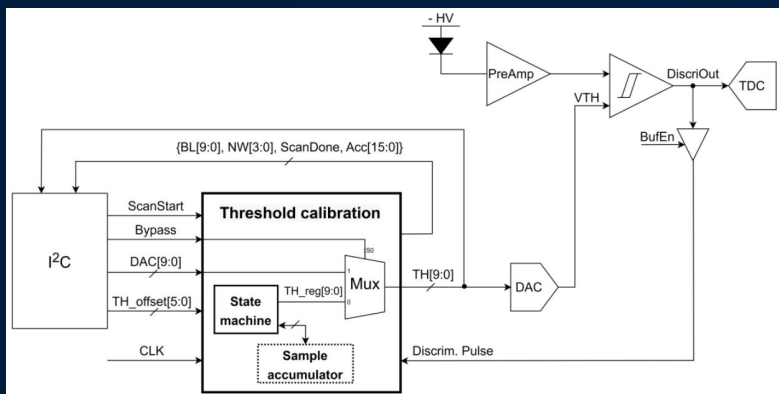
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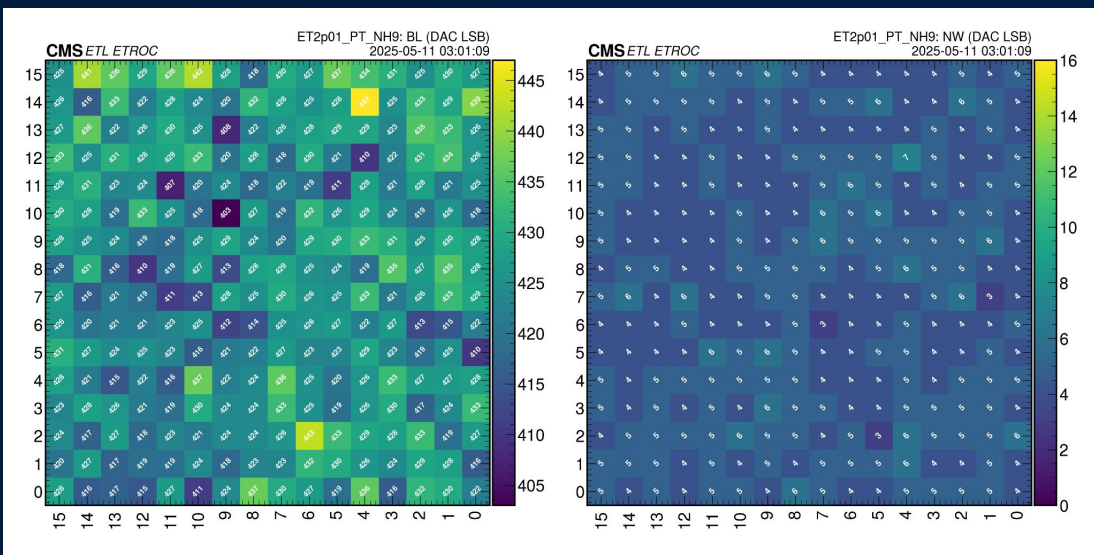
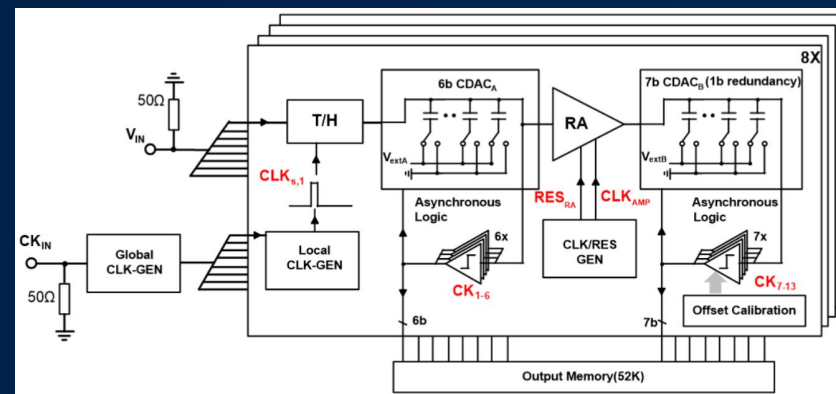
# ETROC - Beyond The Timing Precision

ASIC Design must incorporate features that make the detector operation feasible

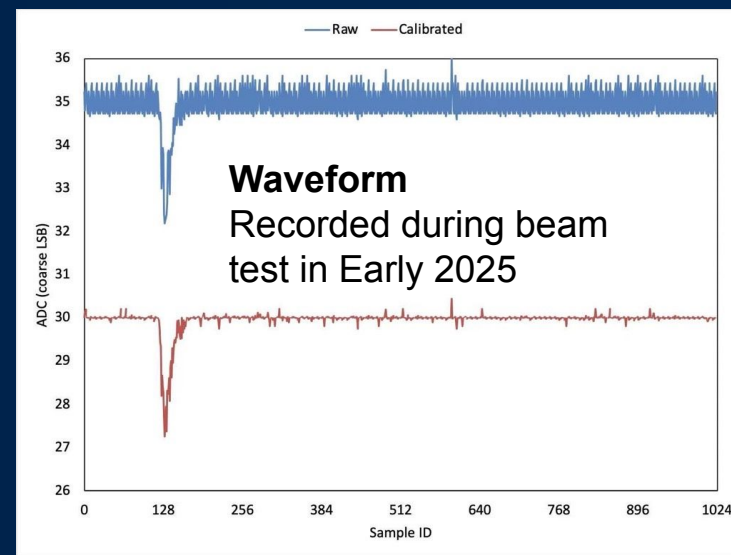
## Automatic Baseline Calibration



## 2.56GSps Waveform Sampler



Study LGAD signal shape evolution with TID, etc with 33k oscilloscopes across ETL!





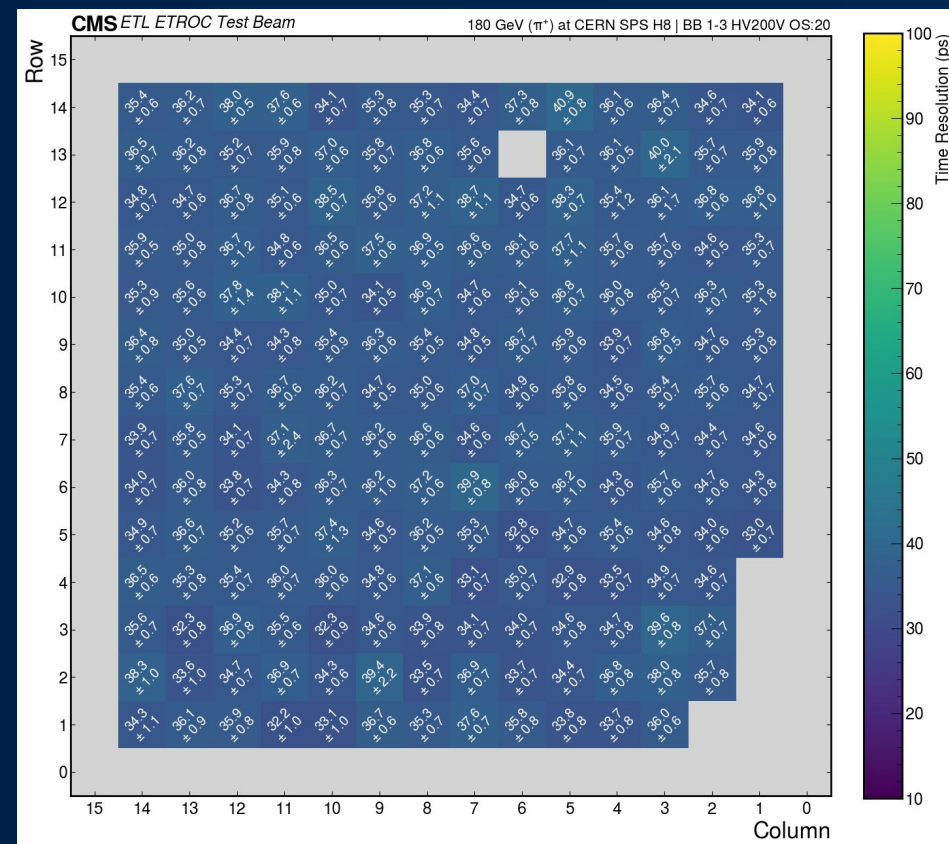
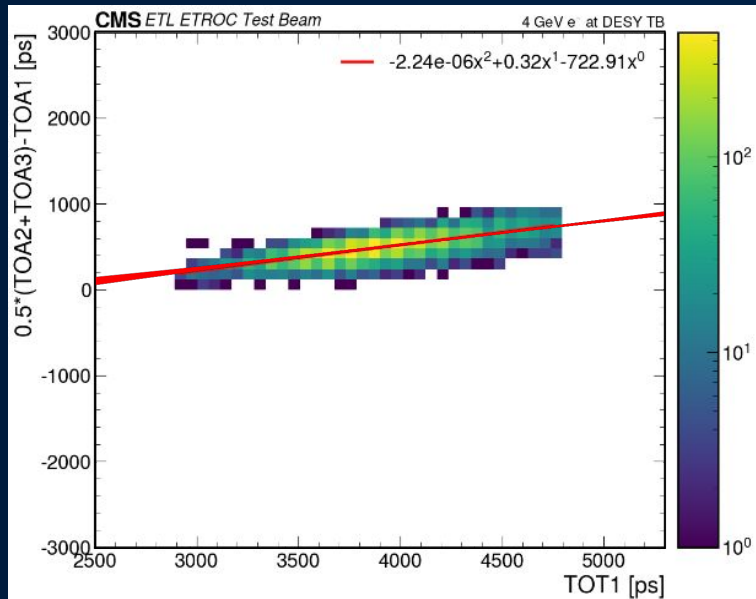
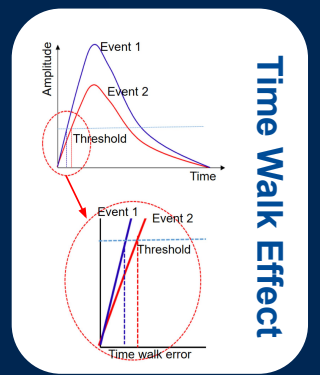
# ETROC - Beyond The Timing Precision

ASIC Design must incorporate features that make the detector operation feasible

## Pixel Array Uniformity

TDC Self-calibration with double strobe method helps eliminate PVT variations across the 16x16 array of pixels

This also means each of the 16x16 pixels is expected to perform identically once the self calibration is applied to each pixel





# CMS Endcap Timing Layer

## Module production rapidly converging

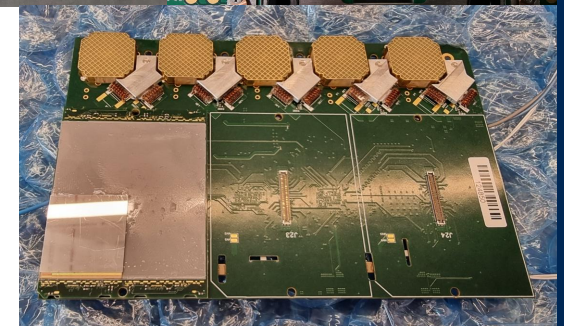
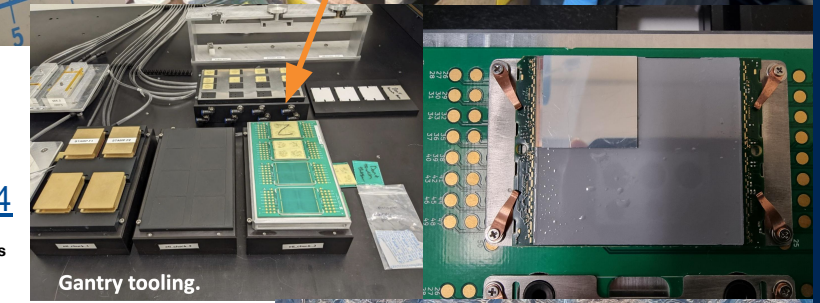
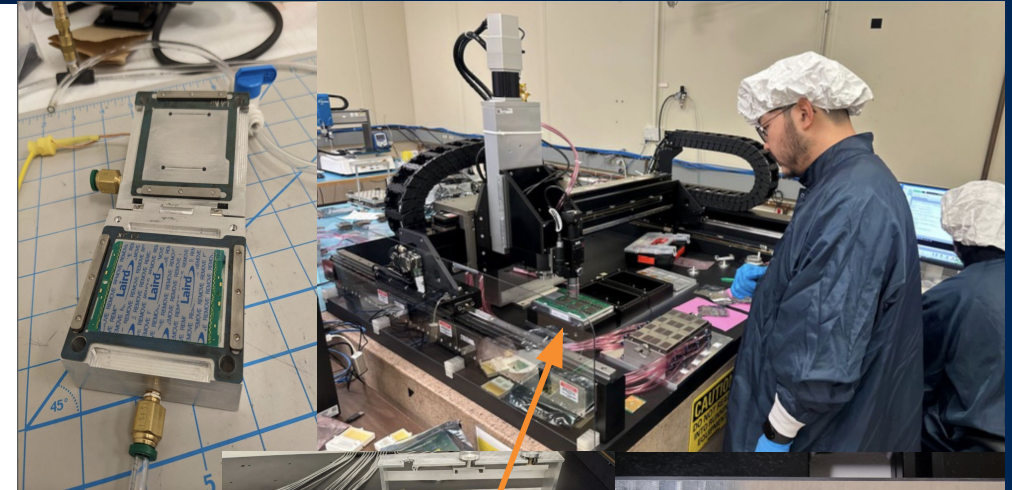
Each ETL module is a 2x2 array of hybrids (LGADs arrays + ETROC) along with a baseplate and PCB for interface with readout

4 ETL assembly sites will produce the 8000 modules required for ETL: **Fermilab, Boston University, INFN (Italy) and IFCA (Spain)**

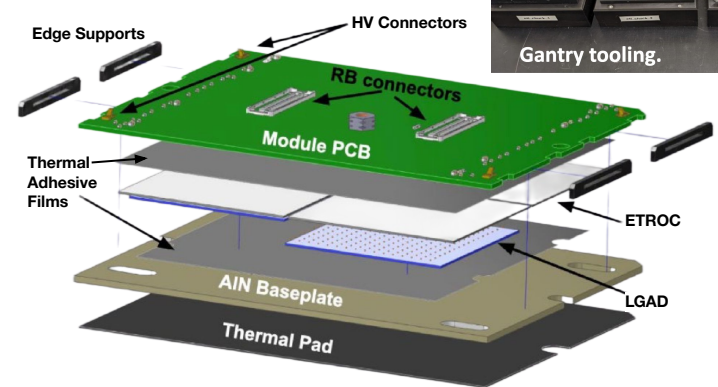
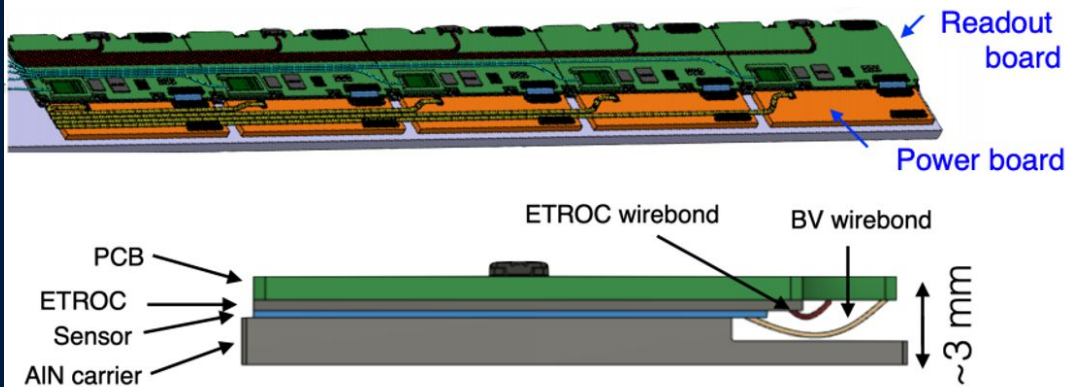
- Currently optimizing QA/QC procedures

Demonstrated production at scale (50 modules/week) to understand personnel requirements and identify remaining issues with the assembly procedure.

- Track time of each step as well as QA/QC data such as alignment and number of re-bonds.



[...More details on Sensor QA/QC from TREDI2024](#)



# CMS Endcap Timing Layer





# CMS Minimum Ionizing Particle Timing Detector

First generation timing detector being deployed at the HL-LHC

- CMS MTD is among the very first generation timing detectors being introduced for the HL-LHC era
  - Successful production, assembly, and operations for the CMS MTD and ATLAS HGTD are crucial pathfinding exercises for future 4D trackers
  - Improved PU rejection, and new capabilities for LLP / displaced searches and ToF PID
- The CMS MTD will provide near hermetic precision timing ( $|\eta| < 3.0$ ) for tracks using the BTL and ETL
  - Different constraints from radiation hardness, access requirements, instrumented area, etc allow the use of different technologies in each
    - BTL: LYSO:Ce + SiPM
    - ETL: LGADs
- BTL team concluded a successful, multi-faceted campaign of prototyping, optimization, and validation
- BTL production phase has begun in full force, with SM, DM, RU, and tray production and assembly underway
  - Tray assembly on track for early 2026 completion
- ETL team is also nearing the end of a successful characterization campaign
- Sensor procurement tenders are out and ASIC engineering run have commenced
- BTL and ETL on track for timely installation in CMS for Phase-2 upgrade!



# CMS ETROC Acknowledgments

- *This work was produced by Fermi Forward Discovery Group, LLC under Contract No. 89243024CSC000002 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics. Publisher acknowledges the U.S. Government license to provide public access under the DOE Public Access Plan DOE Public Access Plan*
- *The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).*
- *The research leading to these results has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement no. 101057511.*



# Fermilab

Fermi *FORWARD*



U.S. DEPARTMENT  
*of* ENERGY



# CMS Barrel Timing Layer

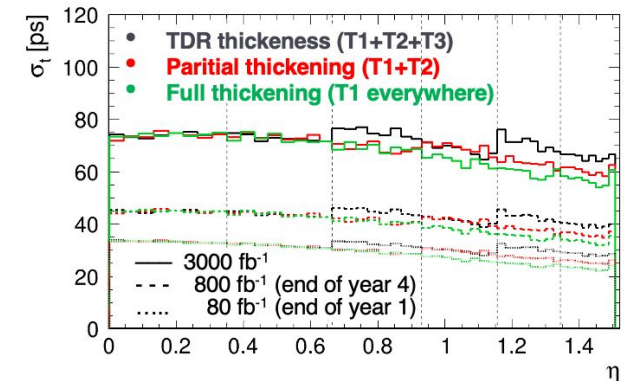
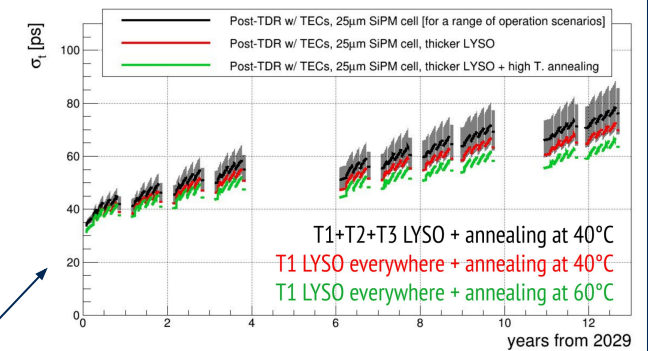
Optimize signal amplitude, rise time, dark count rate for timing performance

$$\sigma_t = \sigma_t^{ele} \oplus \sigma_t^{phot} \oplus \sigma_t^{DCR} \oplus \sigma_t^{clock}$$

Electronic Noise term goes as rise-time/SNR  
Photostatistics term goes as 1/root(amplitude)  
Dark Count Rate term goes as root(DCR)/amplitude

**LYSO:Ce** bar geometry minimizes SiPM area wrt crystal volume:  $3.12 \times 3.75 \times 54.7 \text{ mm}^3$

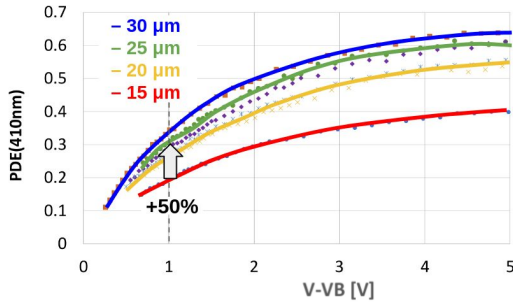
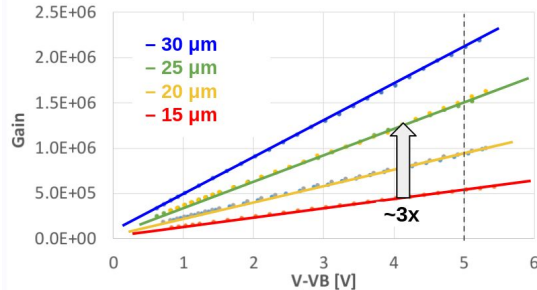
- **Thick** crystals used across the full BTL detector
- Optimized wrapping for improved light collection





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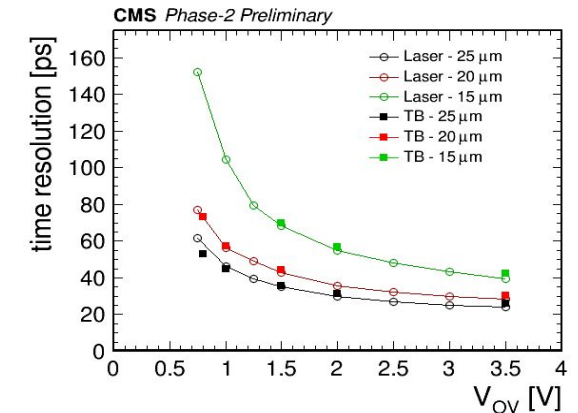
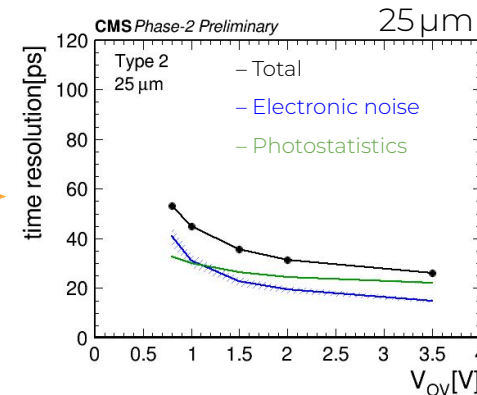
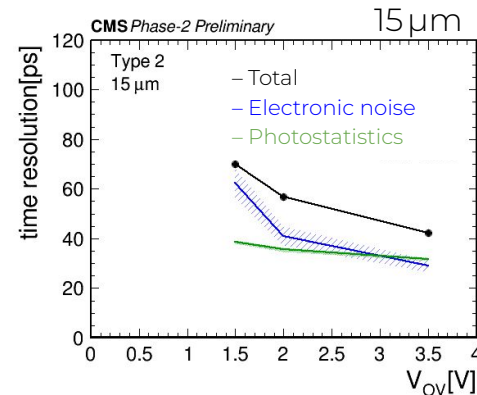
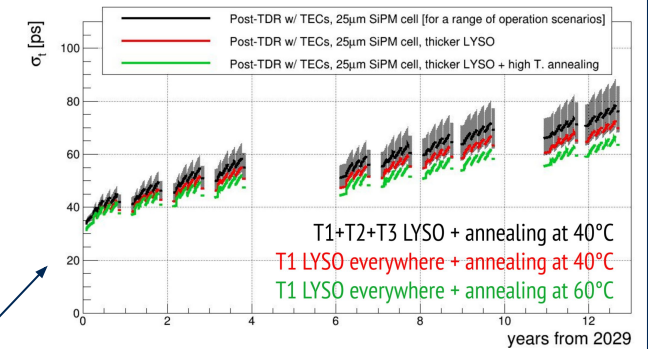
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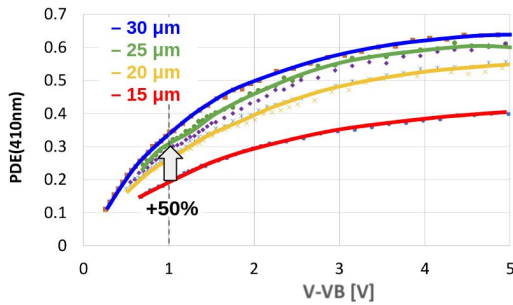
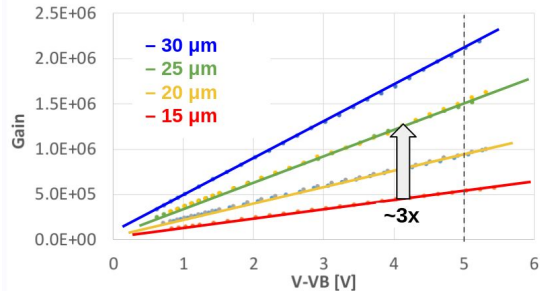
**SiPM** gain, photodetection efficiency, and speed increased by using **25μm cell size**





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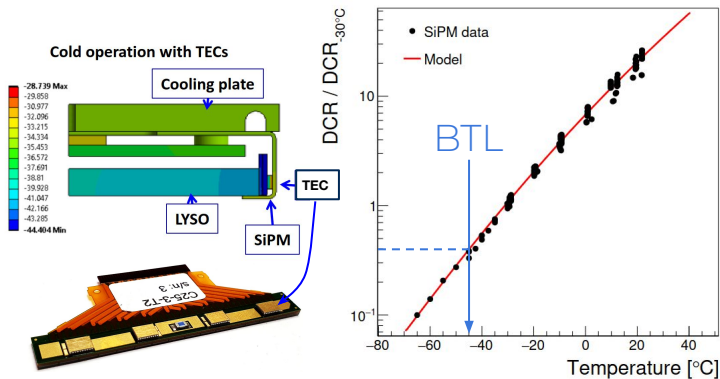
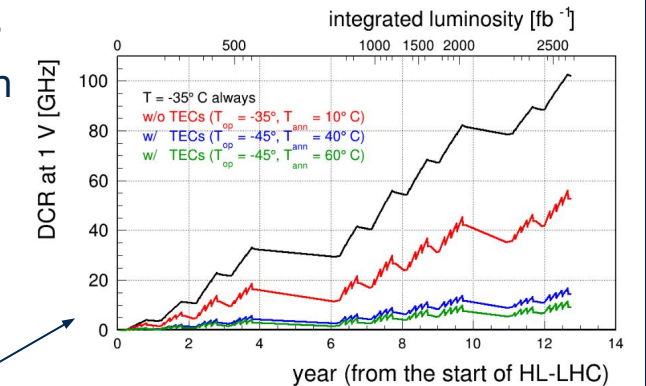
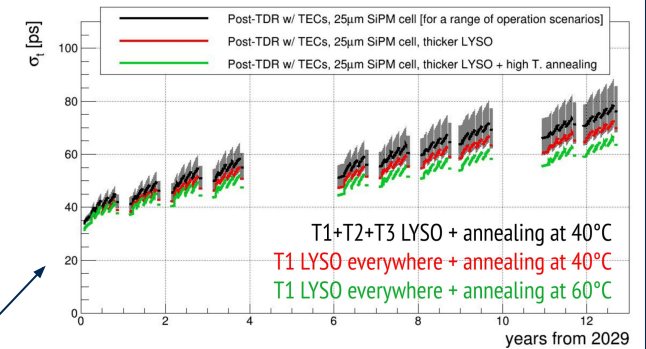
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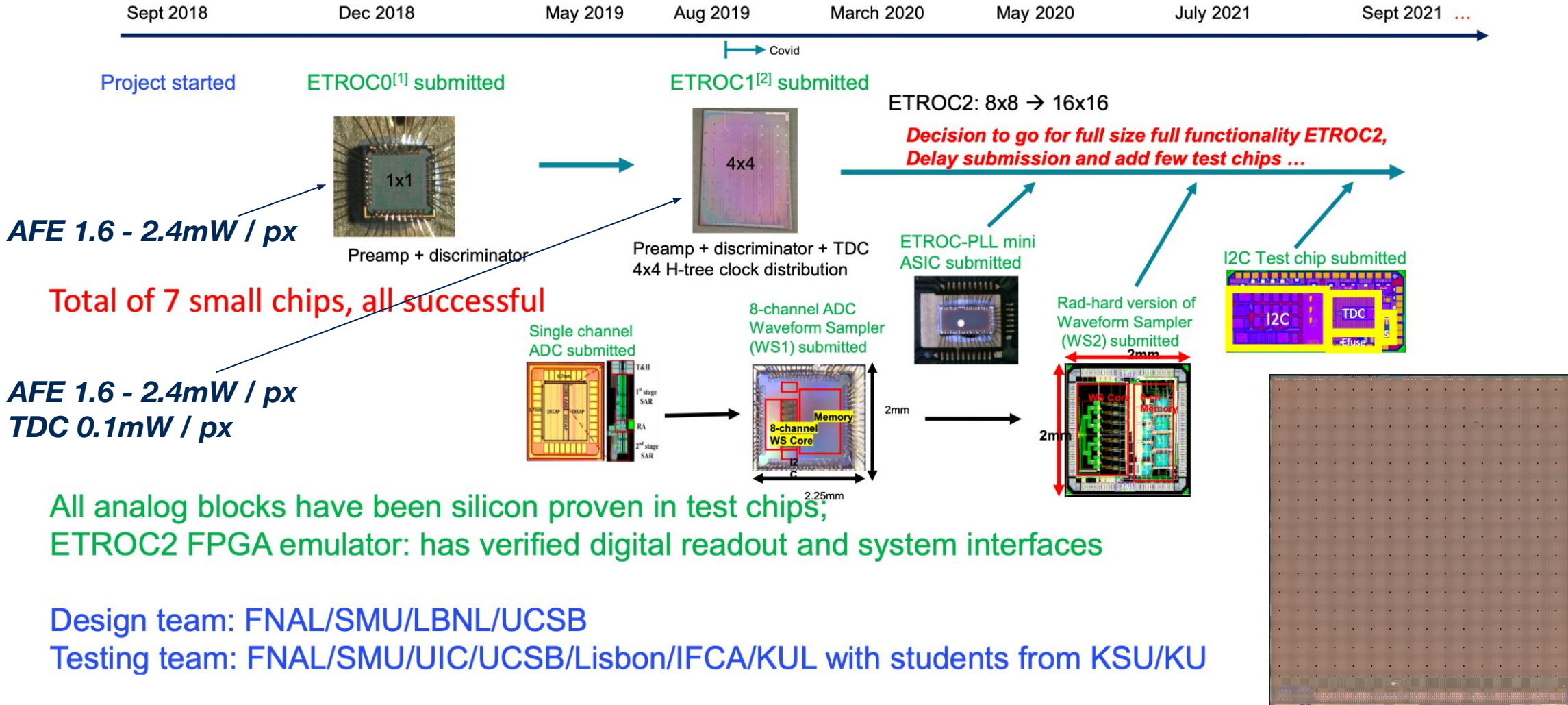
**SiPM** gain, photodetection efficiency, and speed increased by using **25 μm cell size**

- **Operate at -45 C** (dual-phase CO<sub>2</sub> + Thermoelectric Cooling) to minimize DCR
- High temp **annealing at 60 C** to heal radiation damage over 3 ab<sup>-1</sup>



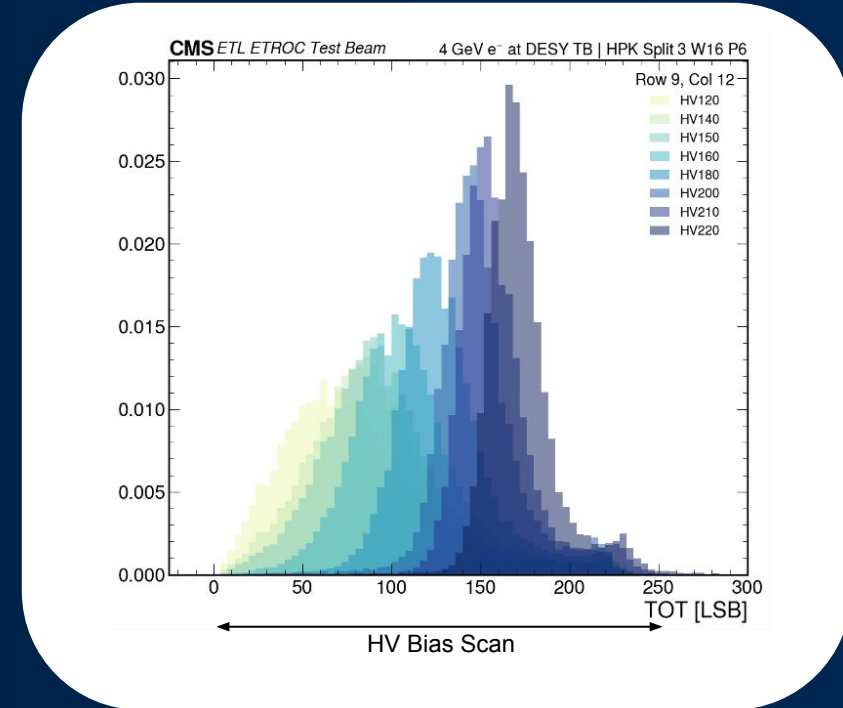
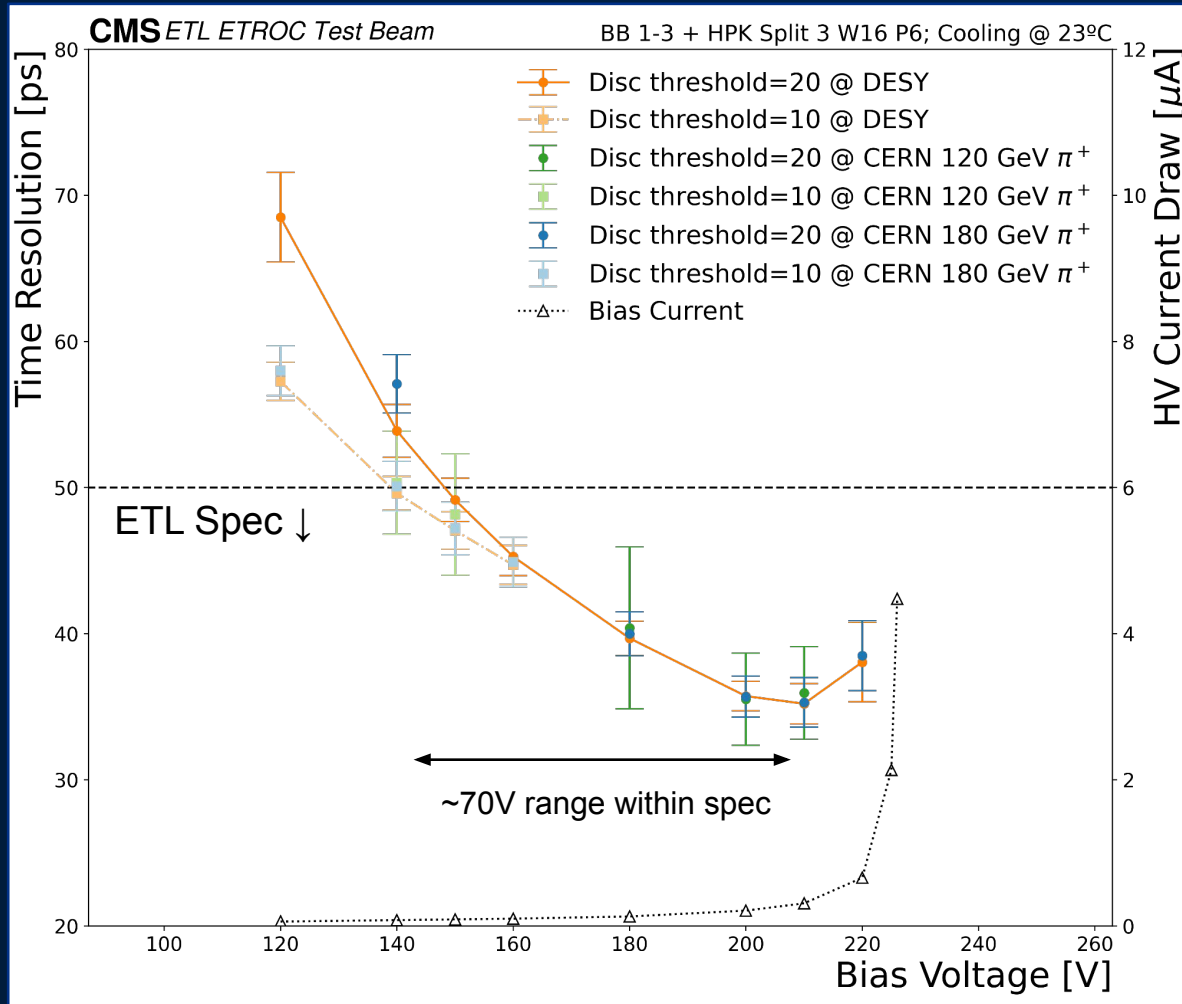


## Long Journey to the full sized chip...





# CMS ETL - ETROC2 + LGAD Validation



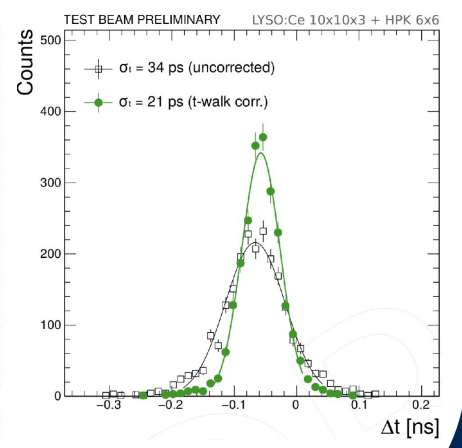
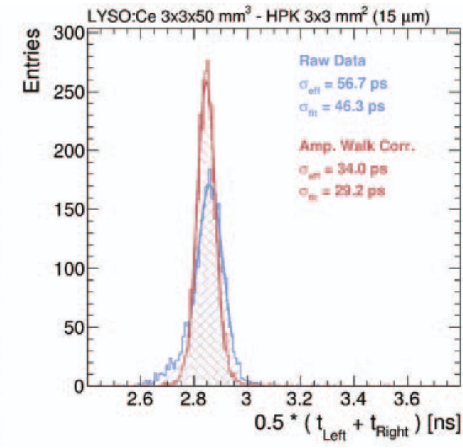
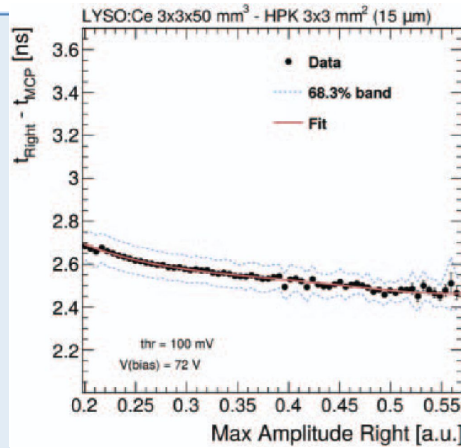
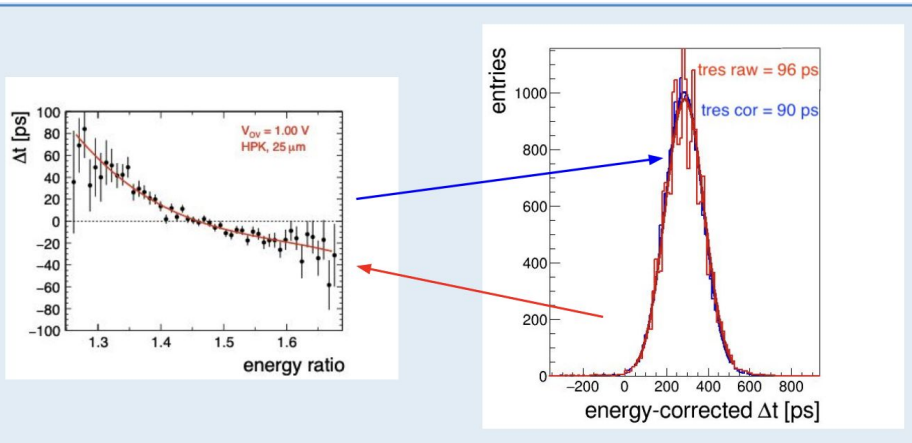
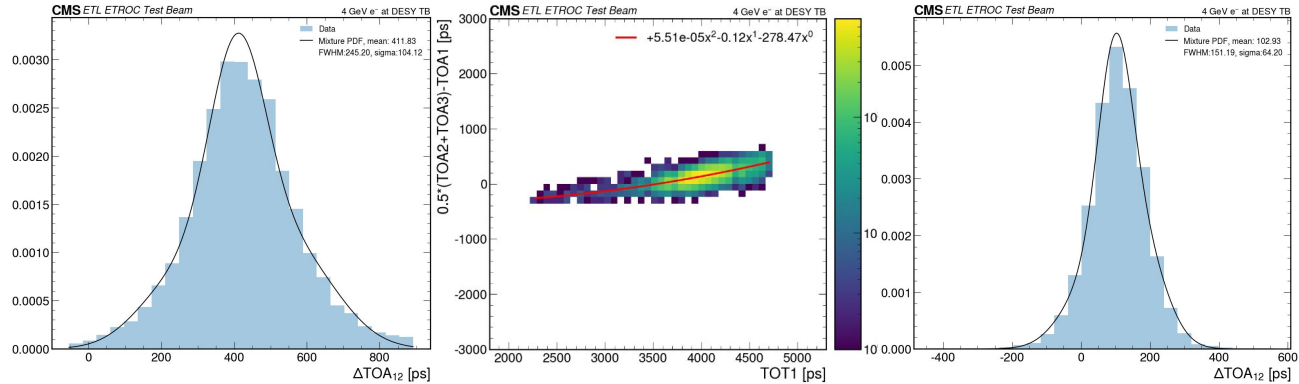
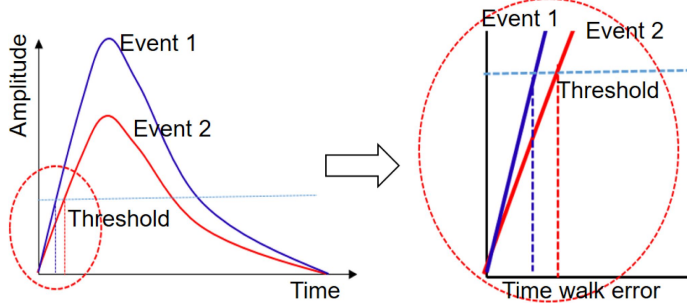
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**Total typical chip power consumption is below 800 mW, well within the design constraints on the ETROC**

# CMS MTD - Time Walk Correction

Examples from ETL and BTL

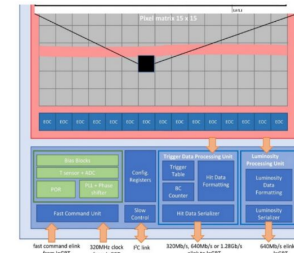
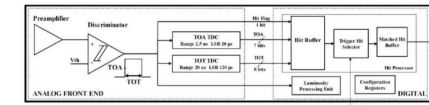
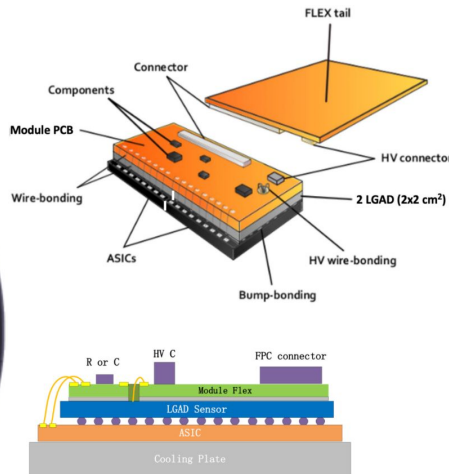
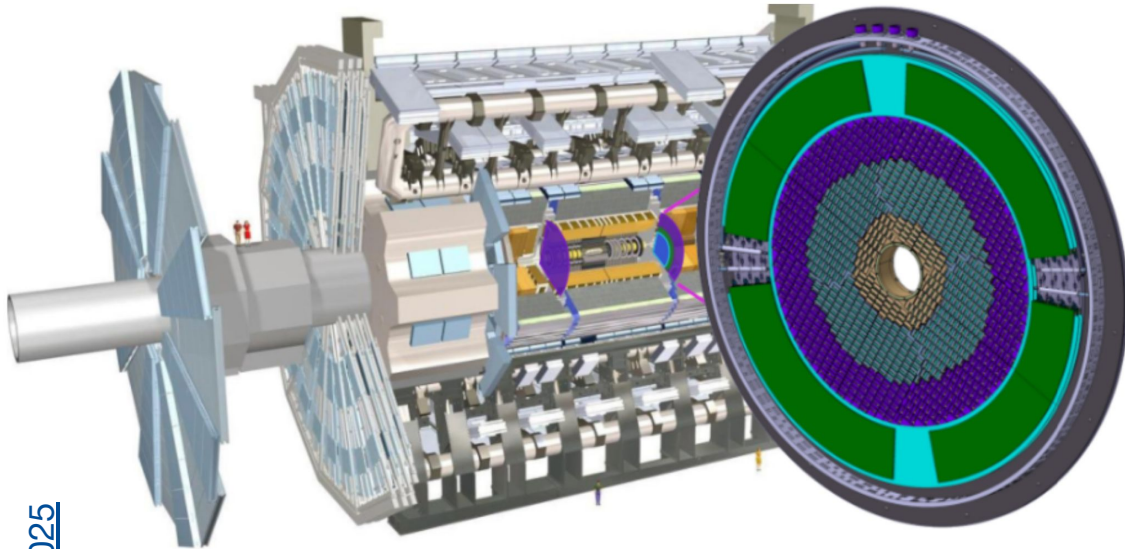
## Time Walk Effect



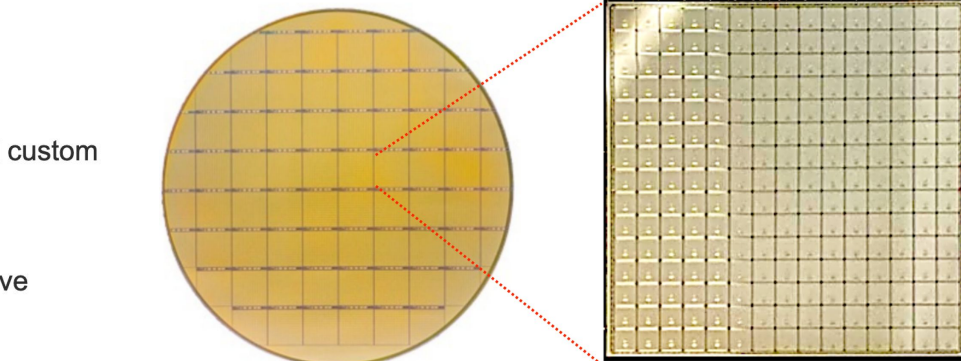


# HL-LHC: First generation timing detectors

## ATLAS High Granularity Timing Detector



Architecture of the ALTIROC ASIC readout 15x15 pads, 2x2 cm<sup>2</sup>, CMOS 130 nm, Jitter ~25 ps



8-inch LGAD wafer

Full size 15\*15 LGAD sensor

Xiao Yang at VCI2025

2x double-sided layers, based on **Low Gain Avalanche Detectors (LGADs)** and custom ASICs (ALTIROC)

- Target: **30-50 ps per track** (35 - 70 ps per hit),
- **6.4 m<sup>2</sup>** silicon detector, **3.6M** channels, **1.3 × 1.3 mm<sup>2</sup>** pixel size, **50 μm** active thickness.

Radiation hardness requirement:  
**2.0 MGy TID** and **2.5E15 n<sub>eq</sub>/cm<sup>2</sup>** @ -30 °C  
 for **50 ps** and **4 fC**