ALICE ITS3 MOSAIX stitched wafer-scale sensor Implementation challenges and solutions

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On behalf of the MOSAIX design team and ALICE collaboration

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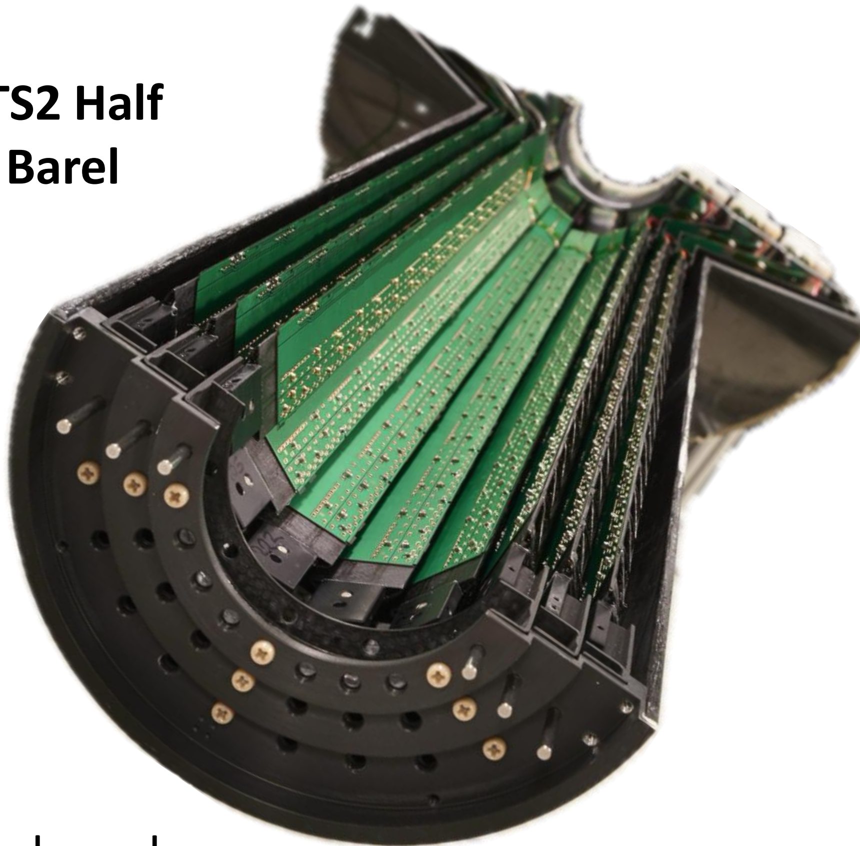
Towards ITS3

ALICE ITS2 Half Inner Barel



- Stave-based
- Flexible printed circuits with mounted sensors
- Power and data run through stave structures
- Liquid-based cooling via staves
- **Material budget 0.36% X_0 per layer**

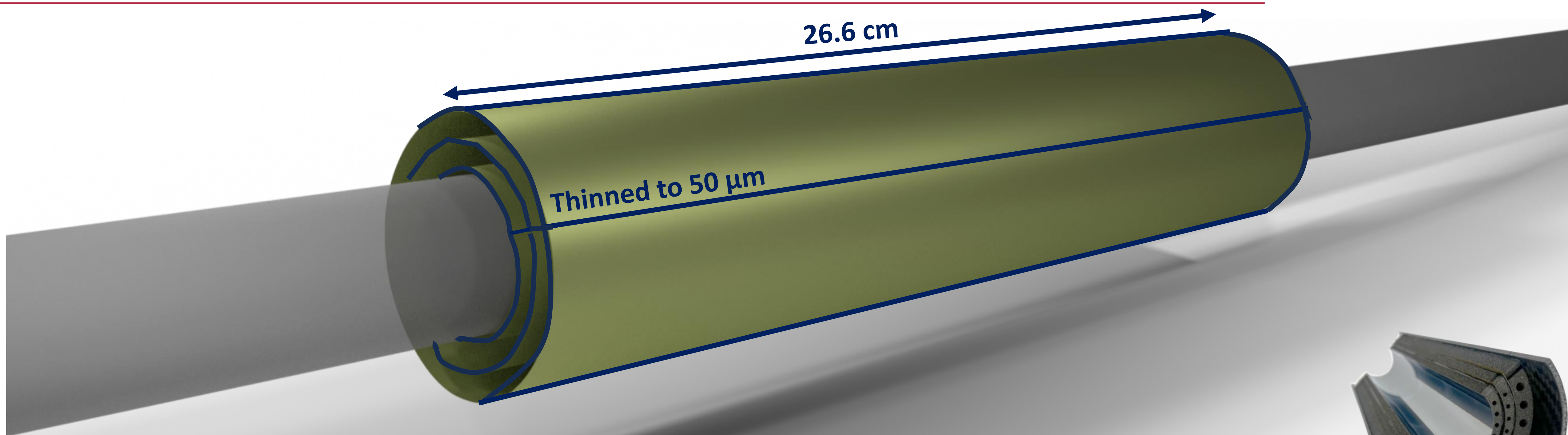
[ITS2 overview presented by Jiyoung Kim]

Towards ITS3: Silicon-only pixel detector

- Truly cylindrical
- Self supporting
- Air cooling
- **Material budget 0.09% X_0 per layer**

[ITS3 overview presented by Livia Terlizzi]

What are the challenges?



MOSAIX: full-size, full-functionality prototype for ITS3
Designed in TPSCo 65 nm technology

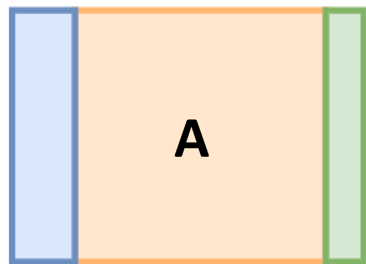
Design challenges:

- On-chip data transmission
- On-chip power distribution
- 30.72 Gb/s off-chip data transmission
- Yield management
- Low power (40 mW/cm^2)

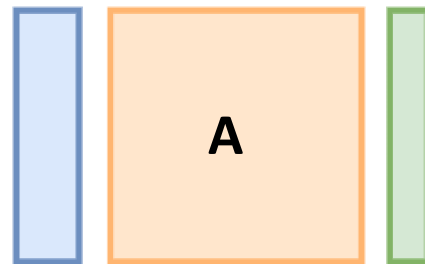
How can we build a wafer-scale sensor?

The lithography machine can only expose a limited region of the silicon wafer in one shot.

Standard Reticle



Split design reticle for stitching



A = active area

ITS3 sensor wafer map

30 mm wafer

Left Endcap (LEC)

Repeated sensor unit (RSU)

Right Endcap (REC)

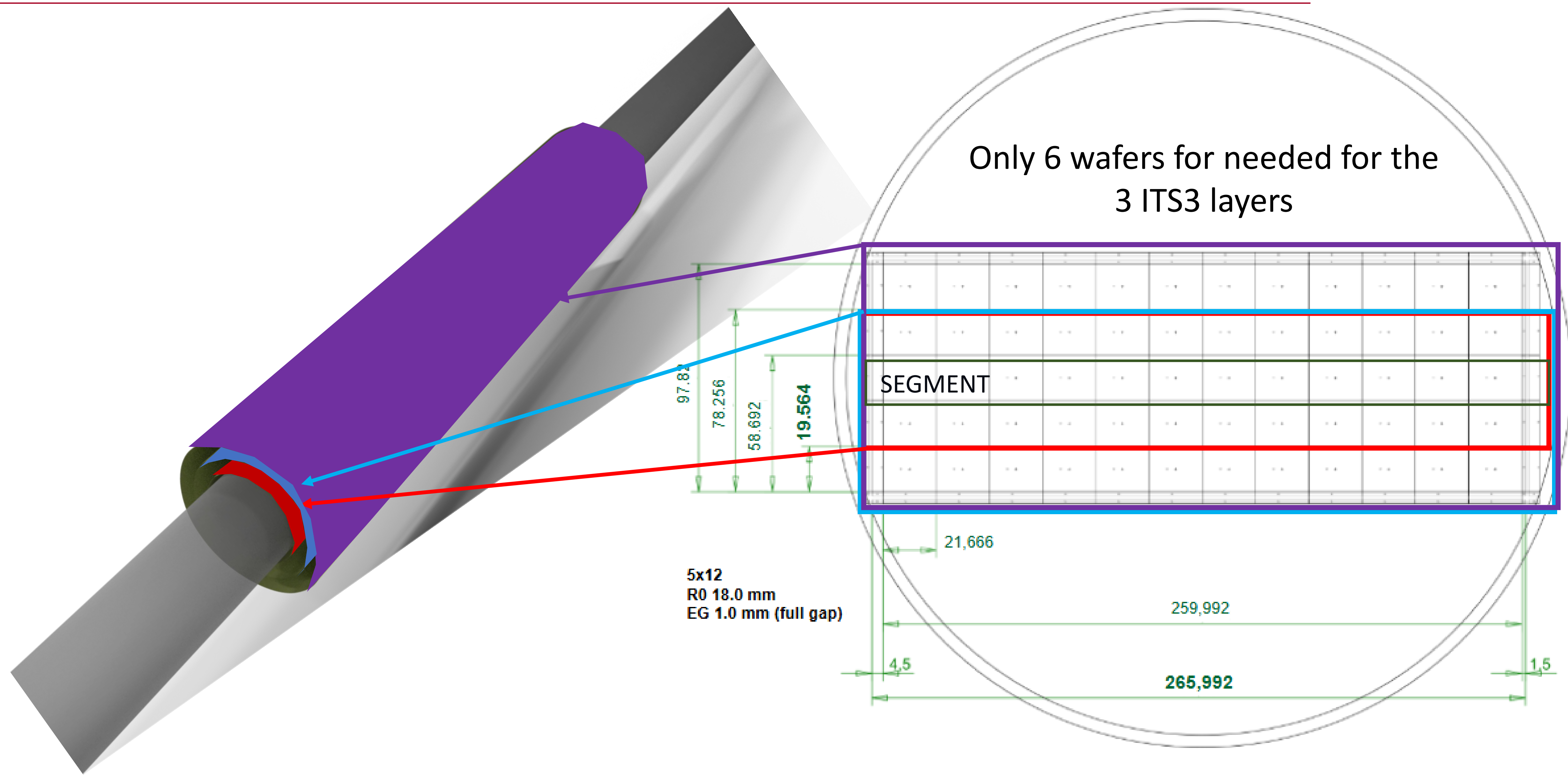
Segment: Independent stitched sensor

97.82
78.256
58.692
19.564

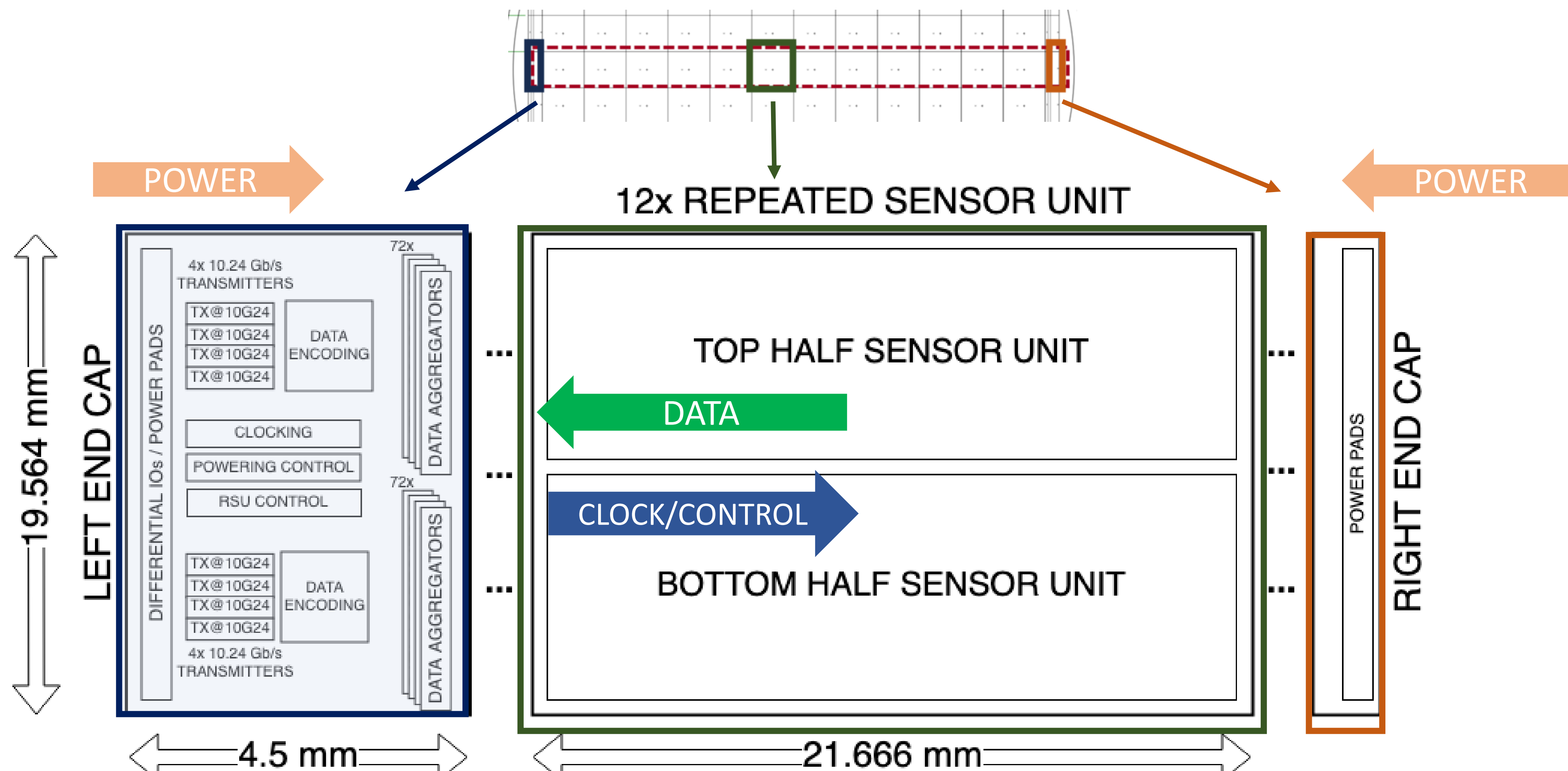
21,666
259,992
4,5
265,992
1,5

5x12
R0 18.0 mm
EG 1.0 mm (full gap)

One set of photomasks for the entire detector



The entire system on one silicon die



LEC

- Power pads and IOs
- 8 x 10.24 Gb/s serializers
- LpGBT frame encoding

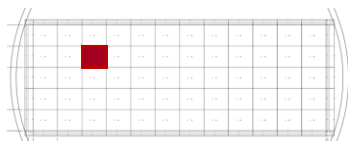
RSU:

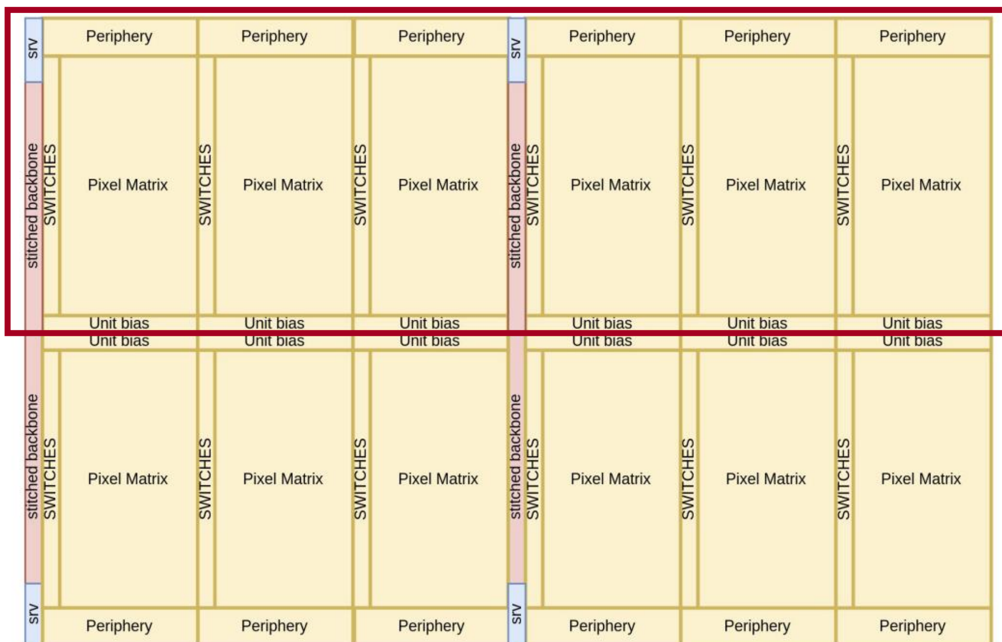
- 830k pixels/RSU
- Assembles independent building blocks

REC

- Power pads

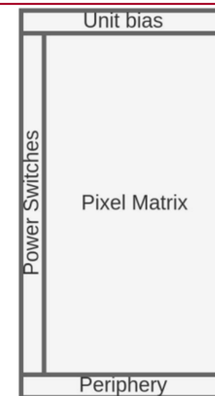
Repeated Sensor Unit - RSU





- 2 mirrored halves
- Assembled by repeating smaller building units
- 93% sensitive region

Stitched backbone:
For on-chip data and clock transmission



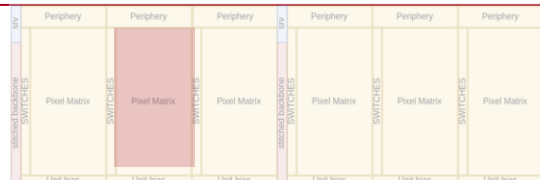
Tile

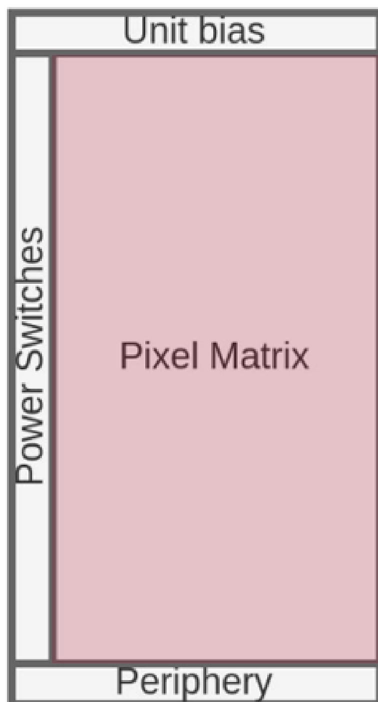
- The Building block of MOSAIX
- Can be switched on or off, bias and read out independently
- Tiles share global clock, reset and sync signals
- 144 tiles in total

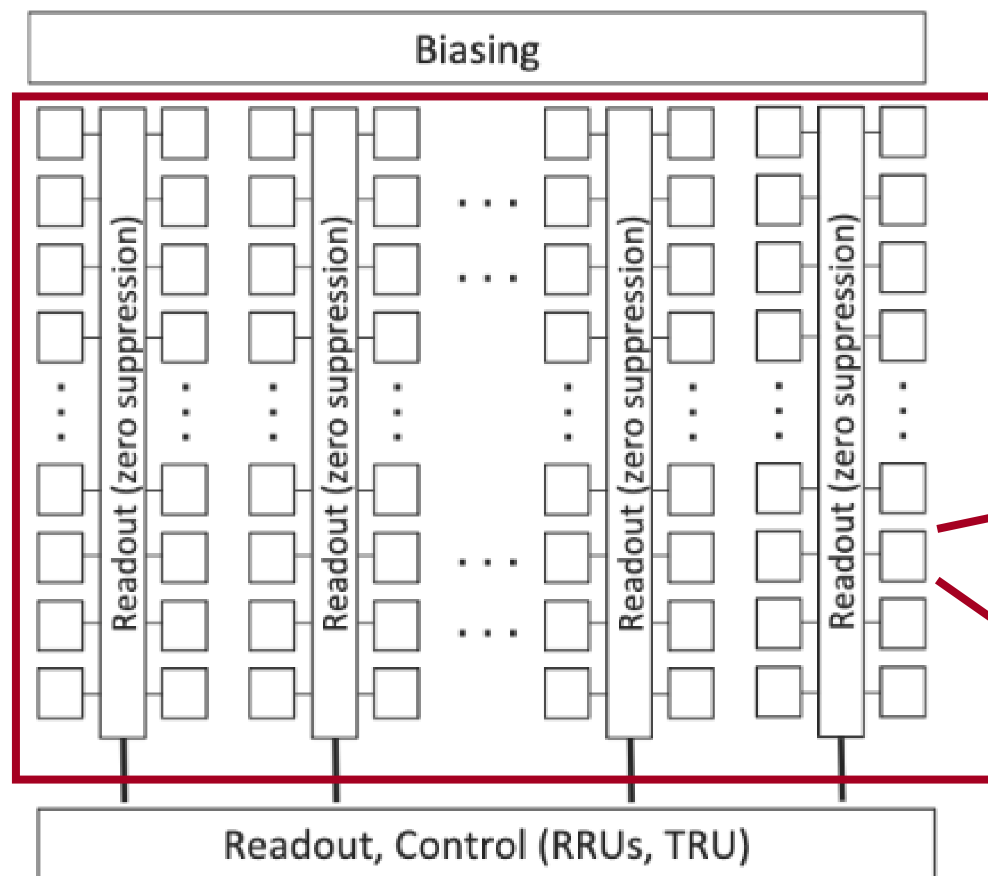
0.7% sensor area granularity

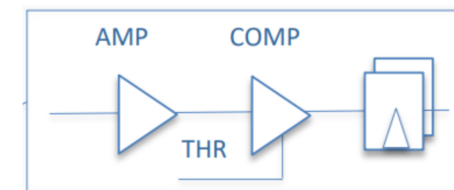
21.666 mm
10.833 mm
3.56 mm
0.090
0.020
0.06 mm
0.9 mm
9.782
STITCHED BACKBONE
SRV NODE
POWER SWITCHES
Unit Bias
TILE
PIXEL ARRAY
TX@160Mbps
PERIPHERY

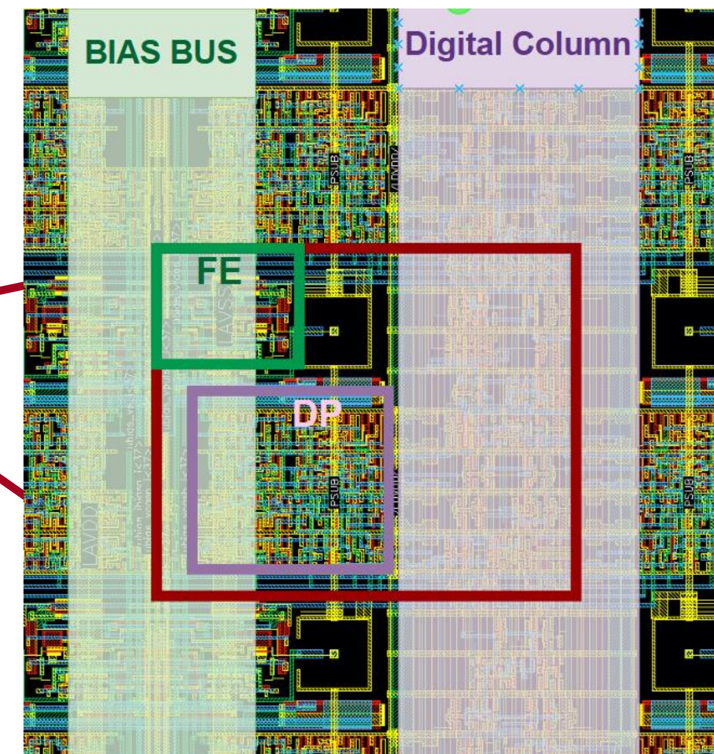
Pixel Matrix











Pixel matrix:

- 444 x 156 pixels
- 144 matrices / segment
- 9.97 Mpixels / segment

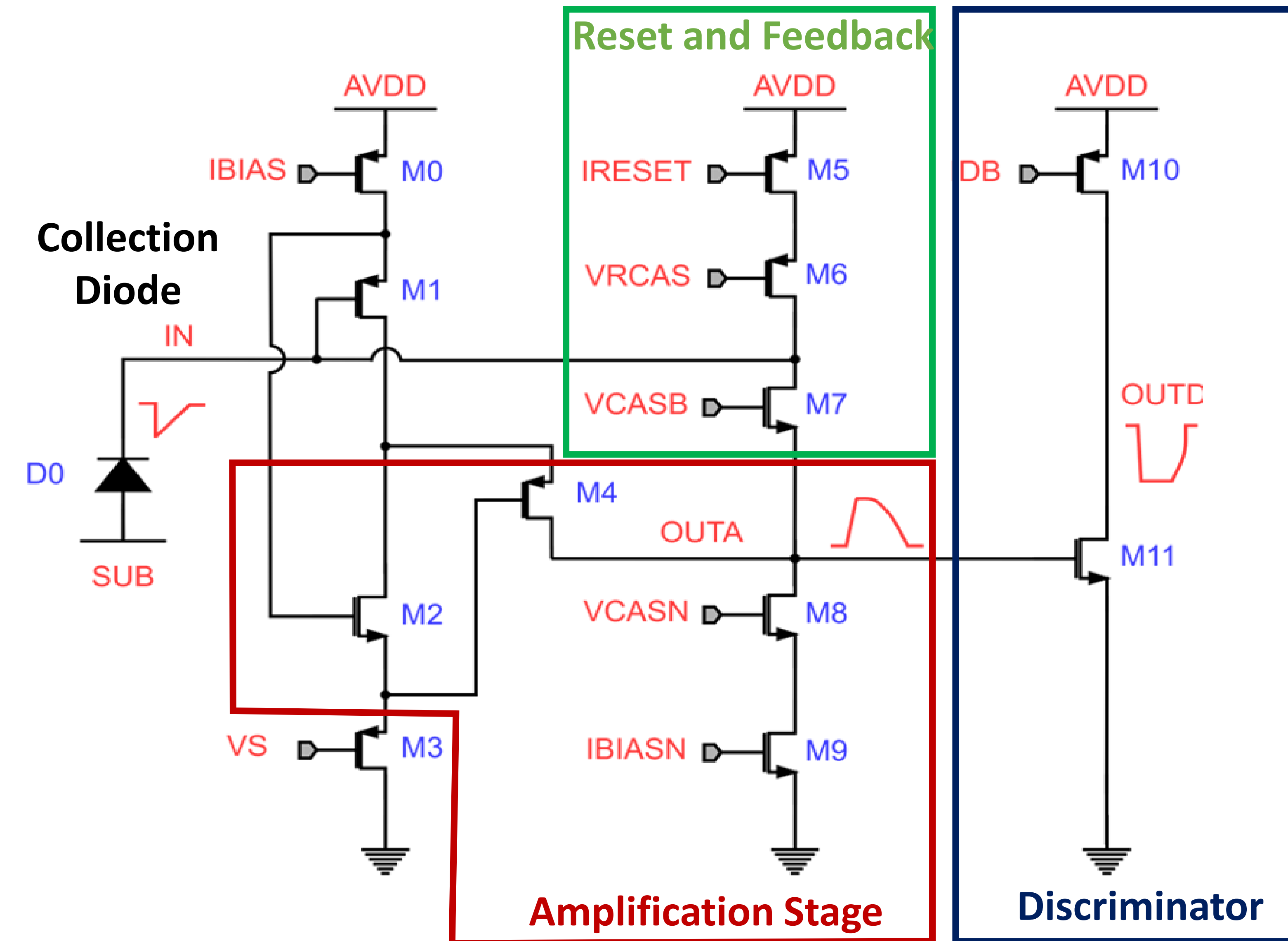
Readout:

- Double column
- Zero-suppressed with priority encoders
- Time-framed continuous (min integration window of 2 μs)

Unit bias: 6 DACs for biasing pixel FE

Pixel: Analog Front-end (FE) and Digital Pixel (DP with 2 memory registers)

Pixel Front-End



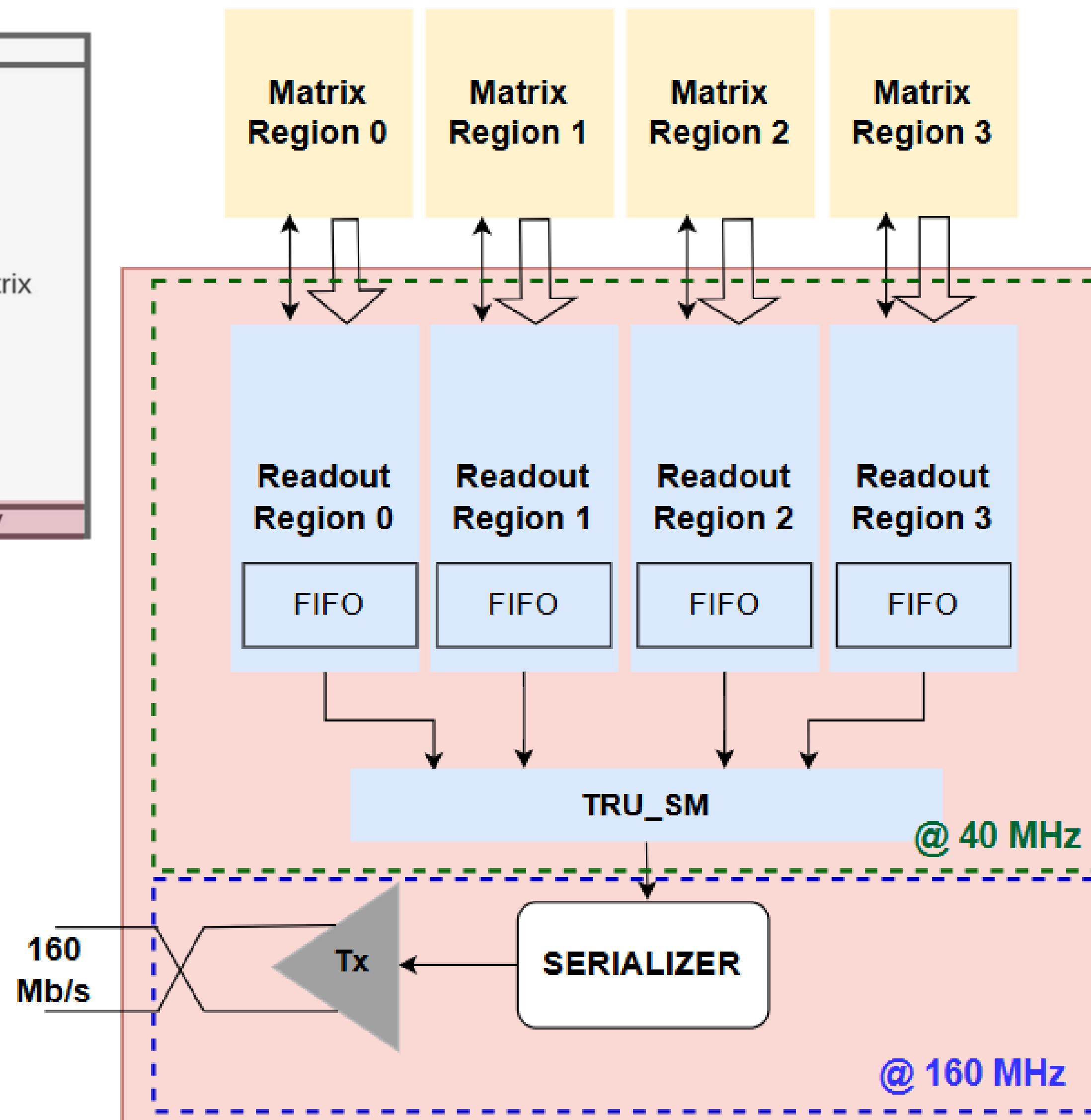
- 22.8 × 20.8 µm² pixel size
- Substrate voltage tied to -1.2V

- Designed for
  - Detection efficiency >99% at particle rates up to 4.4 MHz/cm²
  - Fake hit rate < 0.1 pixel^{-1} s^{-1}

- 12 variants included in MOSAIX (combinations of 6 font-end and 2 bias block variants)

- Frontend topology already validated with MOSS testing

Tile Periphery



High Level Diagram of the Periphery Readout

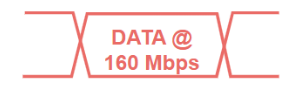
Readout:

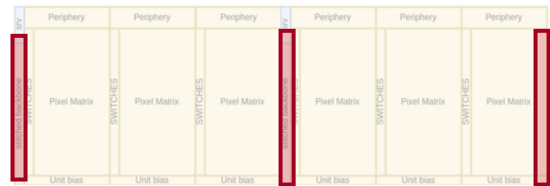
- 4 Readout Region Units
- Continuous trigger-less readout
- Physics-driven data model was used for optimal dimensioning of the readout architecture

Physical implementation:

- Digital on top implementation
- Feedback loops between periphery and matrix (2 independent implementation flows)
- Power optimization
  - Clock-gating strategies
  - Latch-based FIFOs
- Logic triplication for SEE mitigation
- Very dense block in a small area (~1 million transistors)

Stitched Backbone: on-chip clock and data transmission





10.8 mm

N+1

N

N-1

TX@160Mbps

TX@160Mbps

TX@160Mbps

TX@160Mbps

TX@160Mbps

TX@160Mbps

160 Mb/s serial data links

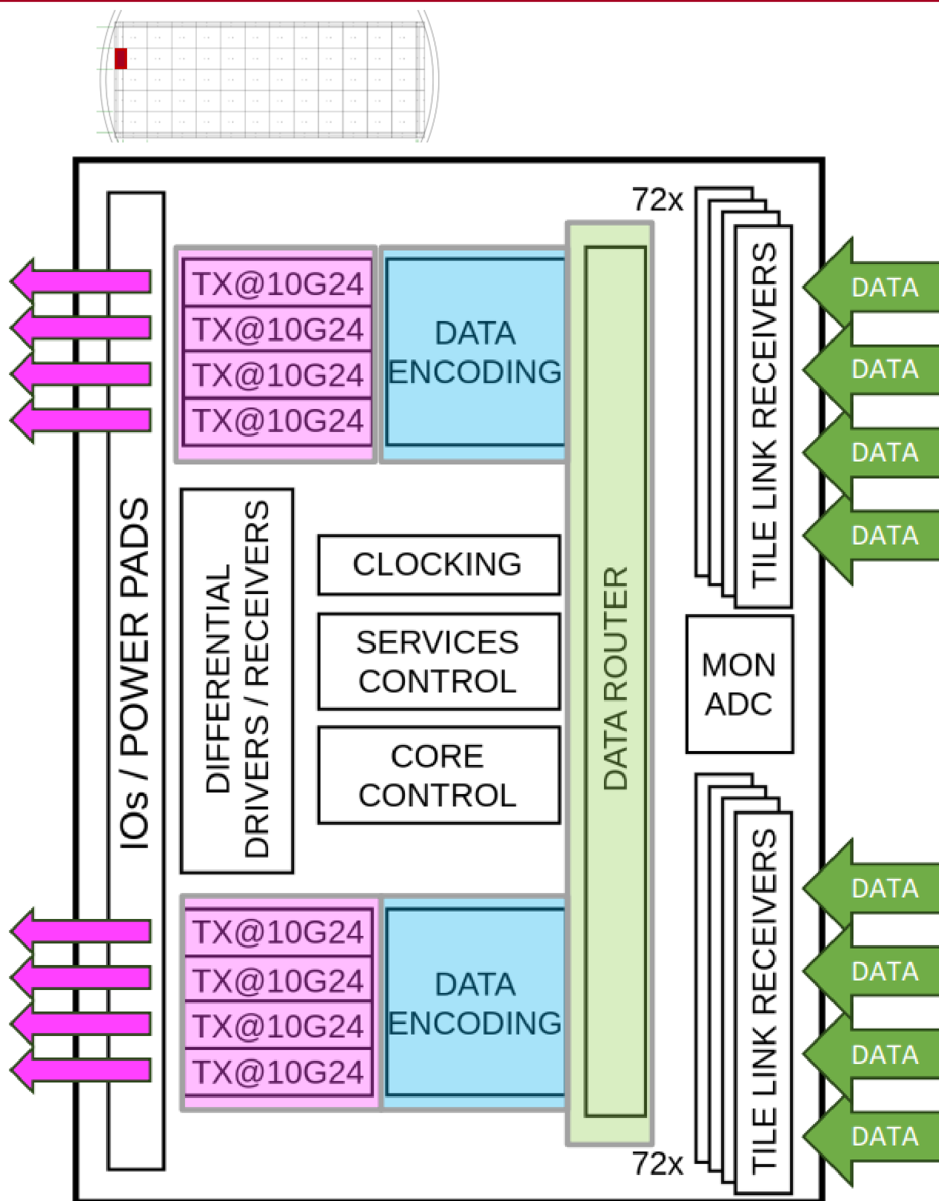
- Data lines routed over the pixel matrices
- Differential transmission with low voltage swing
- Hopping of data links to allow for stitching
- Retiming and regeneration after 10.8 mm

160 MHz clock from LEC to tiles

- Full rail to rail CMOS swing signal

- One-to-one direct connection between tile and left endcap
- 144 on-chip transmission links

Left Endcap



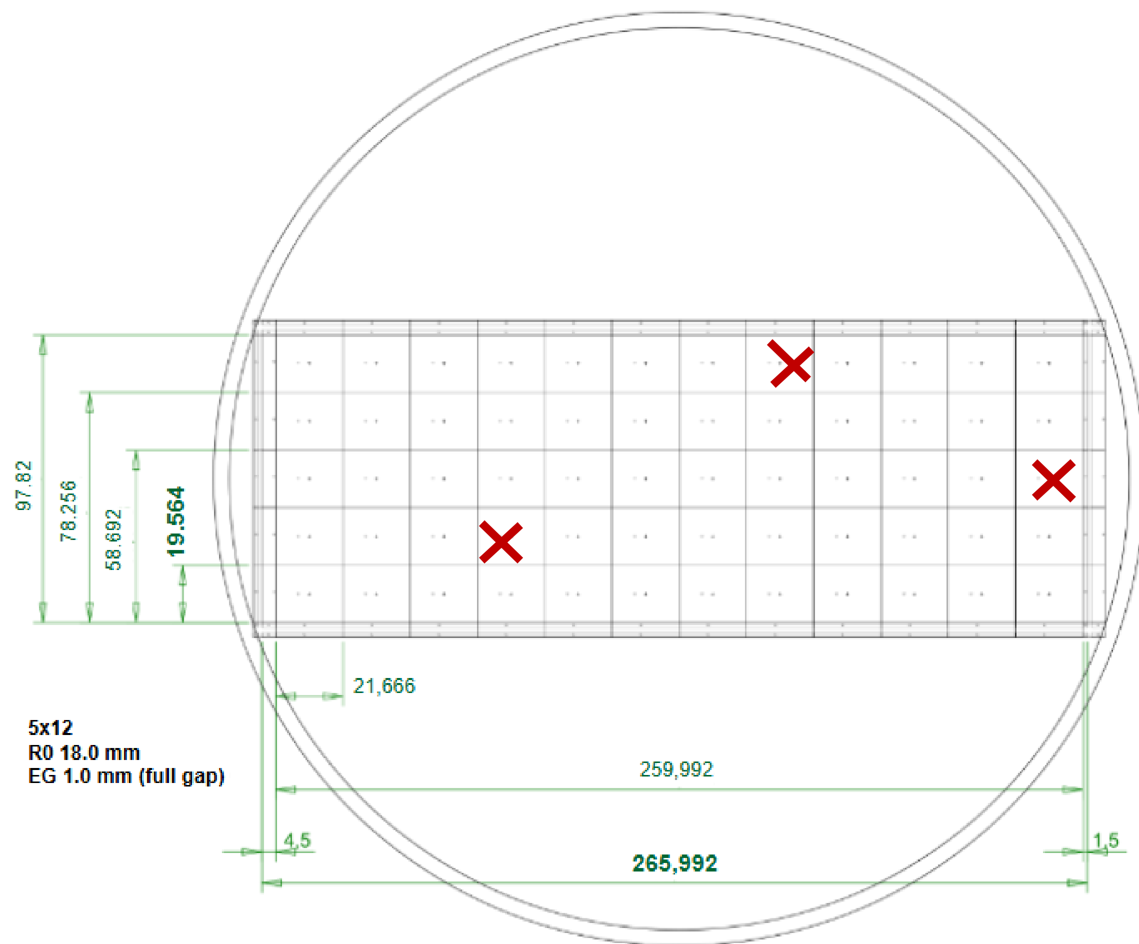
Control and data interface
- Main hub for both data and control signals
- Input capacity 144×160 Mb/s = **23 Gb/s**

LEC driving electro-optical transceivers (VTRx+) directly
- Data encoding block ported from the lpGBT chip

8 High Speed Serializers
- Driving **30 cm long lines** to VTRx+ transceivers
- **30.72 Gb/s** nominal data transmission load
- Configurable for 2 speeds
  - **10.24 Gb/s** line rate : 3 serializers are used
  - **5.12 Gb/s** line rate: 6 serializers are used
- Redundant serializers integrated to **mitigate the risk of failures** of off-chip optical link components
- Unused serializers are switched off

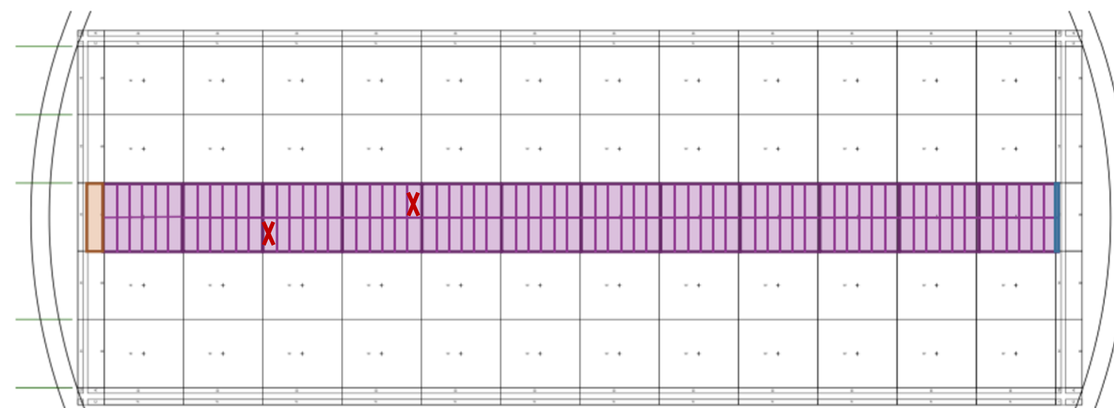
All IOs connected via the short edge
- Very limited resources

How to ensure high yield at this scale?



Operation with a few defects must be possible:

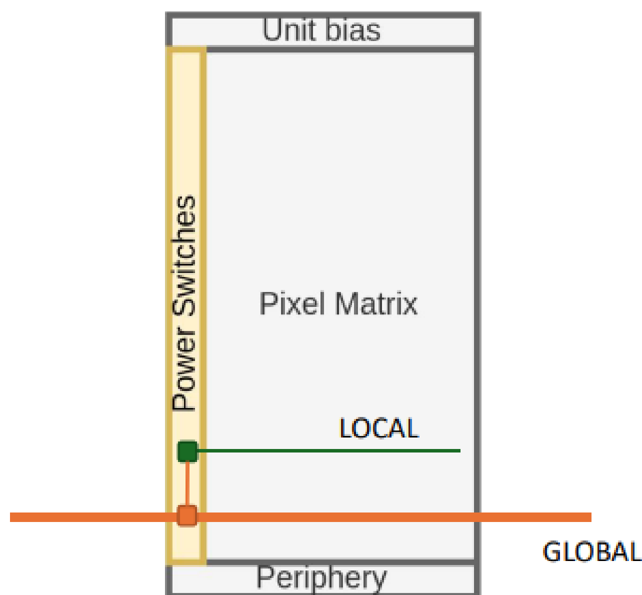
- Modular design and segmented power
  - Each tile can be switched off independently
  - 0.7% chip area granularity
- Probability of shorts needs to be minimized



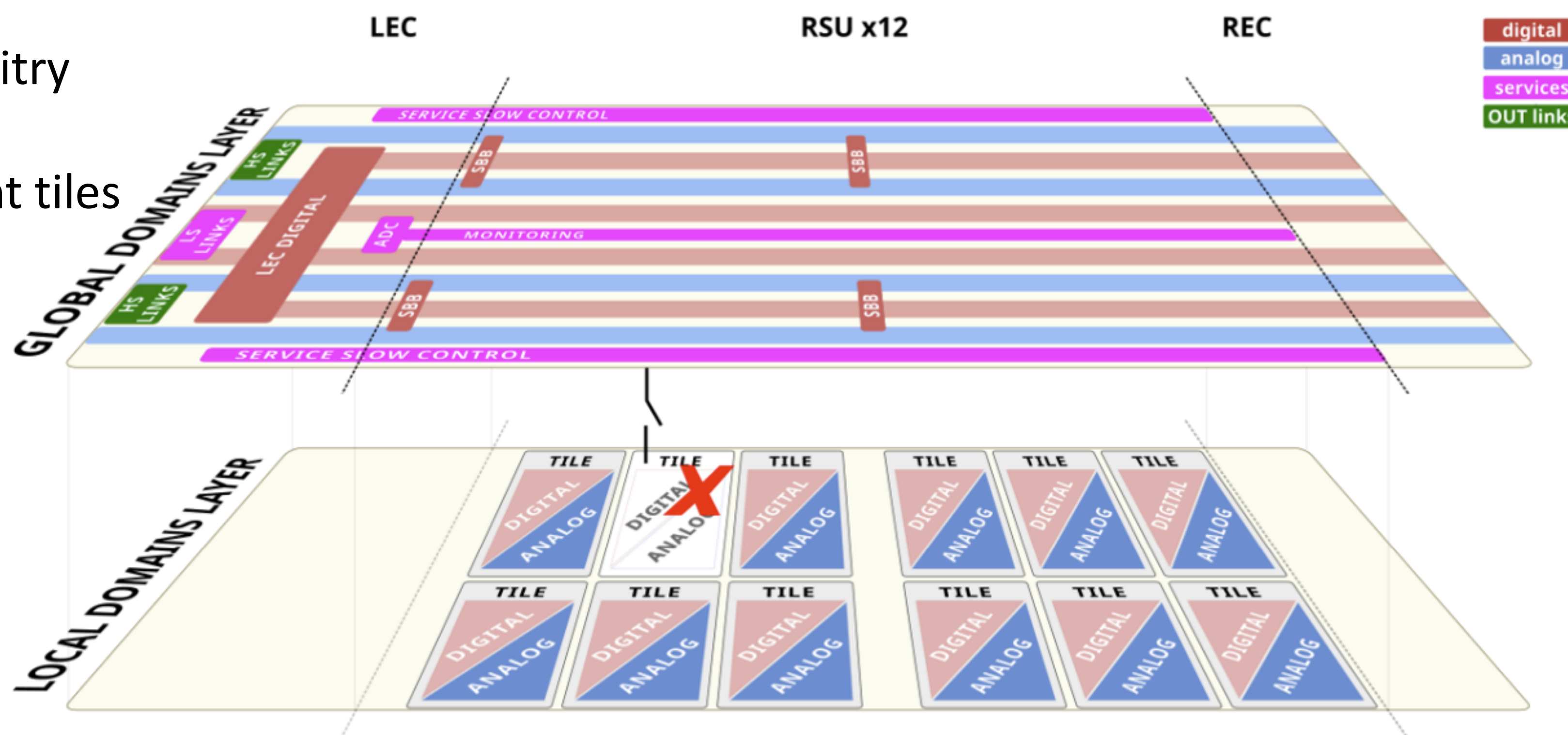
Power segmentation

Two powering layers

- GLOBAL
  - supplies only configuration circuitry
- LOCAL
  - segmented into 144 independent tiles
  - allows defects isolation



Power switches to connect or disconnect the tile from the global power network



Disconnecting a tile increases dead area by 0.7%, but without affecting the overall functionality.

[1] S. Bugiel et all Power distribution over the wafer-scale monolithic pixel detector — MOSAIX for ALICE ITS3

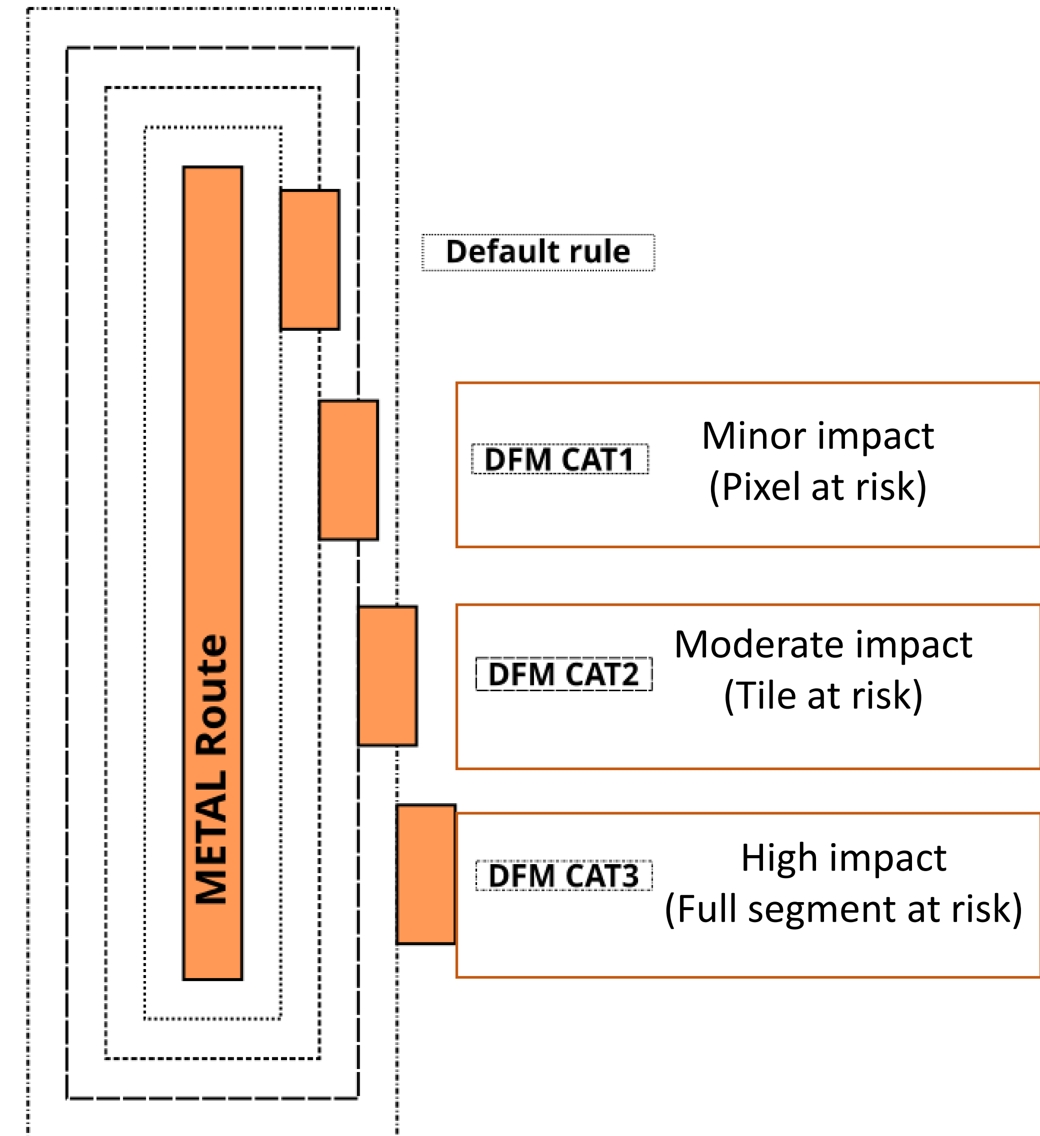
Conservative design rules and custom libraries

Custom design rules

- Sub-blocks categorized by their failure impact
- Custom design rules for each category
- Power nets follow the strictest spacing constraints
- Analog building blocks fully implemented with custom rules, Digital blocks partially

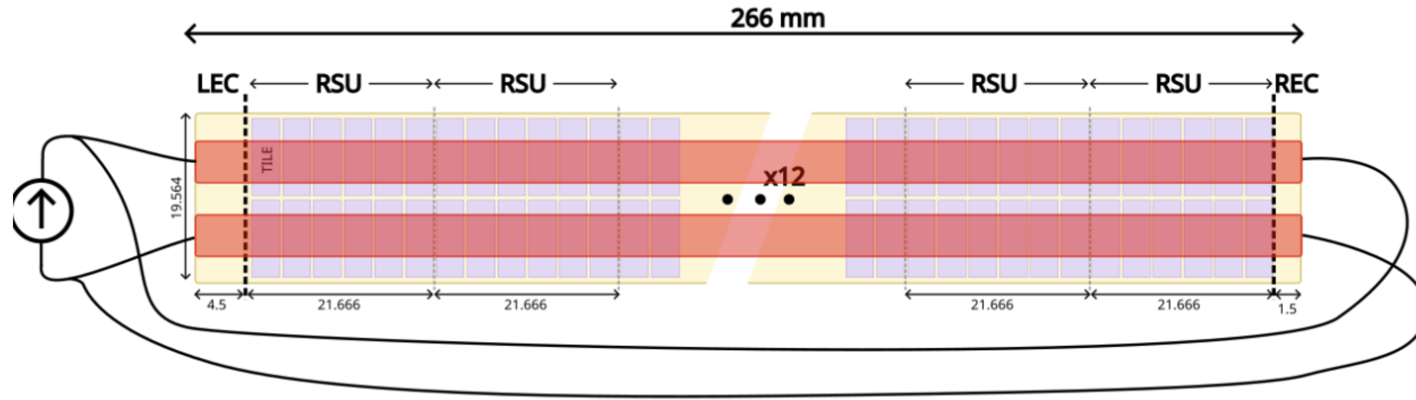
Custom cell libraries, combining changes for:

- Low-leakage
  - Increased gate length
- Design for manufacturability (DFM) improvements
  - Wider metal tracks, bigger metal spacing
  - Double contacts
- Additional change for in-matrix cells
  - Substrate connected to -1.2V



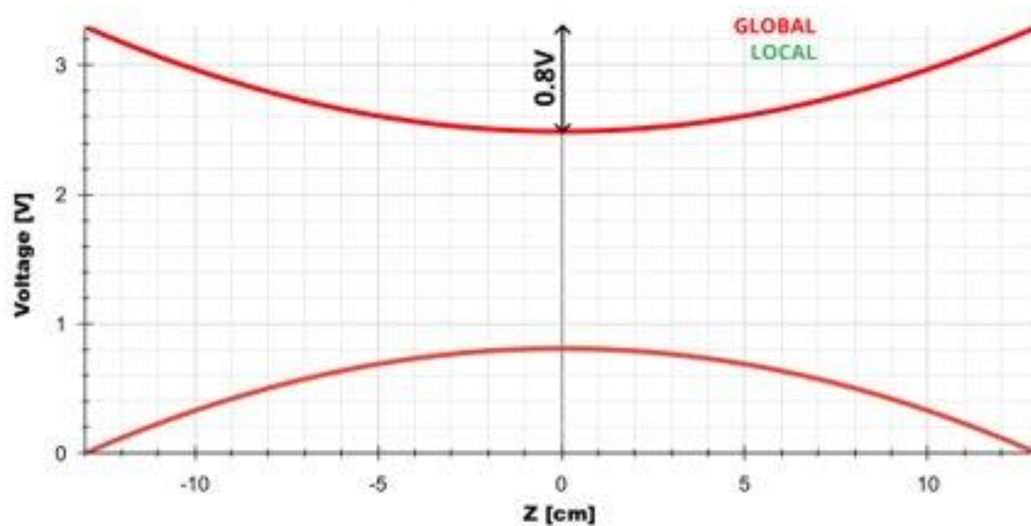
Example of custom rules for MIN spacing

Power distribution over the large area

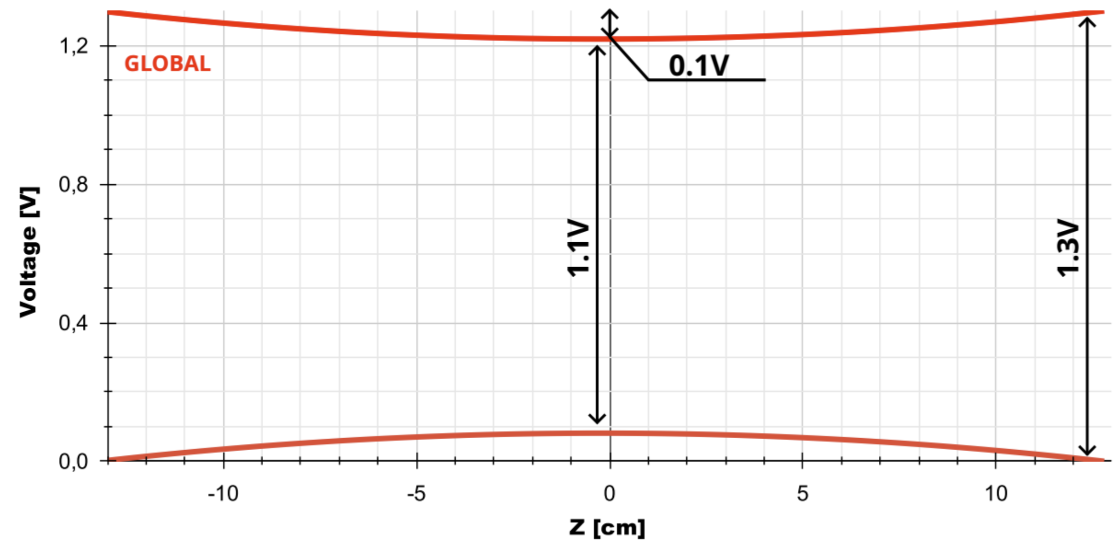


- Power connections only to short edges and spread over 26 cm
- Metal stack changed during design phase
- With the new metal stack, the IR drop was significantly reduced

IR drop estimate with the initial metal stack

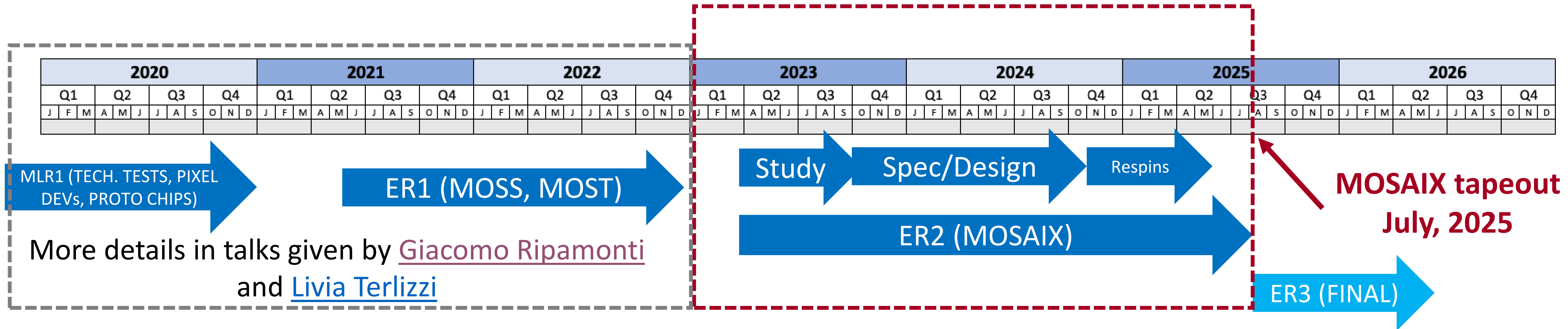


IR drop estimate with the final metal stack



Power grid validated to satisfy specifications < 100 mV worst case IR drop on global supplies

MOSAIX development and verification



Signoff Verification:

	Tests	Runtime
Functional	Tile: 98k tests rsu+lec+mosaix: 10k tests	28 days 4 days
Gate Level	15k tests per corner	20 days
Single Event Effects	rtl – 40k tests gate level – 5k tests	15 days 10 days
Power-aware	2k tests	4 days

Conclusions

- First stitched sensor in a HEP environment designed as a **full-scale, full-functionality prototype** (26.6 cm x 1.96 cm) for the **ALICE ITS3 upgrade** designed in **TSPCo 65 nm CMOS** imaging technology

- **Breakthrough in scale and complexity:** ~230M transistors per RSU, ~3B transistors in total
- **30. 72 Gb/s** off-chip transmission, **9.97 Mpixels** in total**, 22.8 x 20.8 μm²** pixels, with detection efficiency **above 99%, 40 mW/cm²** power consumption

- Complex integrated system with **on wafer power and signal transmission**

- Full system verification, functional and physical implementation with full **digital on top design**

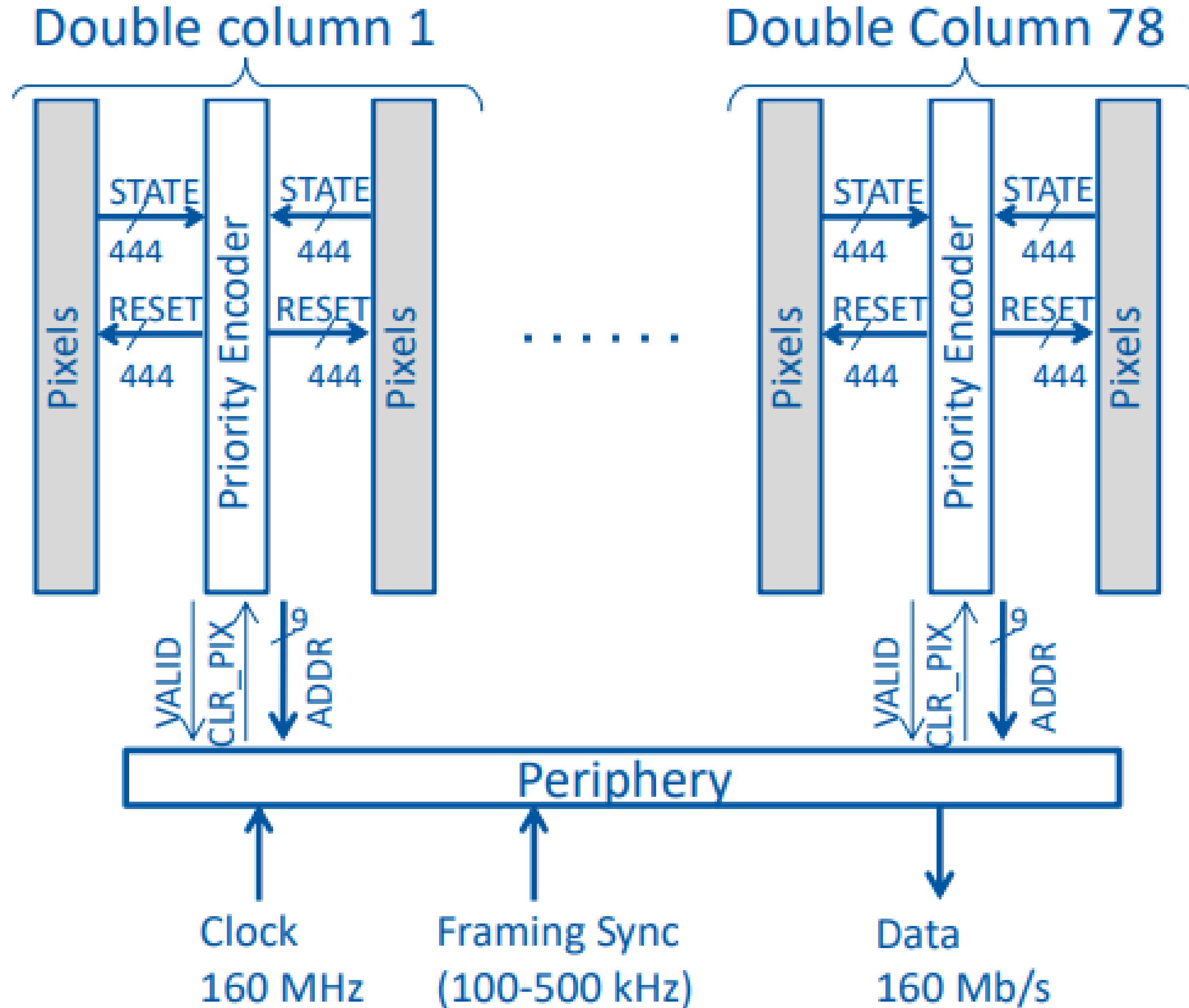
- MOSAIX taped out in **July 2025**, ER3 planned for 2026

Thank you for the attention!

MOSAIX key specifications

Fill factor	93 % sensitive region
	0.7 % sensor area modularity
	144 tiles (independent units)
Pixel performance	$22.8 \times 20.8\,\mu m^2$ pixel size
	Detection Efficiency >99 %
	Fake hit rate <0.1 $pixel^{-1}\,s^{-1}$
Data taking	4.4 MHz/cm^2 particle rate
	30.72 Gb/s off-chip data transmission
	minimum 2 μs integration time
Radiation performance	10^{13} NIEL (1 MeV n_{eq}/cm^{-2})
	10 kGray TID
	Triple modular redundancy
Power budget	40 mW/cm^2

Pixel Matrix Readout

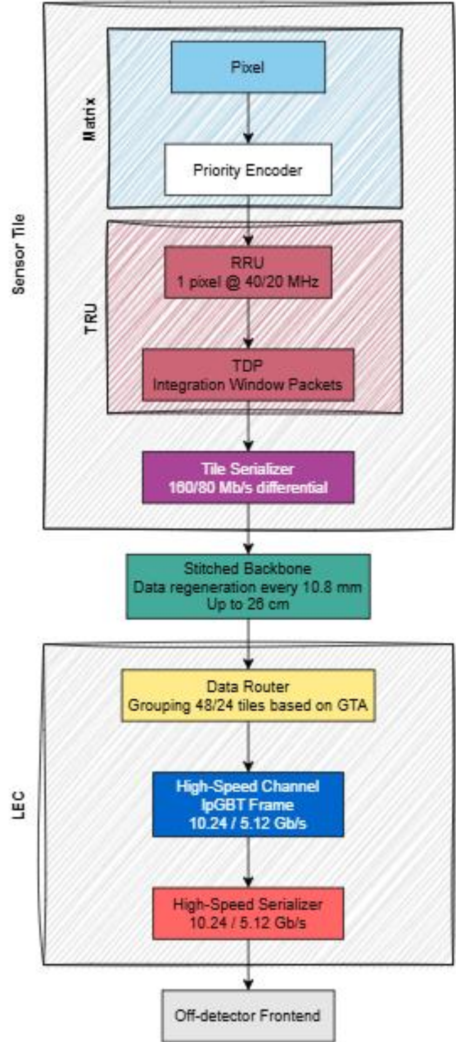


PE is fully combinatorial circuit
No free clock over matrix
No activity where there are no hits

Periphery builds and transmits one data packet for each framing interval (2-10 μs)

Global SYNC signal aligns in time the integration intervals across all the tiles

Data Flow and Tile Periphery



PERIPHERY

SBB

Status Sticky Bits Logic

Slow Control Tile Register...

Analog Parameters Mux

Matrix Configuration Logic

Unit Bias

Power Domain Interface Wra...

Sensor Tile Address Decoder

Reset Synchronizer

SBB Tile

Clock Divider

Pixel Matr...

Tile Serializer

TRU Ouput Scaler

TRU

Sync Synchronizer

Test Vector Generator

Text is not SVG - cannot display