

Phase-2 Upgrade of the ATLAS Inner Tracker

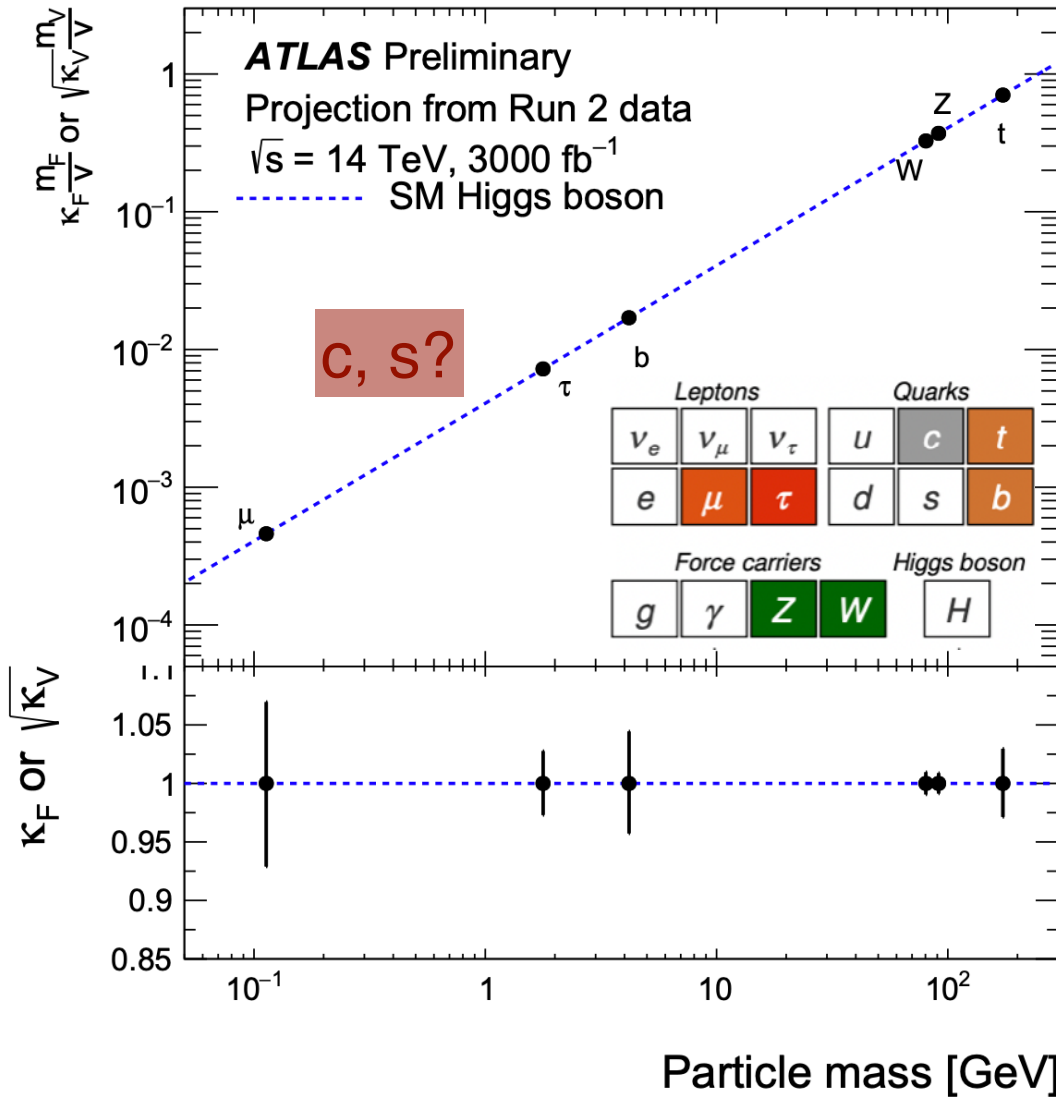
Caterina Vernieri

On behalf of the ATLAS ITk Collaboration



25th – 29th August
VERTEX25
The 33rd International Workshop on Vertex Detectors
Student Union, University of Tennessee Knoxville

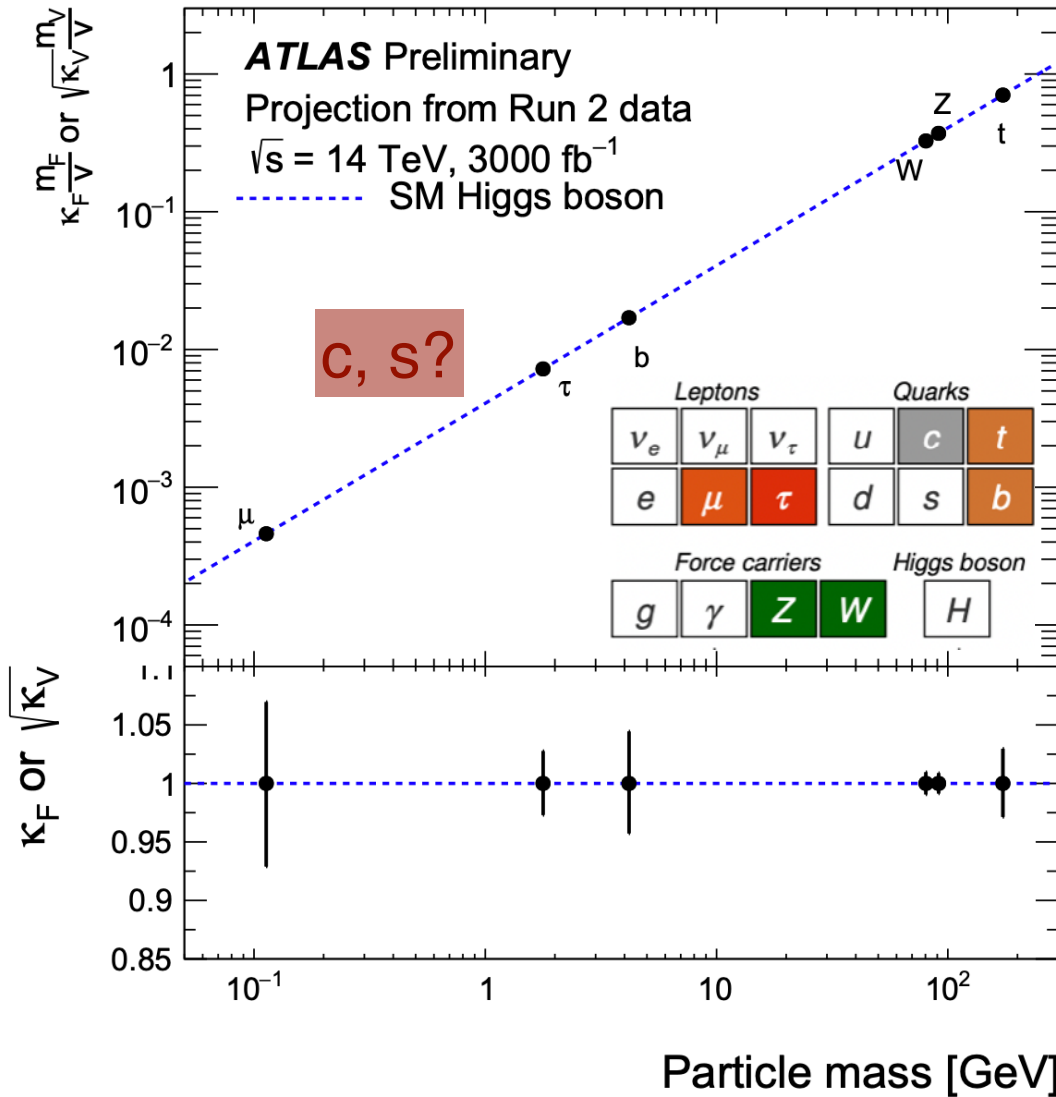
Higgs at HL-LHC



The High Luminosity era of LHC will dramatically expand the physics reach for Higgs physics:

- **2-5% precision for many of the Higgs couplings**
- **BUT much larger uncertainties on $Z\gamma$ and charm and $\sim 30\%$ on the self-coupling**

Higgs at HL-LHC



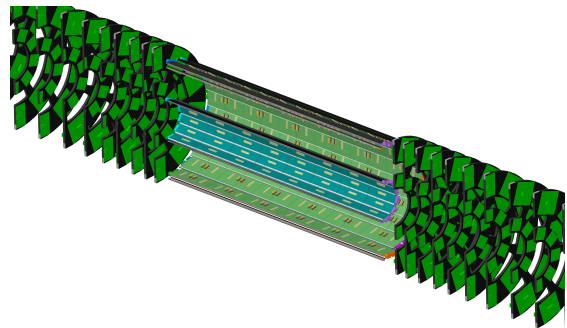
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Light Yukawa out of reach in the LHC environment

LHC → High Luminosity LHC

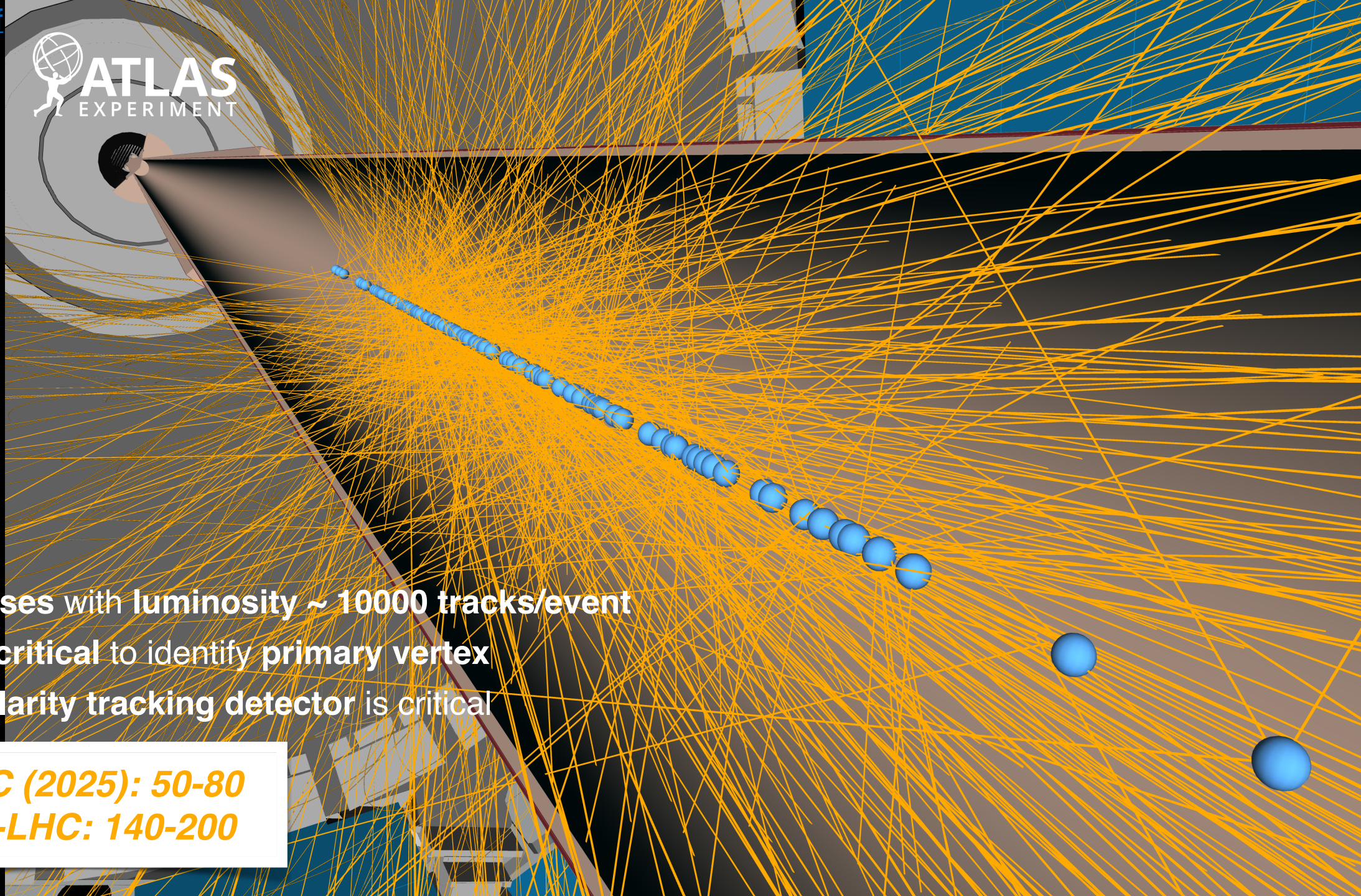
HL-LHC schedule



TODAY

Phase-2 HL-LHC detector upgrades are being built





Pileup increases with luminosity ~ 10000 tracks/event
z position is critical to identify primary vertex
High granularity tracking detector is critical

LHC (2025): 50-80
HL-LHC: 140-200

The upgrade of the Tracker Detector for HL-LHC

A new, whole-silicon, tracker (ITk) to maintain physics performance in the harsher HL-LHC environment

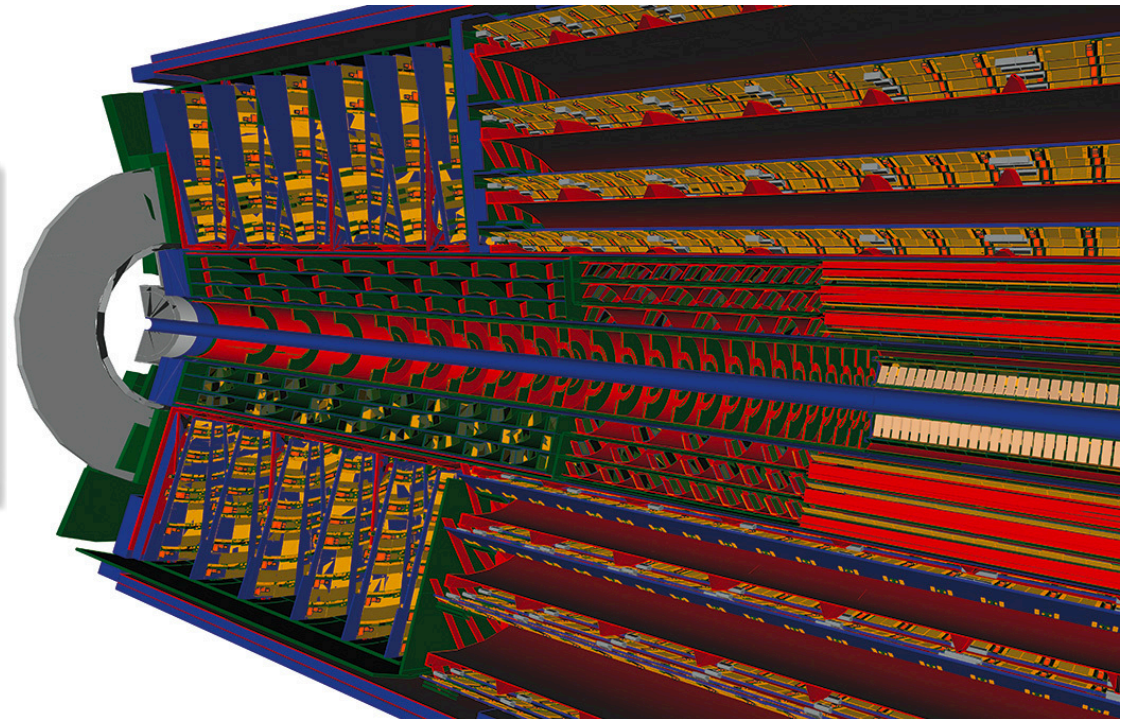
- LHC energy and luminosity increase: operate up 7.5×10^{34} Hz/cm², i.e. 200 PU
- Sustain radiation tolerance up to 10x the dose expected during LHC
- Readout to be compatible with a trigger decision rate ~ 1 MHz 10x increase

Extended tracking acceptance, up to $\eta \sim 4$

Operated at -35C to mitigate radiation-induced damage and prevent thermal runaway

Improved electronics

Smaller Pixel size, occupancy at per mille level



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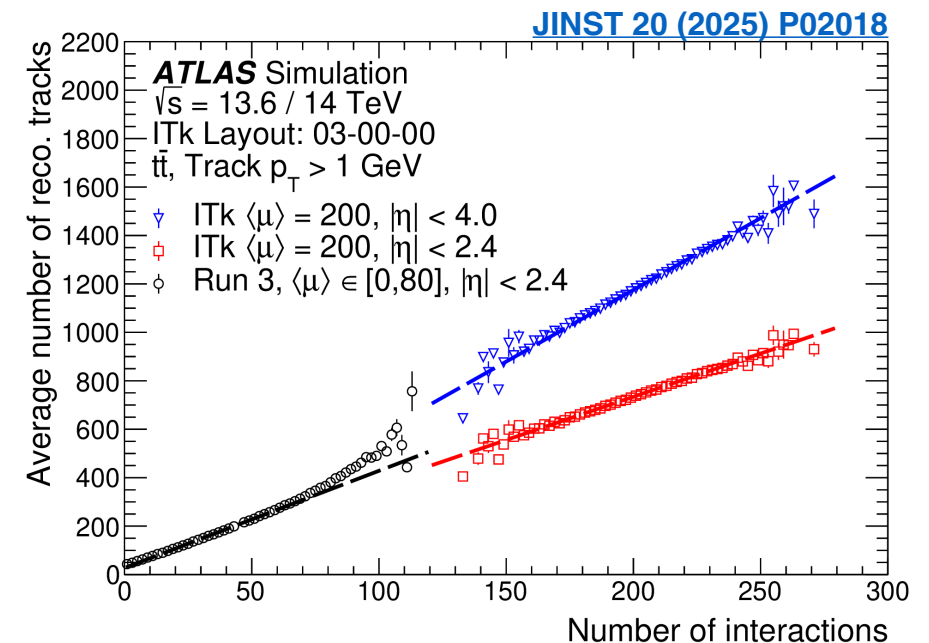
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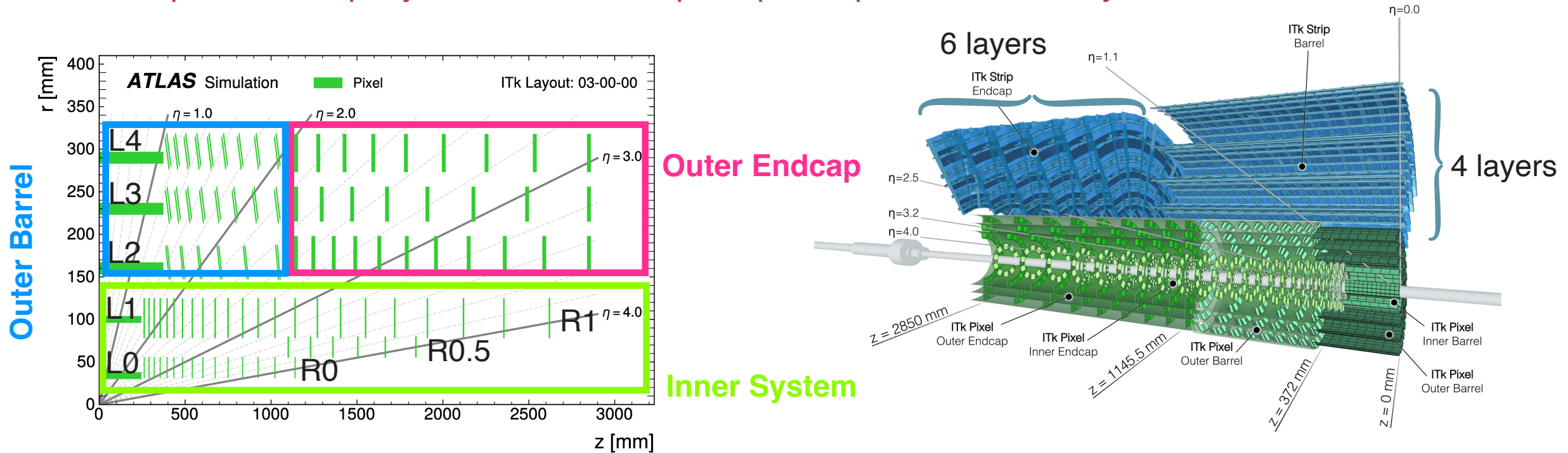
Improved electronics

Smaller Pixel size, occupancy at per mille level



ITK Layout, the largest silicon detector

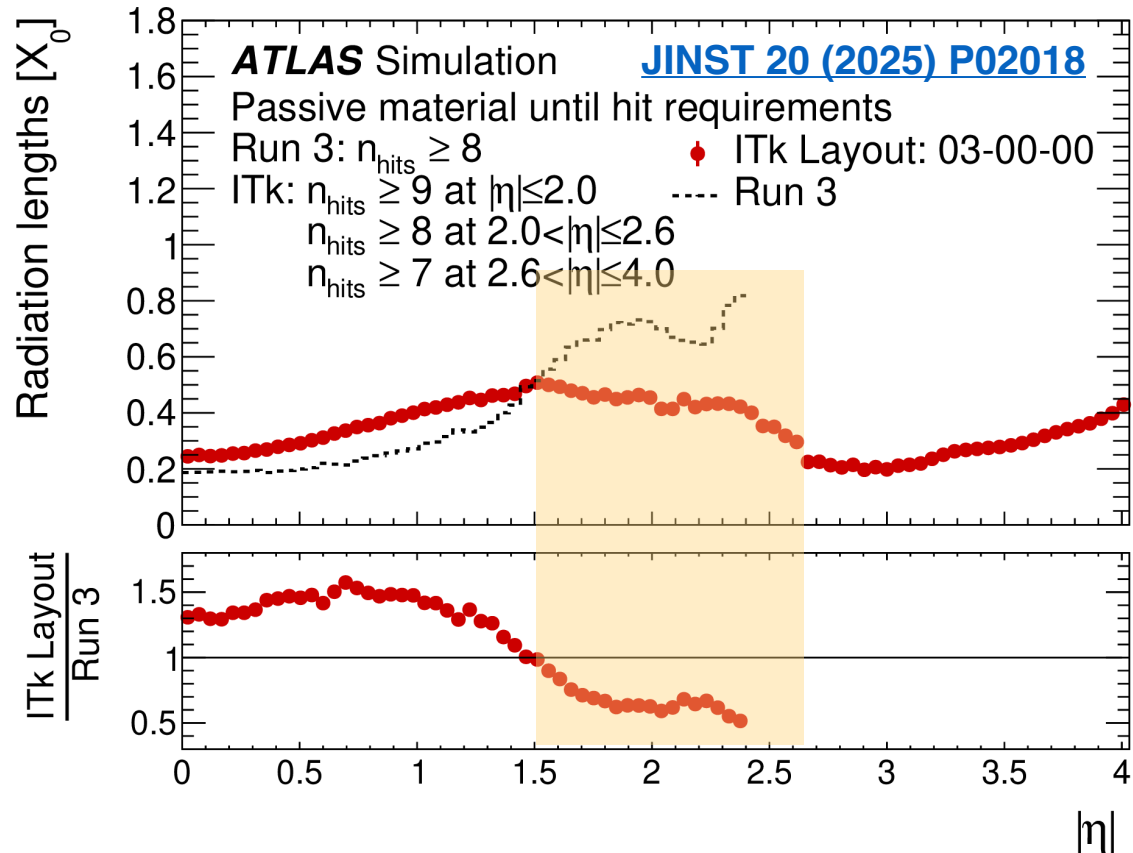
ITK: 5 pixel + 4 strip layers → at least 9 space points per track. First layer at 33 mm from the IP



	Eta Coverage	Pixel (m ²)	Pixel Channels	Pixel Modules	Strip (m ²)
Current Tracker	$ \eta < 2.5$	2	80×10^6	1.7 K	68
ITk	$ \eta < 4.0$	13	5.1×10^9	8.3 K	165

One more challenge: Material Budget

Additional layers of silicon & more channels compared to the ATLAS current detector (ID+TRT)



- **CO₂** two-phases cooling system
- **Carbon fiber structures** for local supports
- **Link sharing and serial powering** to reduce number of readout and power cables respectively

Pixel services: optical conversion outside the detector volume

Higher granularity

Small pixels → Low occupancy, improved impact parameter resolution.

ITk will feature :

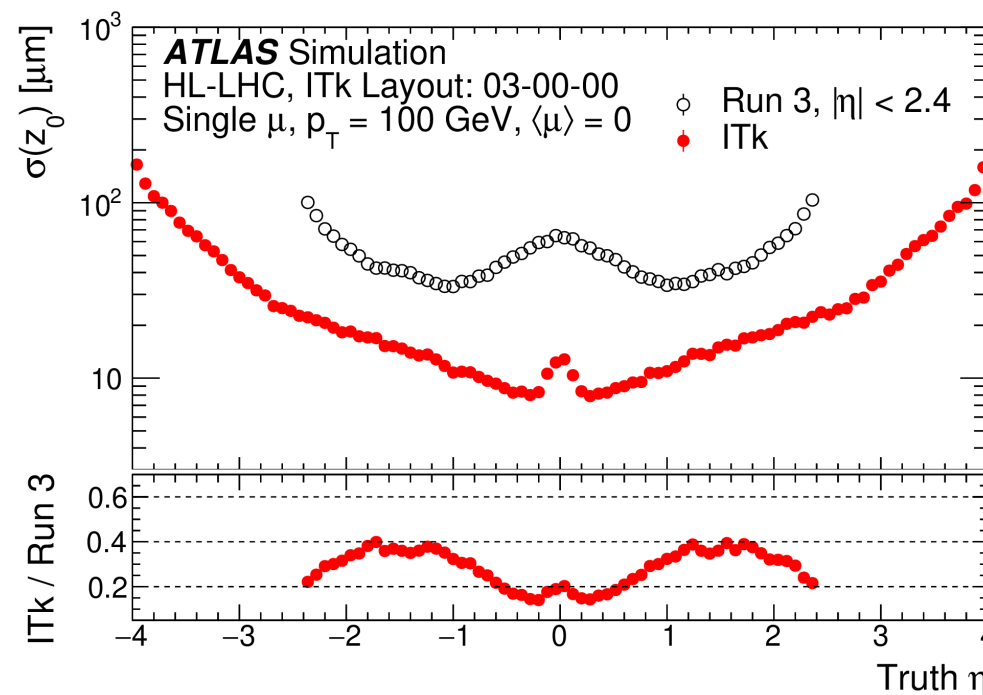
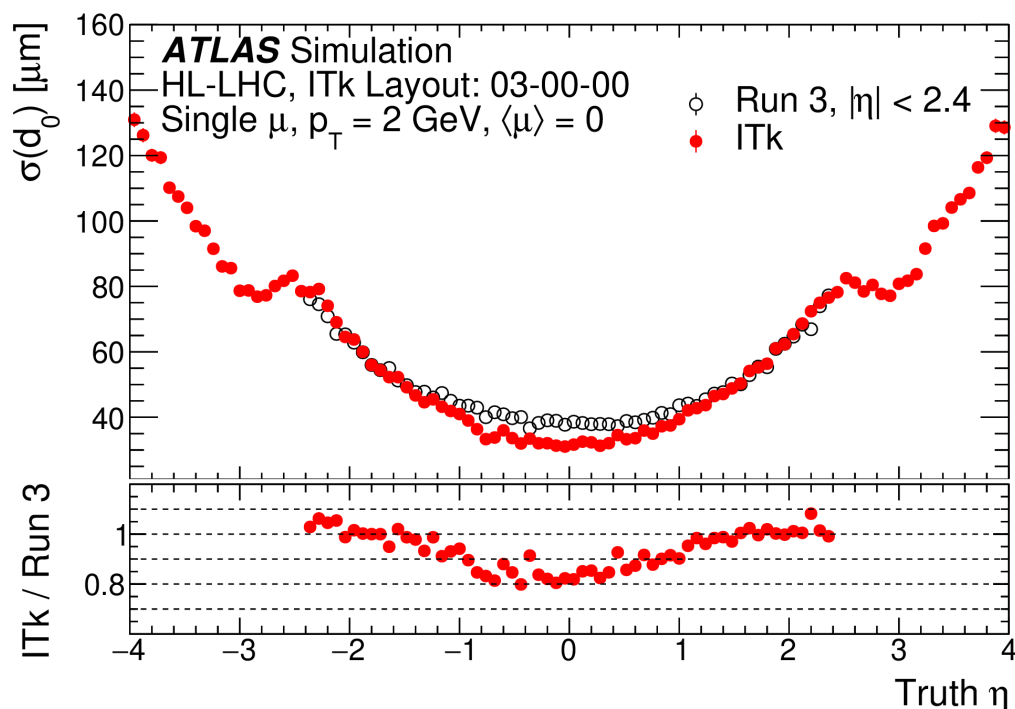
25 x 100 μm for the innermost layer of the barrel (L0)

50 x 50 μm pitch everywhere else

Run-3

50 x 250 μm for the two innermost layers

50 x 400 μm pitch everywhere else

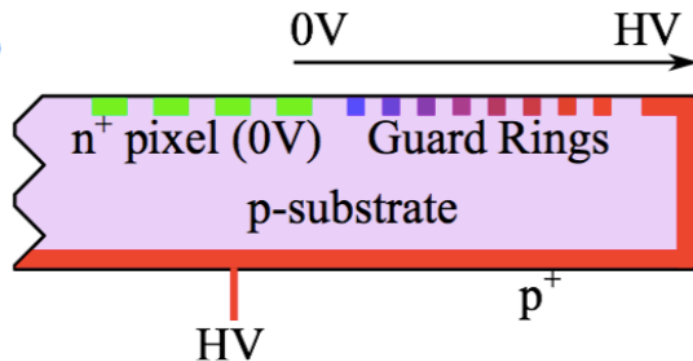
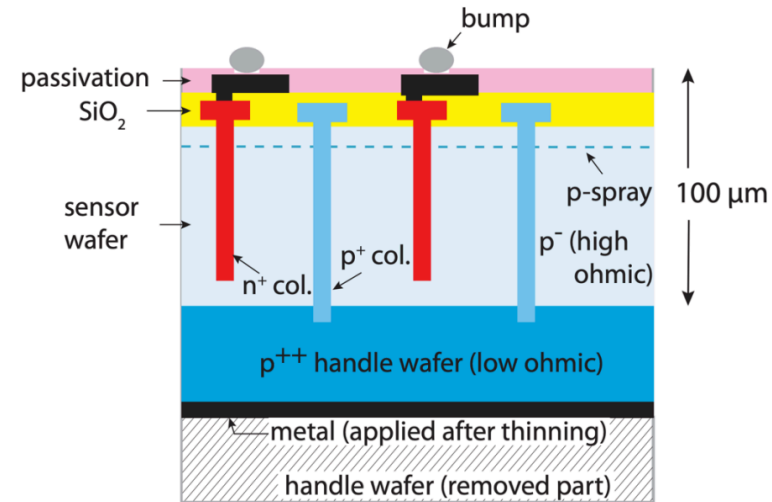
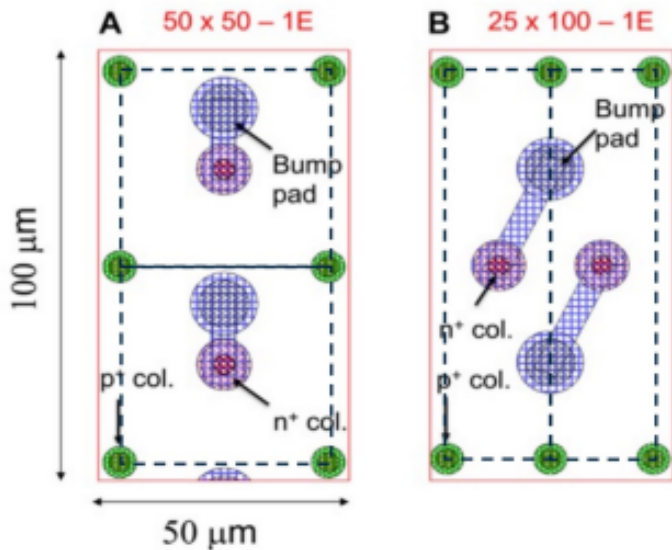


JINST 20 (2025) P02018

The tracking efficiency in the central region of the ITk detector is within 5% to the one of the Run 2

Pixel Sensors

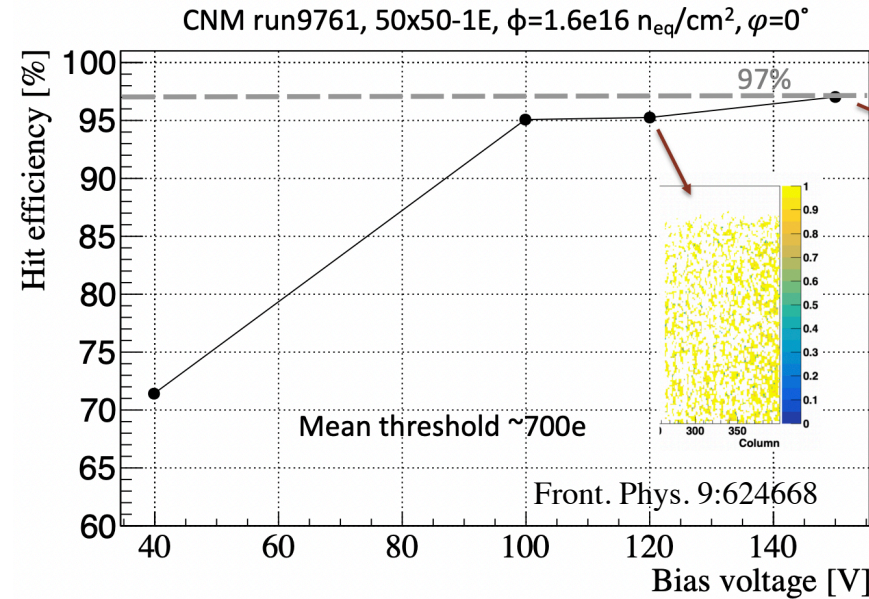
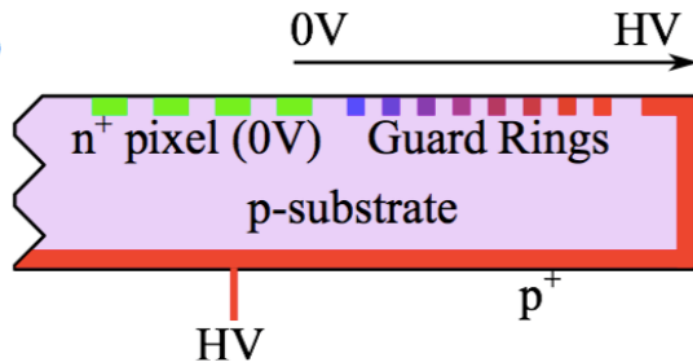
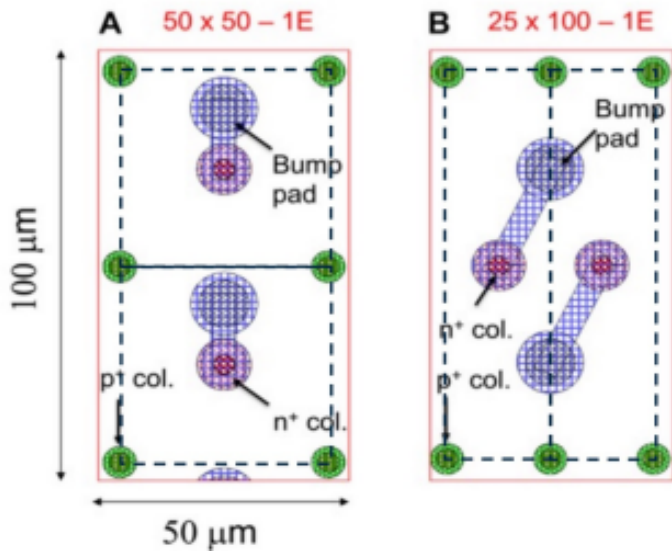
Thin active substrates (100-150 μm) \rightarrow Reduced cluster size and data rates



- For L/R0 3D sensors (**25 μm x 100 μm or 50 μm x 50 μm)** with new single-side technology
 - Bias <150V
 - Radiation hard up to $\sim 1.6 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
 - Vendors: SINTEF, FBK
- For R/L1+ layers feature **n-in-p planar sensors (50 μm x 50 μm)**
 - 100 μm for the innermost layer, then 150 μm
 - Radiation hard to $\approx 4 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
 - Bias voltages up to 600 V
 - Vendors: HPK, Micron, FBK

Pixel Sensors

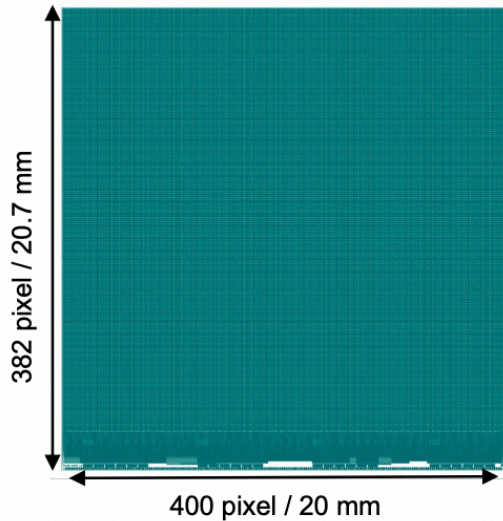
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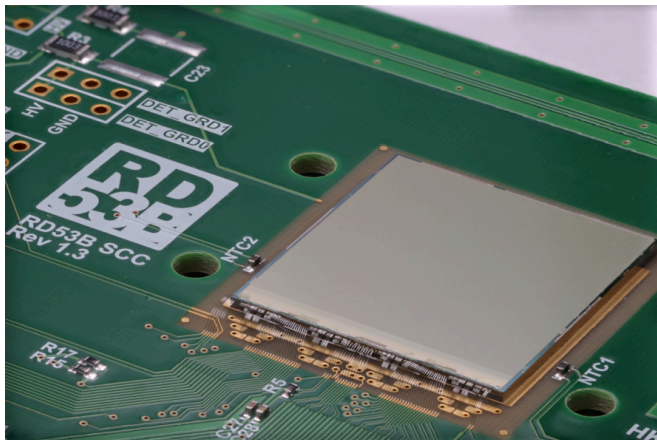
Pixel Front End

RD53 Collaboration shared between ATLAS and CMS R&D - a decade long development



New Front-end ASIC in 65 nm CMOS technology

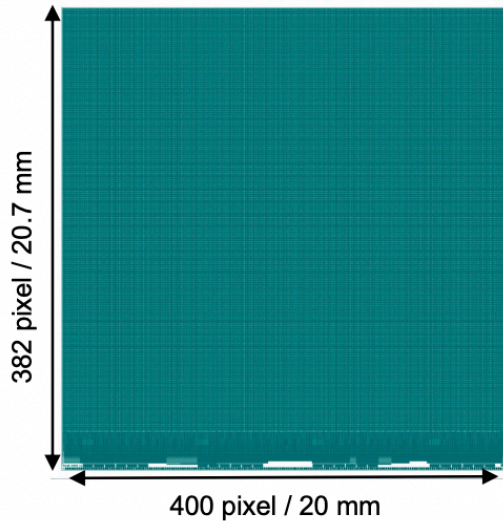
- Final chip consists of one analog differential FE of $2 \times 2 \text{ cm}^2$
- Low threshold $\sim 600 \text{ e}^-$
- Digital Readout with Time over Threshold (ToT)
- Design power 0.8 W/cm^2
- Radiation hard up to 1 GRad and single-event-upset hardened
- 4 data lines at 1.28 Gbps with data compression in output



[JINST 20 P03024](#)

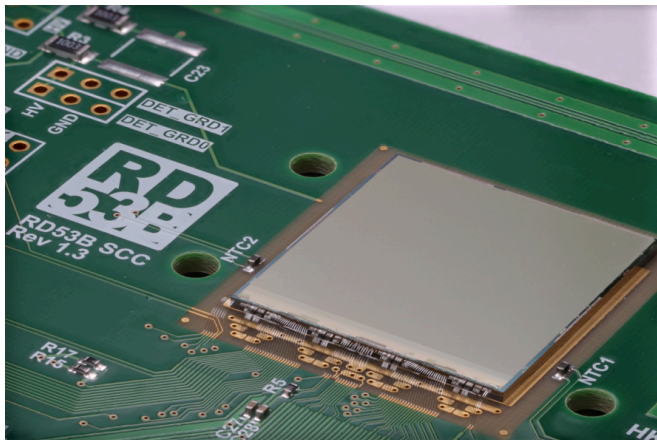
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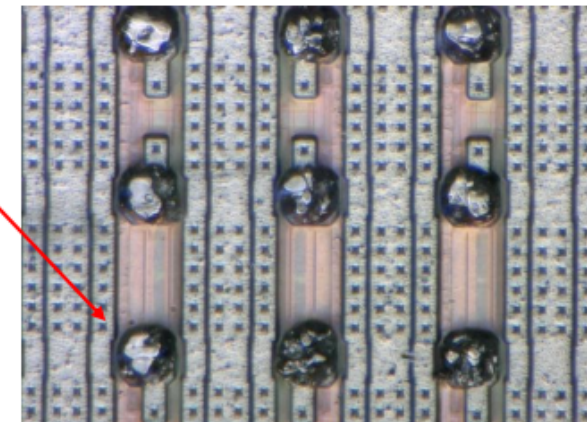


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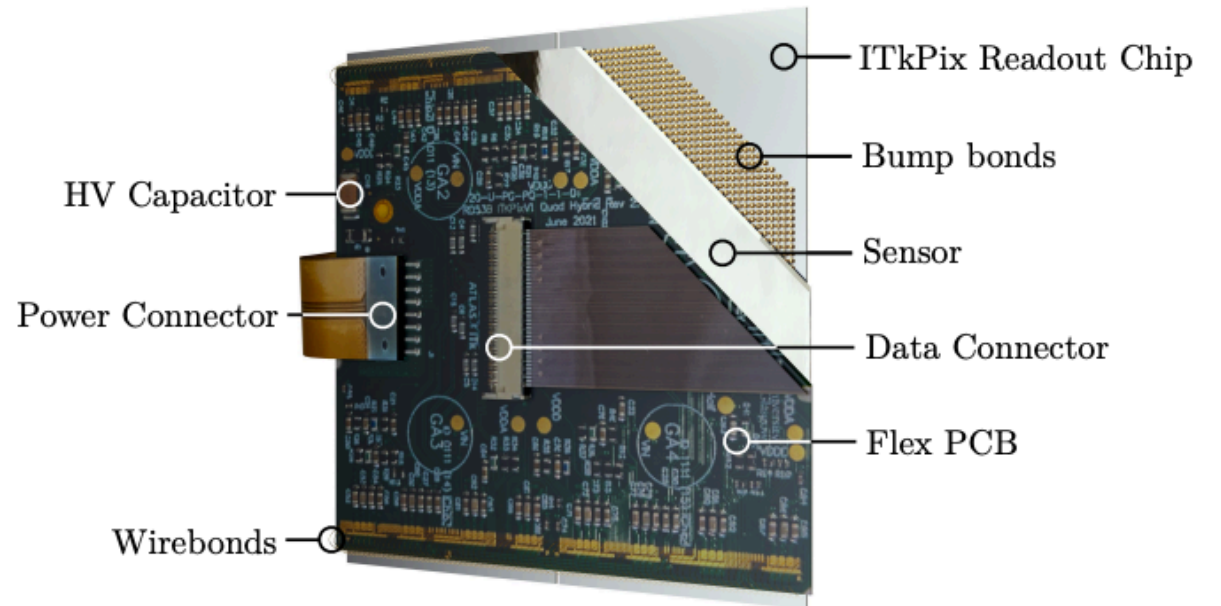
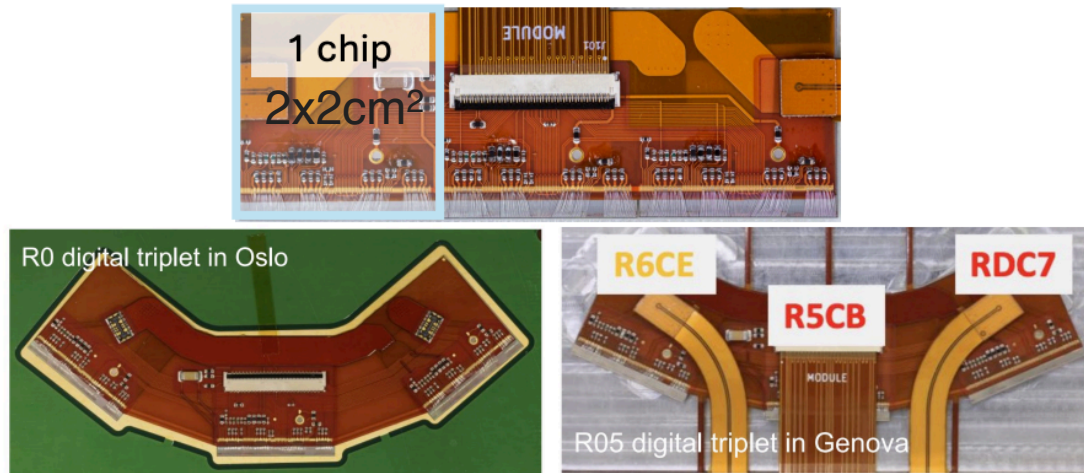
Bump deposition SnAg or In
Under Bump Metallization
Flip-chip
(IZM, HPK)

[More in Charles's talk](#)

Pixel Modules

[2412.04686](#)

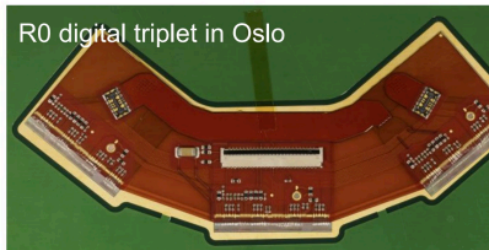
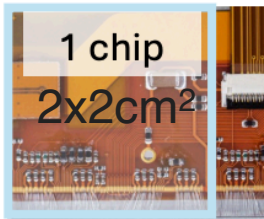
Module = Sensor + ASIC + flex circuit.



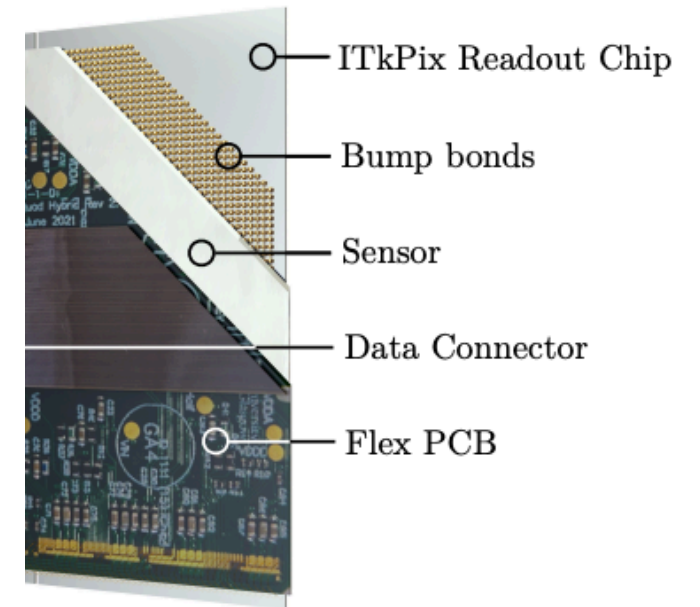
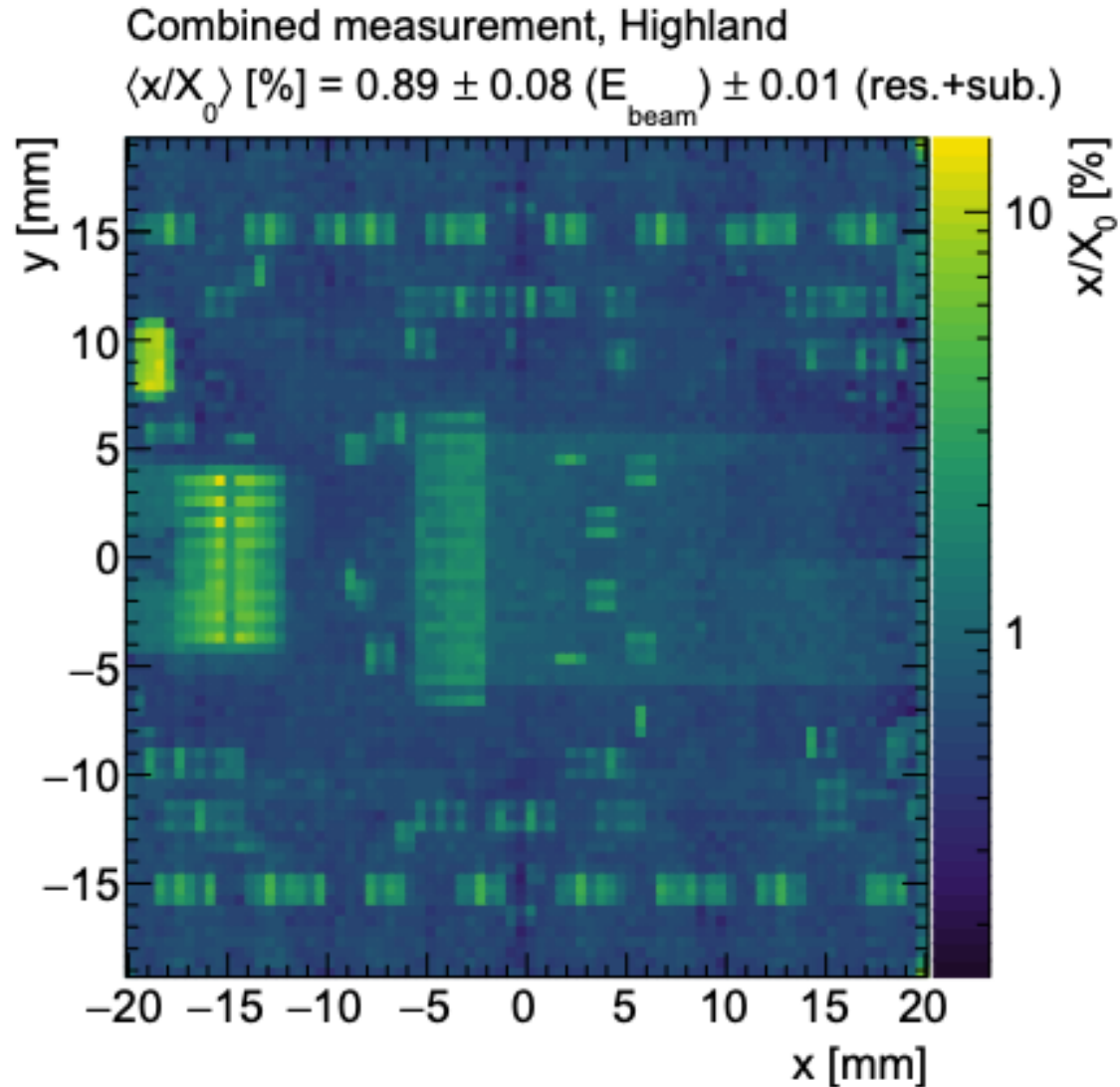
- Parylene protection deposition: reinforce bonds, avoid corrosion, prevent discharge between sensor and front-end.
- **Preproduction O(800) ITKPix-v.1 modules built**
 - Performance after radiation & thermal tests within specs for both 3D single and planar quad modules
- Production is starting NOW in 2025, ~9000 modules in 2 years in 20 assembly sites

Pixel Modules

Module = Sensor +



- Parylene prote between sensc
- **Preproduction**
 - Performance
 - planar qua
- Production is s



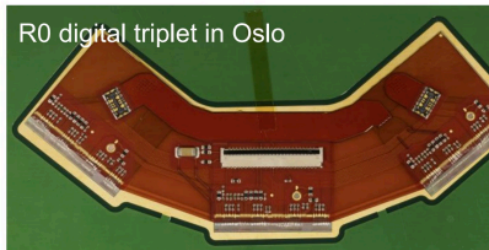
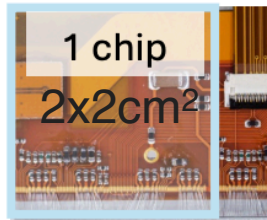
event discharge

1 3D single and

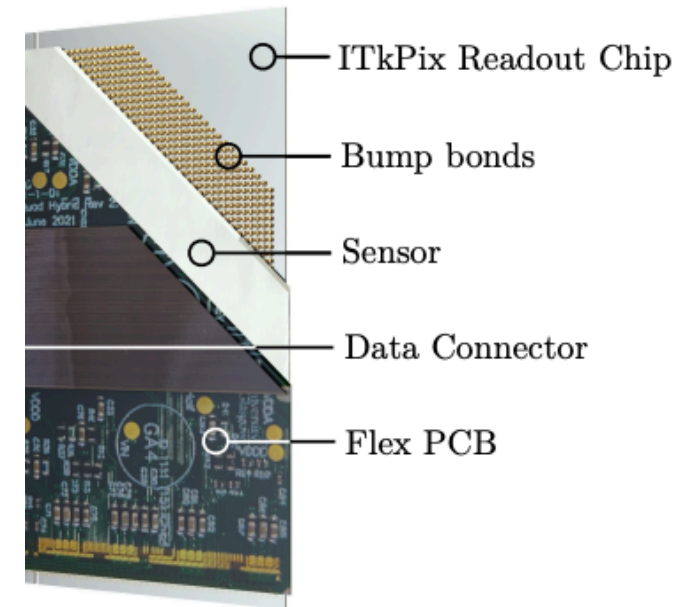
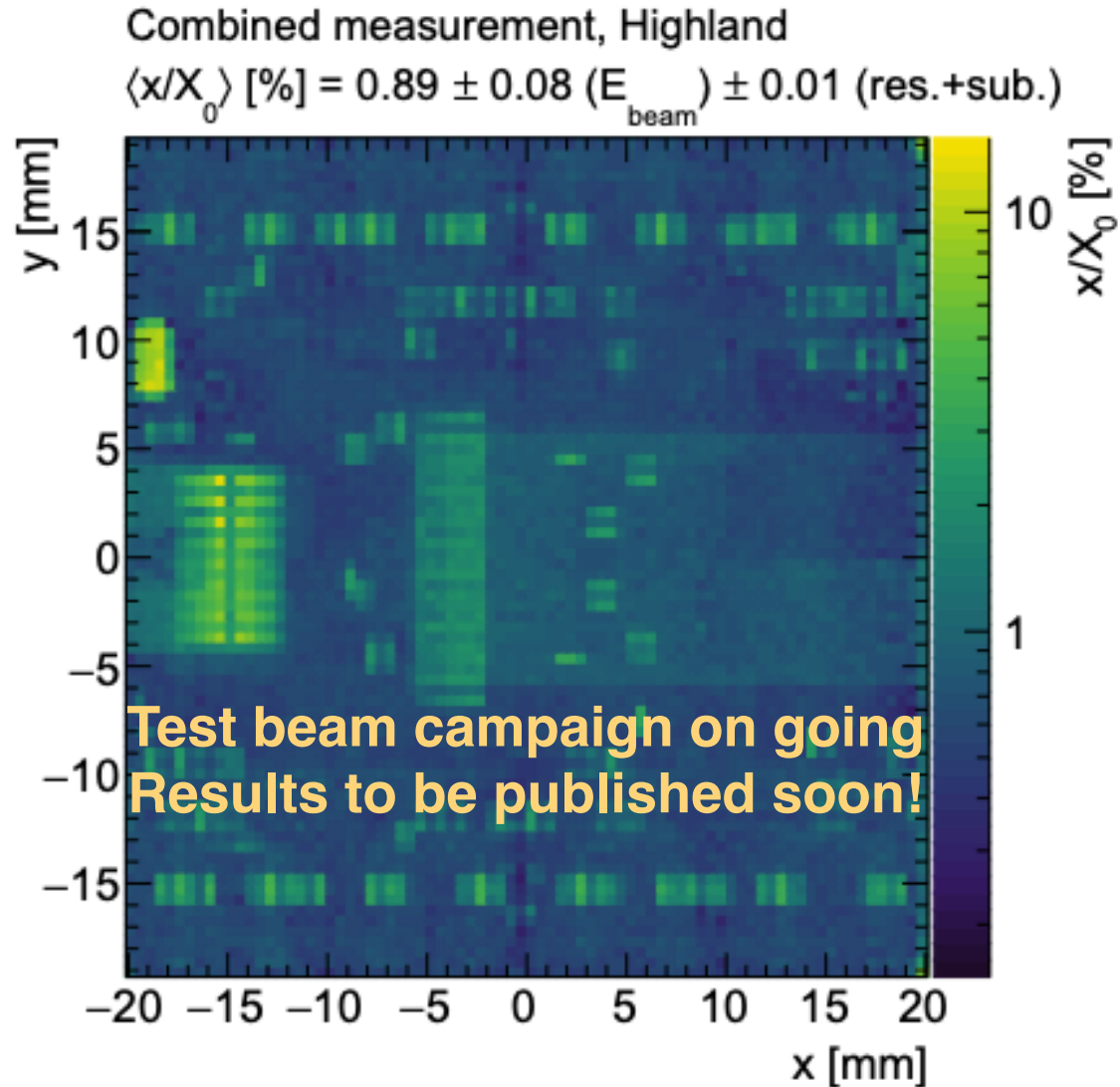
0 assembly sites

Pixel Modules

Module = Sensor +



- Parylene protection between sensors
- **Preproduction**
 - Performance
 - planar quadrupole
- Production is starting



event discharge

1 3D single and

2 assembly sites

From design to construction

Design validated through extensive prototyping and mockups

Operating conditions:

- Temperature: $-45\text{ }^{\circ}\text{C}$ to $+40\text{ }^{\circ}\text{C}$ ($-55\text{ }^{\circ}\text{C}$ to $+60\text{ }^{\circ}\text{C}$ failure margins)
- 10 years lifetime are \sim equivalent to 100 thermal cycles
- Radiation: **up to** 1 GRad (varies with the detector radius)

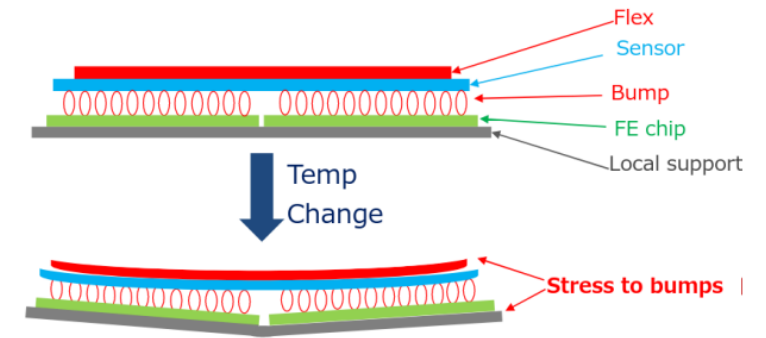
Mechanical & Interface Considerations

- Test parts of the assembly for CTE mismatch to prevent stress-induced failures
- Critical interfaces: **module bump bonds**, adhesives, electrical services
- Electrical services routed on local supports and half shells

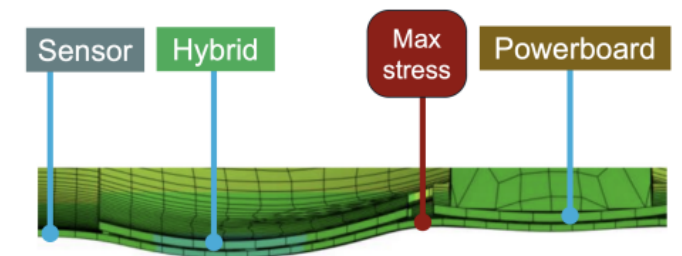
Readiness Approach

Design Validation (QA) to detects weaknesses in design

- Prototypes qualified to limits; some stressed to failure to define margins
- Production Readiness (QC) to identify defects in production



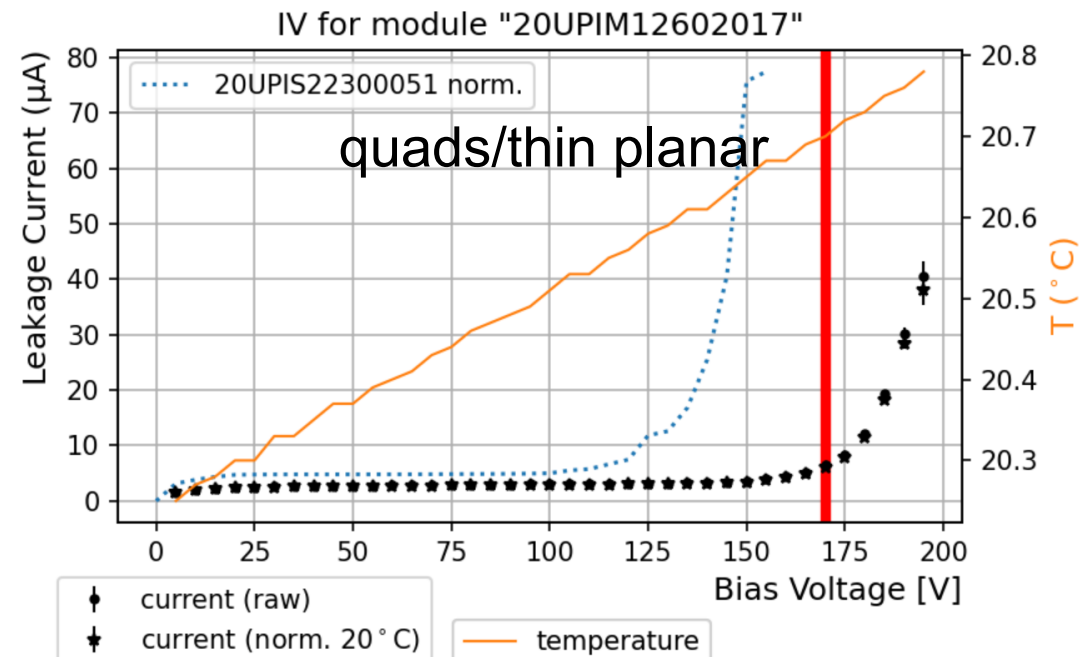
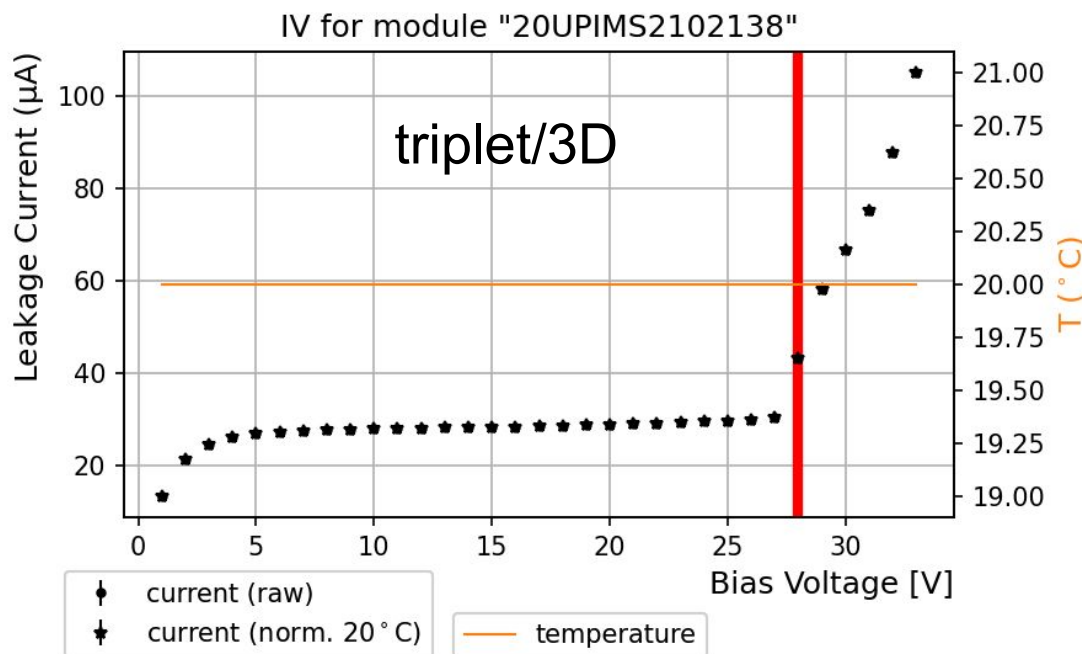
[ATL-ITK-PROC-2024-018](#)



[ATL-ITK-PROC-2024-043](#)

Module testing

Several QC steps at 20C and -10C to probe modules viability for loading



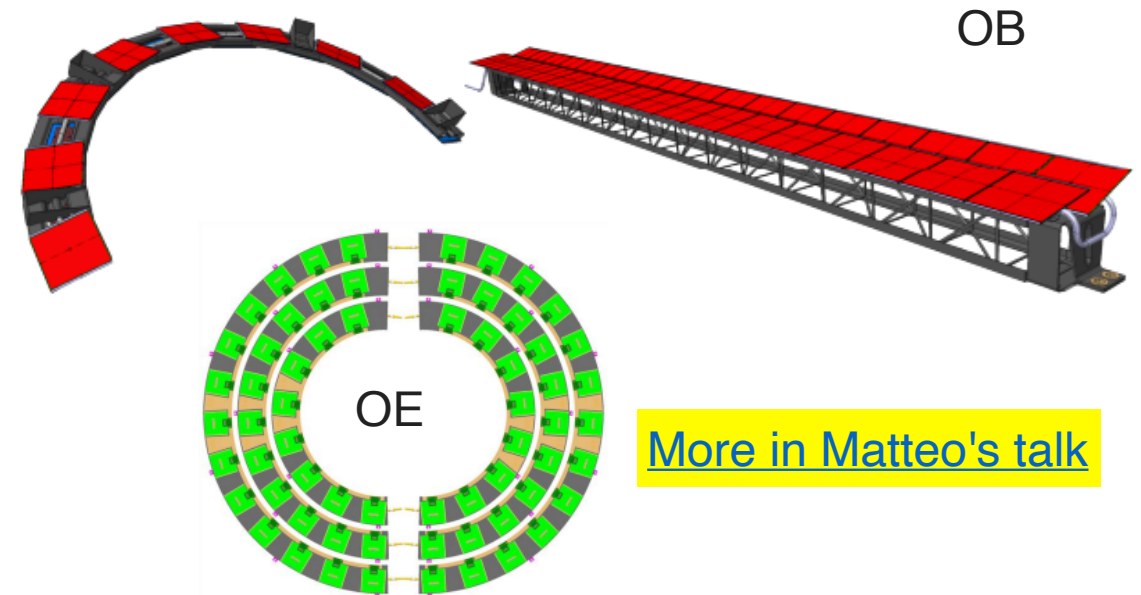
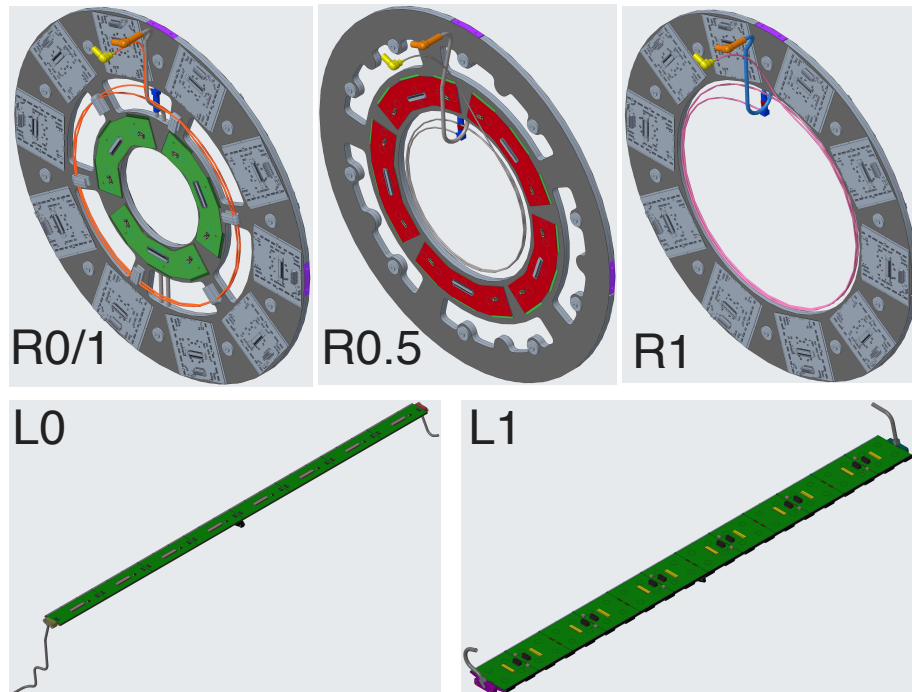
Module QC include: Visual inspection, sensor I–V scan, digital/analog/threshold/ToT/disconnected bump bond tests

Pixel Local Supports

Local support prototypes using carbon fibre and carbon foam to minimize mass and maximize thermal performance

Different geometries optimized for the various layers and region of the pixel detectors:

- **Inner system** : two layers of staves and double-sided rings in the endcaps
- **Outer Barrel** : three layers of longeron and inclined rings
- **Outer Endcap** : three layers of endcap rings



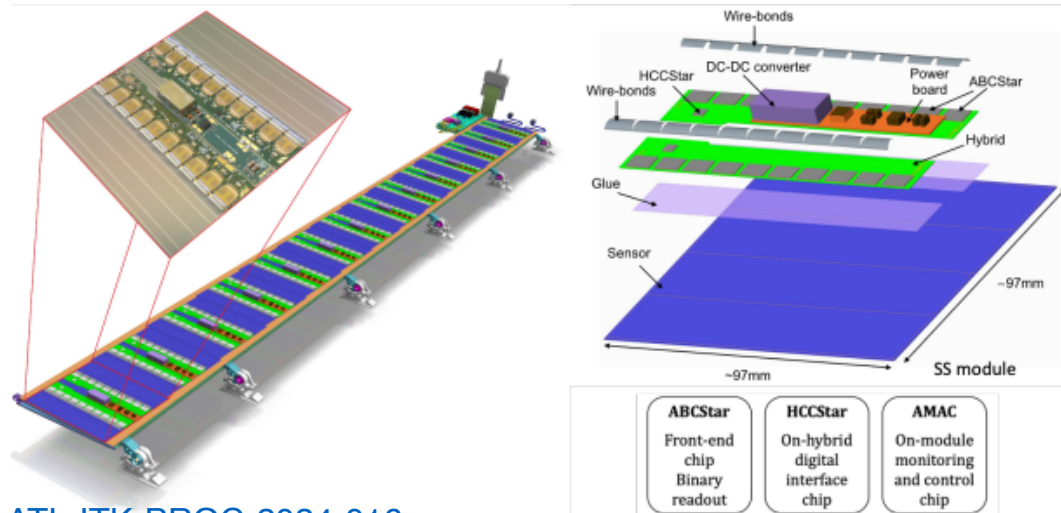
[More in Matteo's talk](#)

Titanium Cooling Tubes embedded into the CF foam

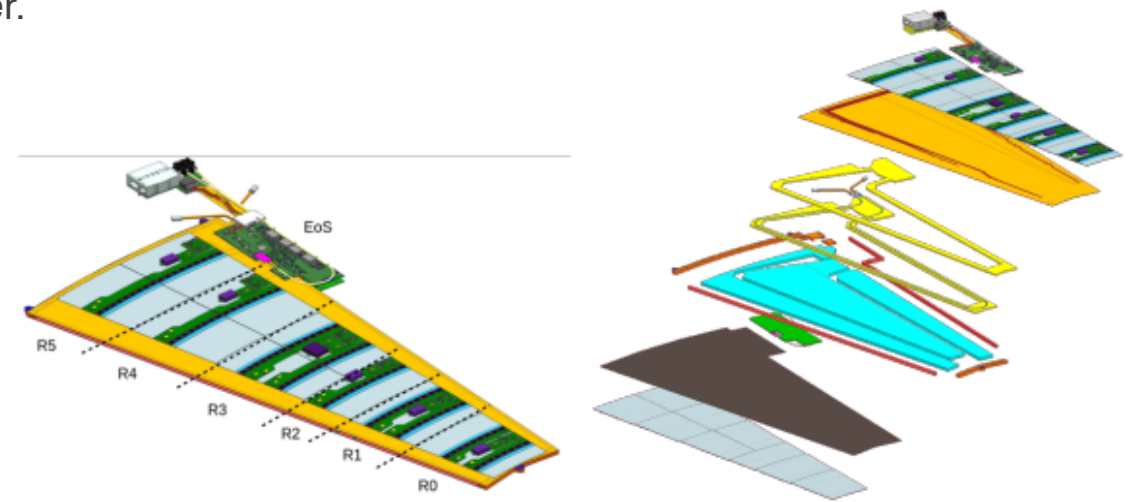
Strip Assembly

Module = sensor + ASIC + power board

- AC-coupled, **n-in-p** silicon sensors, more radiation resistant than p-in-n up to 10^{15} n_{eq}/cm^2
- $75.5\mu m$ pitch, $320\mu m$ thick and $>300V$ depletion voltage
- Barrel modules:
 - Two $\sim 9.7\text{ cm} \times 9.7\text{ cm}$ sensor geometries: short strip (SS) for the inner and long strip (SS) for the outer layers
 - 14 modules per side per stave
- Endcap modules:
 - 6 sensor geometries depending on radial distance from center.



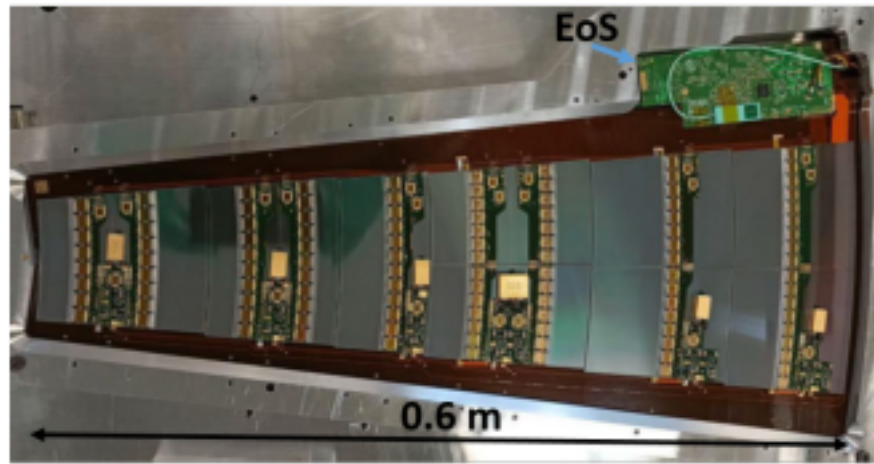
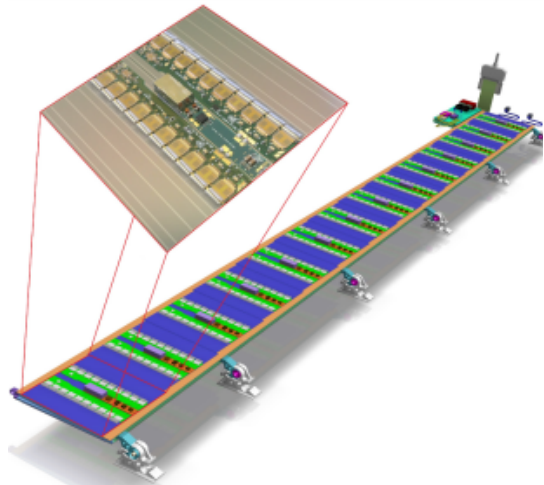
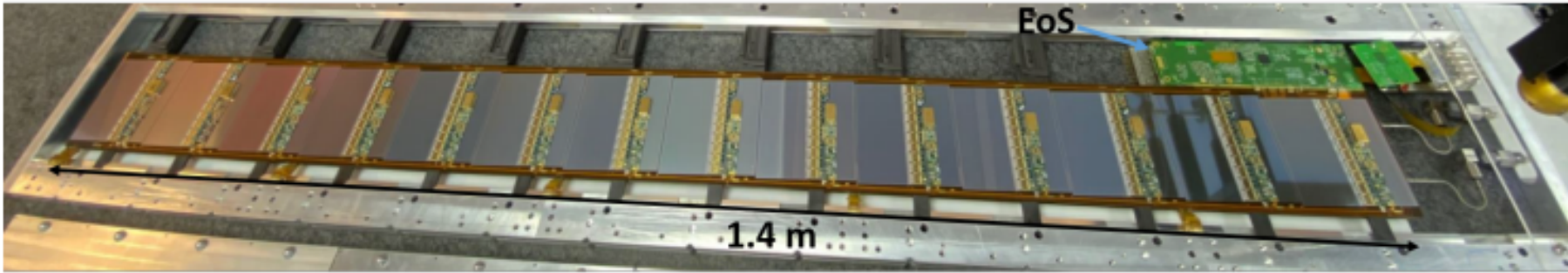
[ATL-ITK-PROC-2024-016](#)



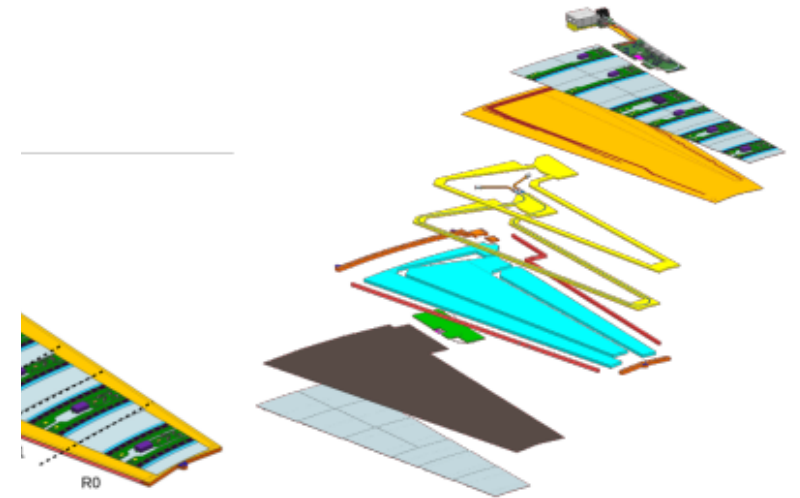
Strip Assembly

Module :

- AC-coupled
- $75.5\mu\text{m}$ pitch
- Barrel modules
 - Two
 - 14 n
- Endcap modules:
 - 6 sensor geometries dependent



Binary readout interface chip and control chip



[ATL-ITK-PROC-2024-016](#)

About 90% sensors received, 85% tested are viable for loading

WIREBONDS

Readout ASIC
ITkPix

adapted from
Simon Koch



SENSOR

BUMP BONDS

FLEX PCB

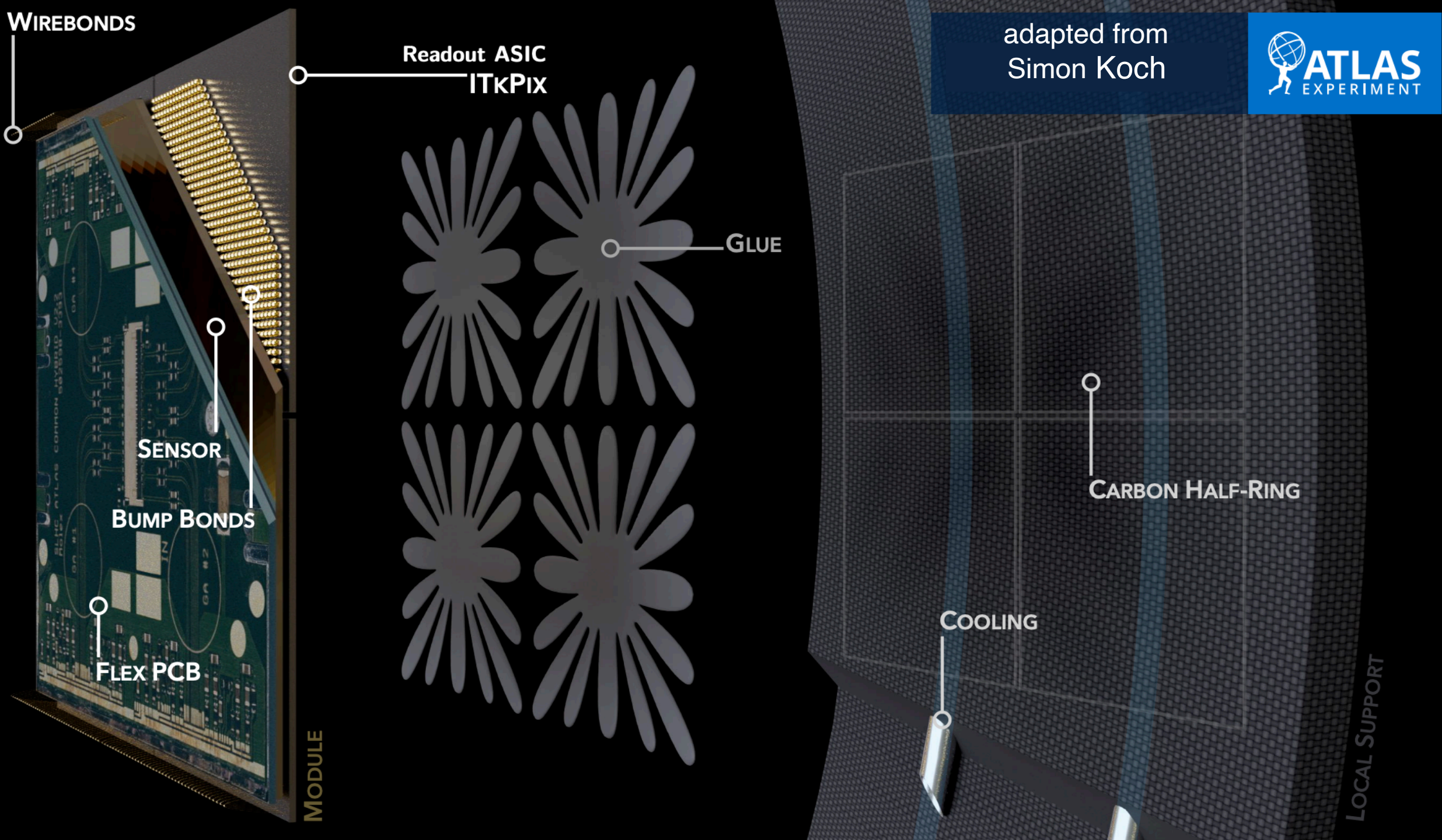
MODULE

GLUE

CARBON HALF-RING

COOLING

LOCAL SUPPORT



WIREBONDS

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ITkPix

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Simon Koch



SENSOR

BUMP BONDS

FLEX PCB

MODULE

Module

$100^{+100}_{-50}\mu\text{m}$

Carbon Fiber

GLUE

CARBON HALF-RING

COOLING

LOCAL SUPPORT

WIREBONDS

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GLUE

SENSOR

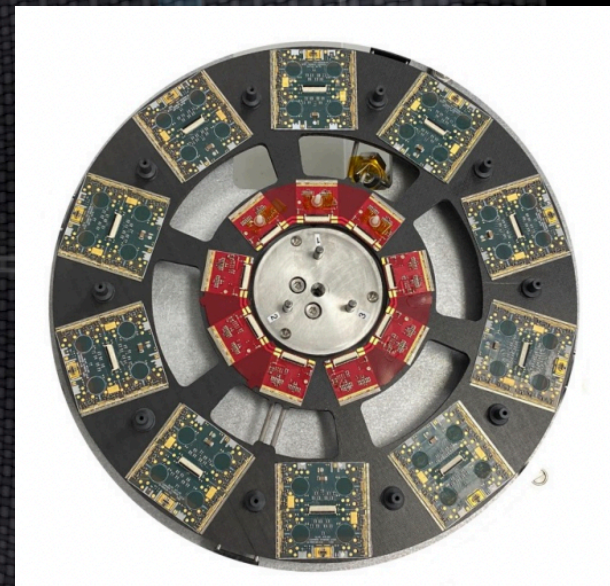
BUMP BONDS

FLEX PCB

Module

100^{+100}_{-50} μm

Carbon Fiber



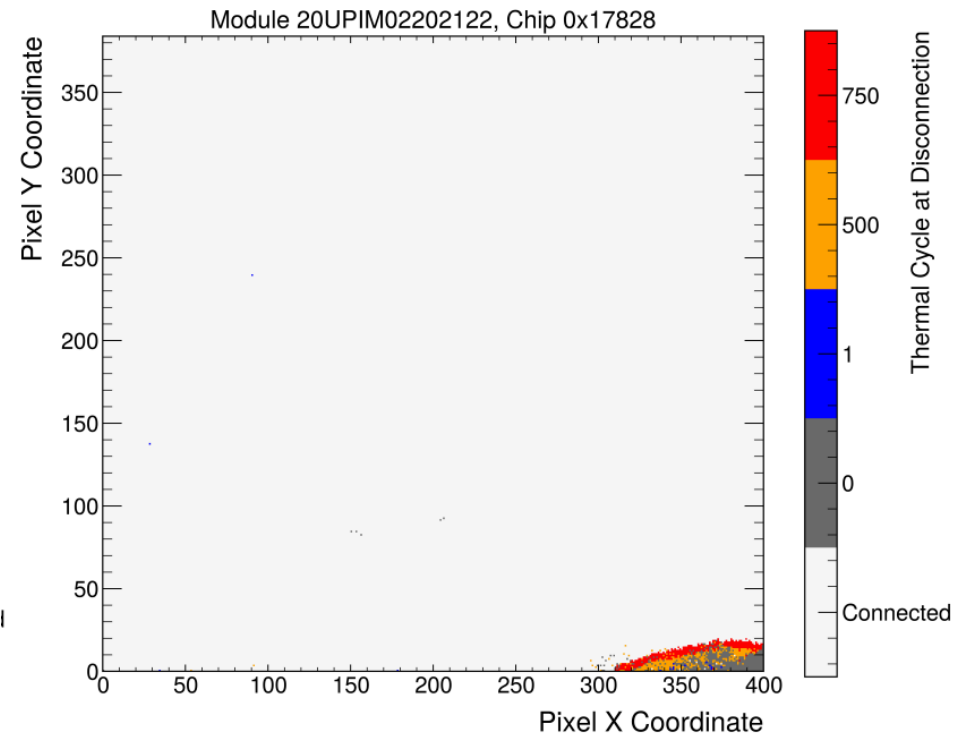
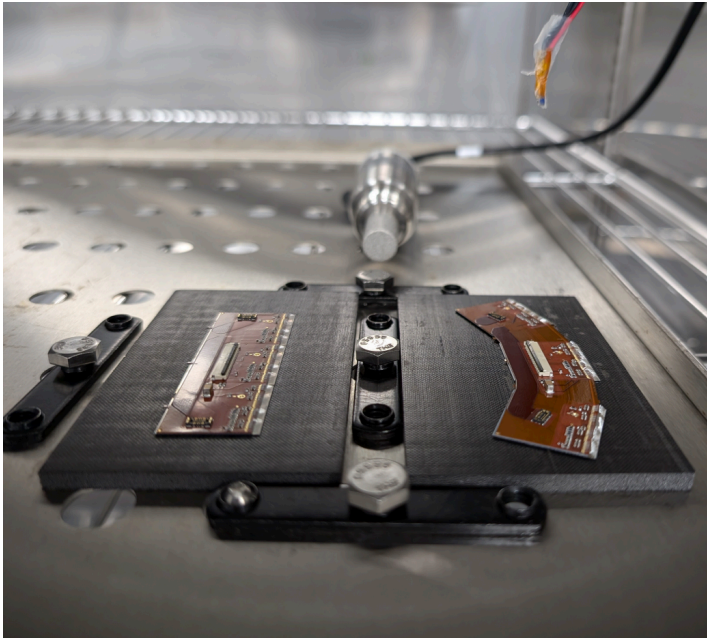
COOLING

MODULE

LOCAL SUPPORT

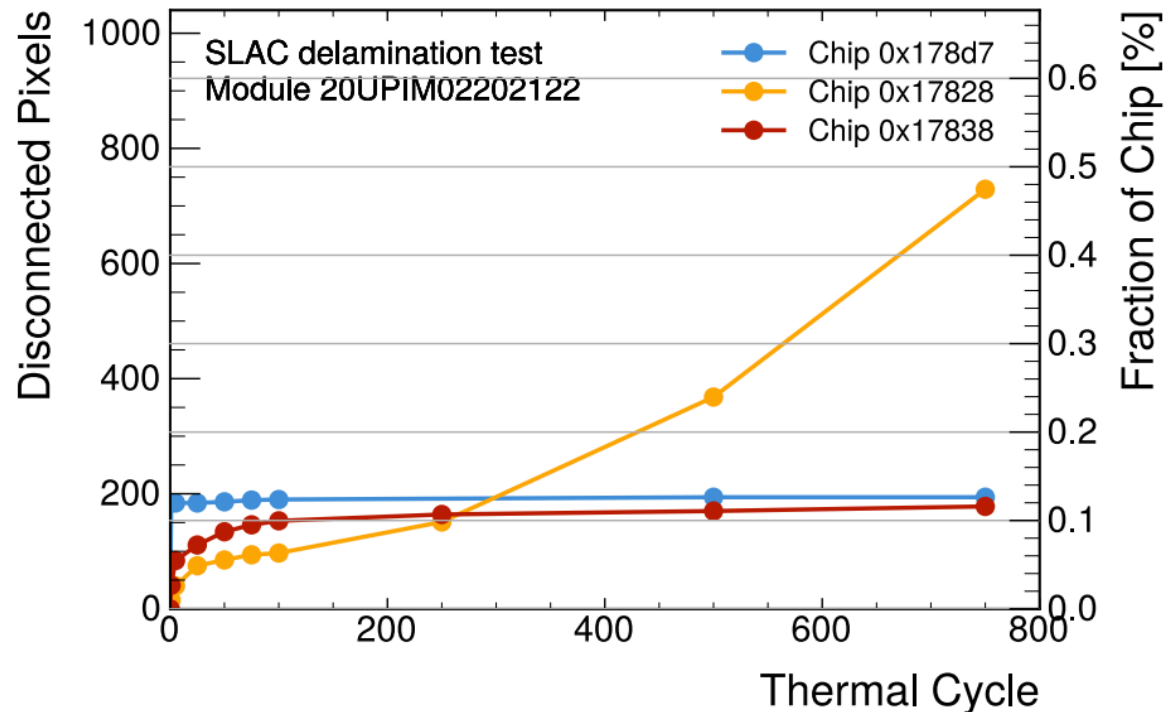
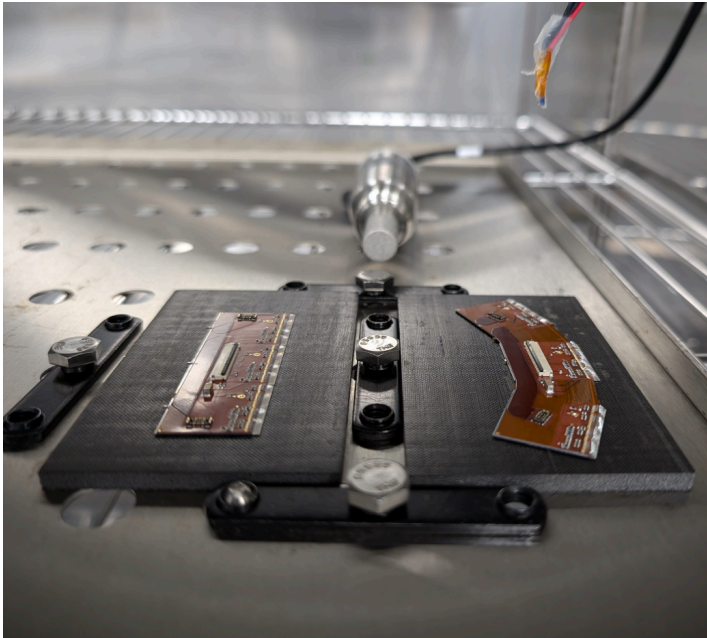
Pixel - The Glue(s)

- Both IS and Outer Endcap will use SE4445
 - a two part silicone based encapsulant gel
 - qualified up to 15 MGy with dedicated radiation testing campaigns (*pre-print in preparation*)
- The Outer Barrel uses Stycast (more rigid)
- Delamination studies have been performed to validate the glue doesn't add stress on the bump bonds
 - Modules glued onto a CF sample and thermal cycled between -55+60C for ~750 cycles



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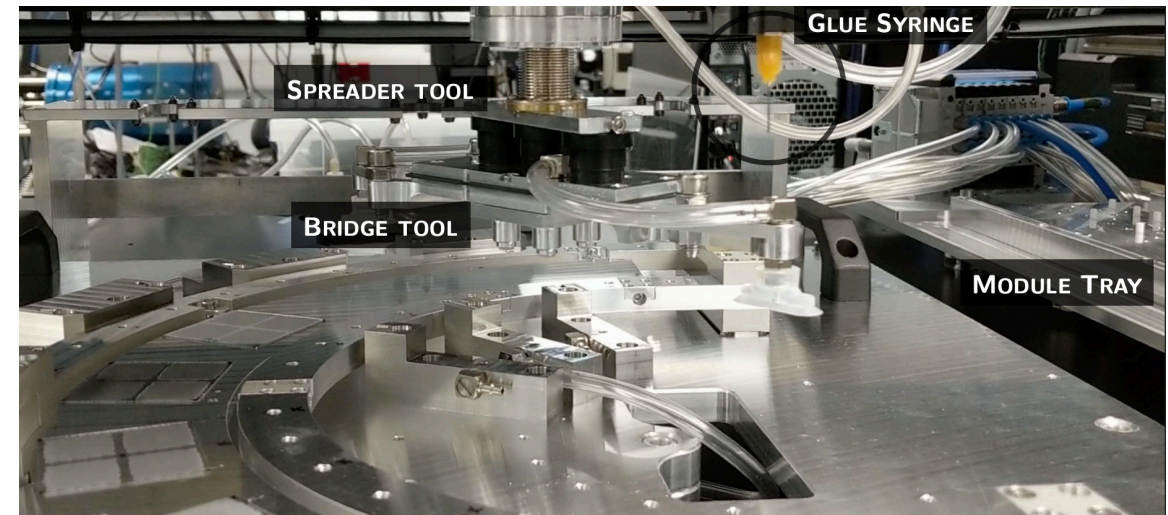
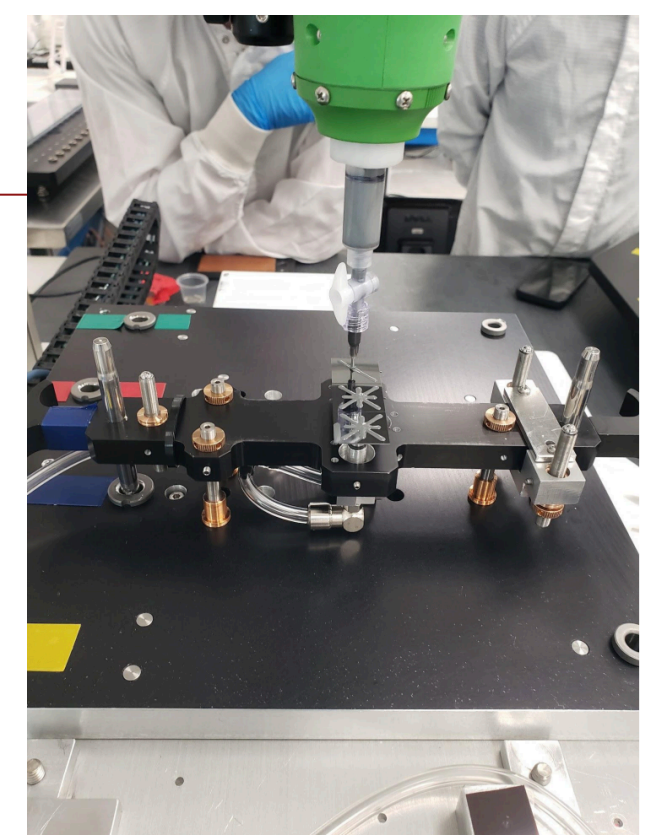
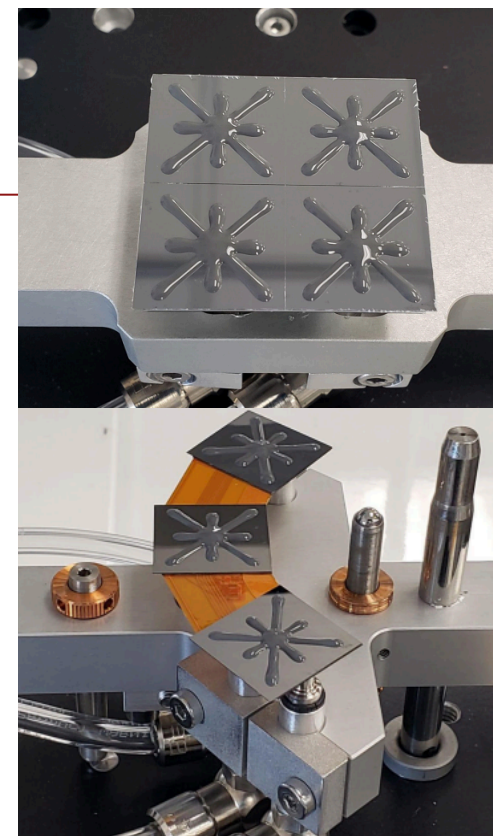
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Pixel - Loading process

Gluing modules into the local supports

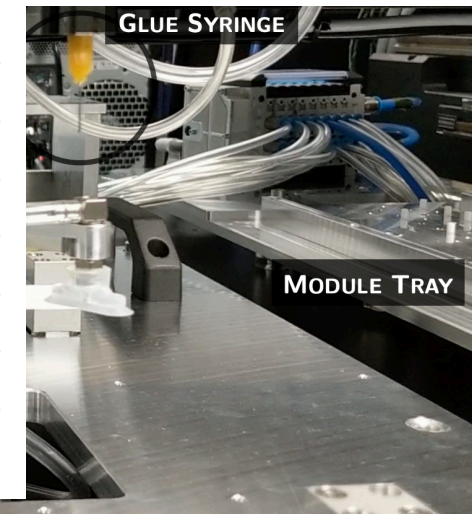
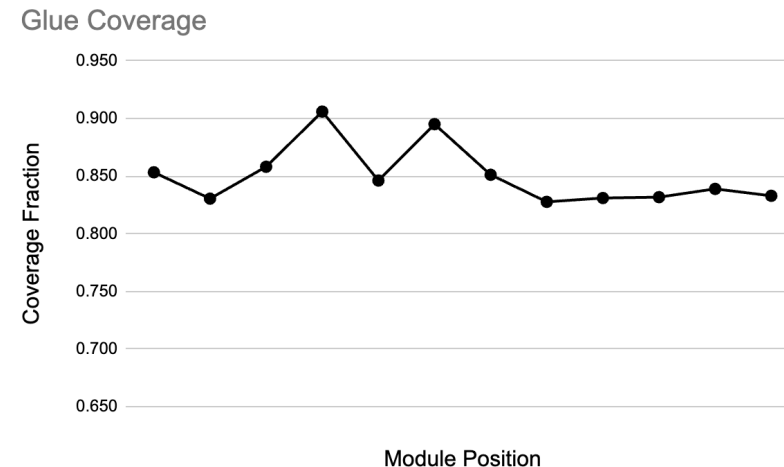
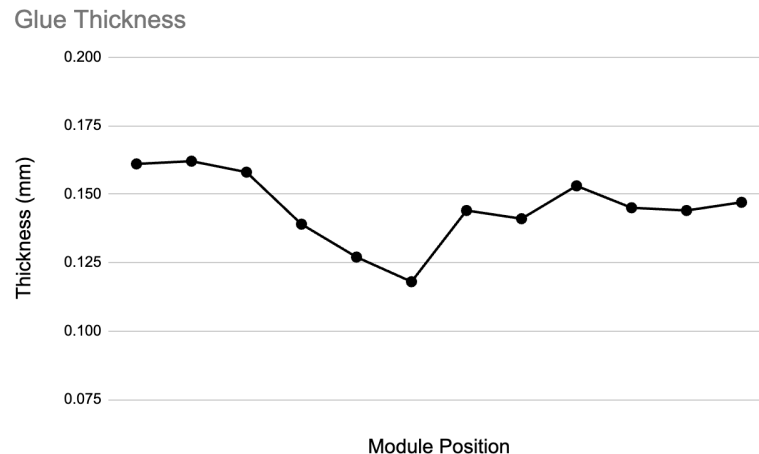
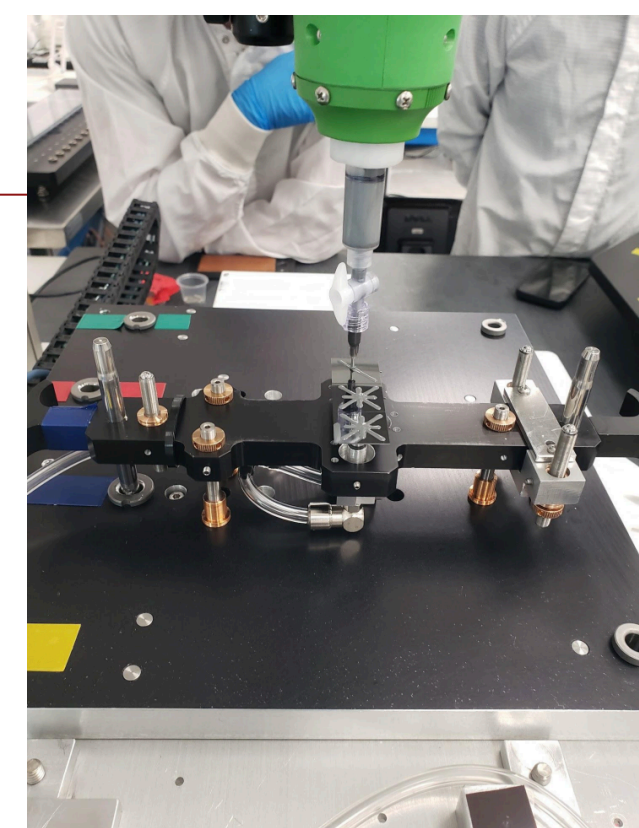
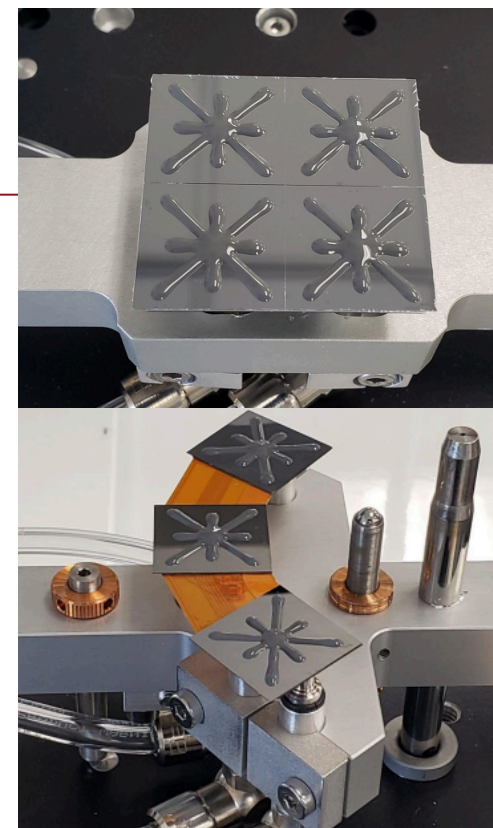
- Star pattern chosen to achieve good coverage without leaving trapped air
- Thickness & coverage of the adhesive optimized to ensure good thermal conductivity
 - $100^{+100}_{-50}\mu\text{m}$ thickness
 - 70-90% coverage
- Using 105 mg per deposition with a volumetric dispenser
- Primary bond line controlled by $106\ \mu\text{m}$ beads (1% by mass in glue)



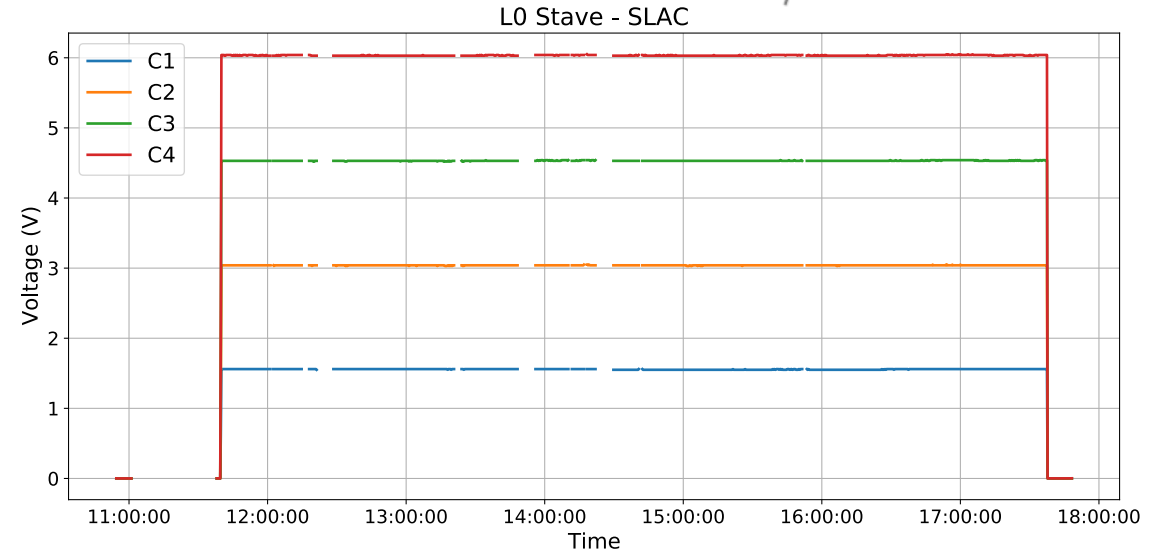
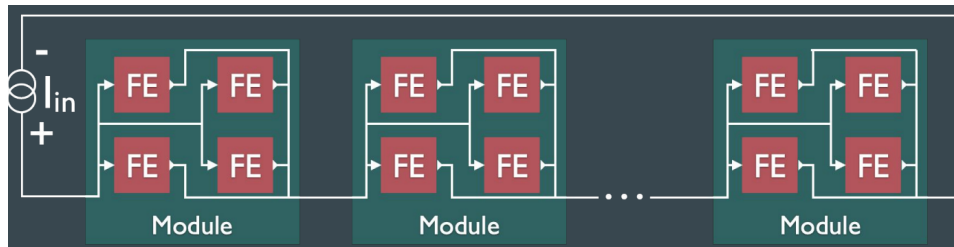
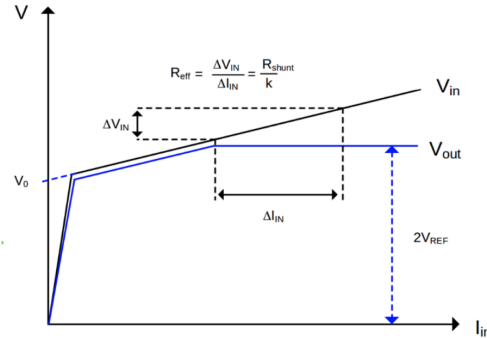
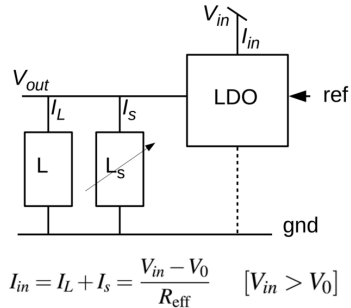
Pixel - Loading process

Gluing modules into the local supports

- Star pattern chosen to achieve good coverage without leaving trapped air
- Thickness & coverage of the adhesive optimized to ensure good thermal conductivity
 - 100+100₋₅₀μm thickness
 - 70-90% coverage
- Using 105 mg per deposition with a volumetric dispenser
- Primary bond line controlled by 106 μm beads (1% by mass in glue)



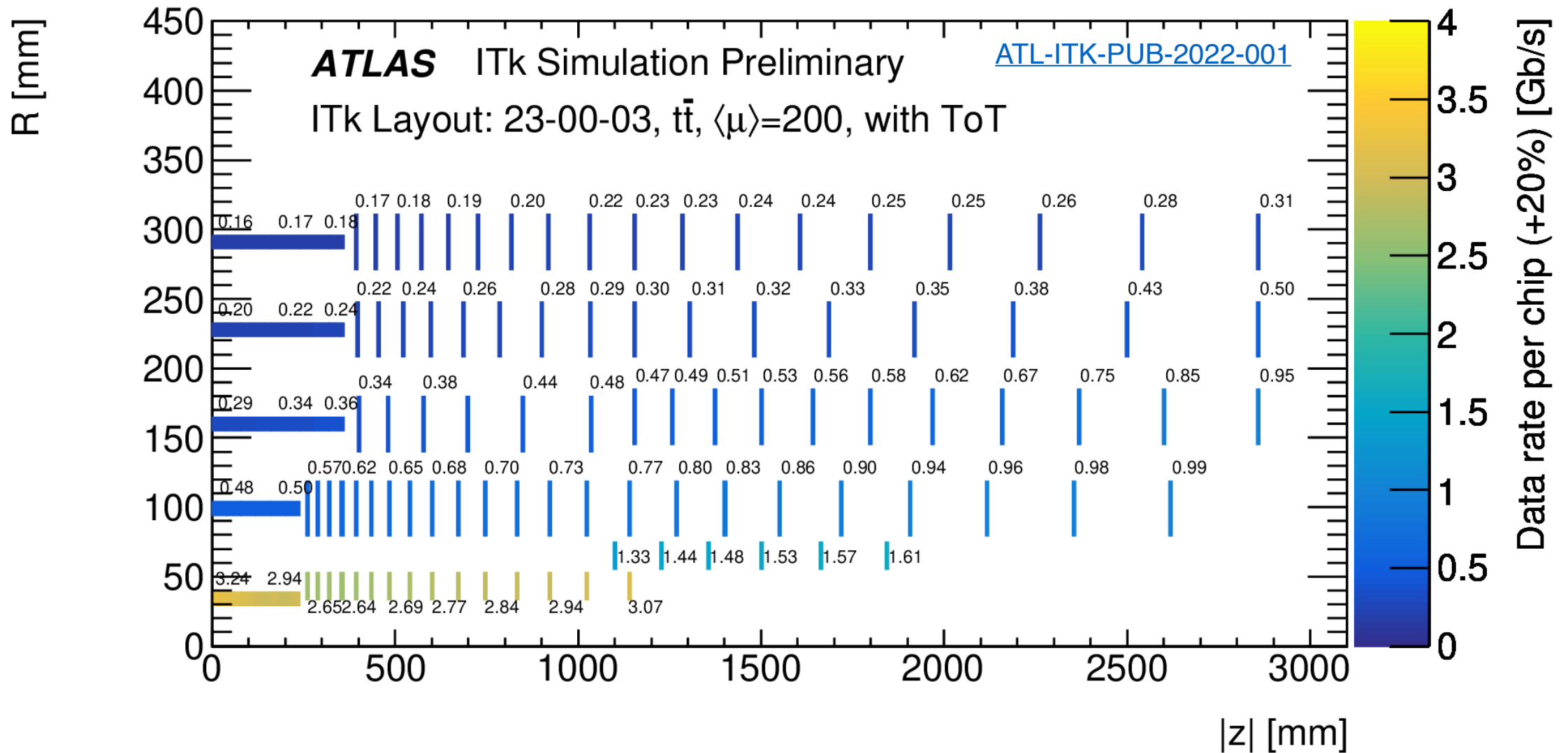
Pixel - Serial powering



- Modules are powered in series to reduce material budget: the number of supply lines is greatly reduced
- Each ITkPix chip has a radiation-hard Shunt Low Drop Output (SLDO) power regulator
 - It takes a constant input current and dynamically adjust their shunt current to maintain stable on-chip voltages.
 - Within a module, chips are powered in parallel to ensure local voltage regulation on each chip and improves chain robustness
- The ITk will use $O(1000)$ serial) powering chains, each driving up to 14 quad and 5 triplet modules.

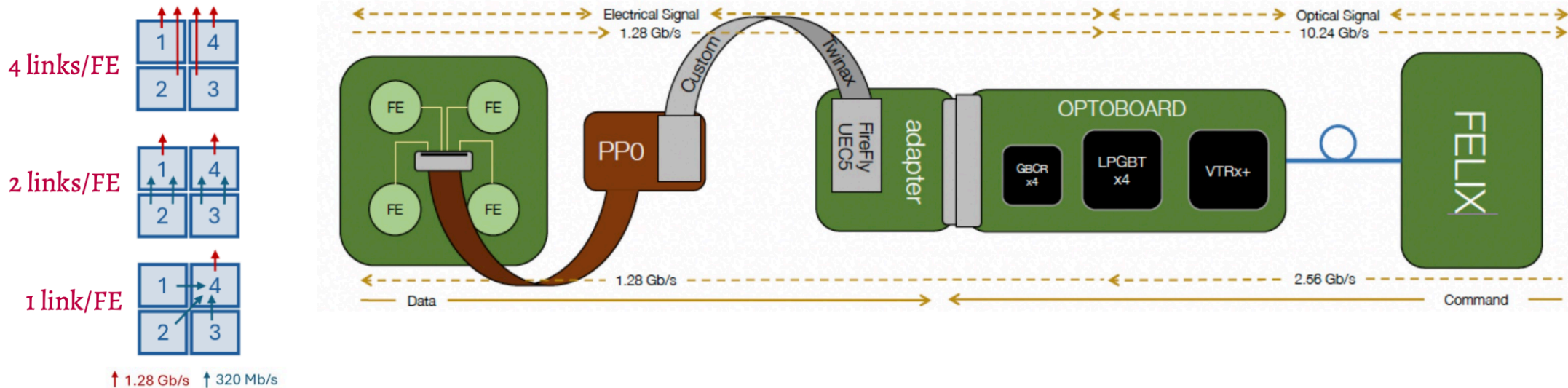
Pixel - Data transmission scheme

Link sharing on all layers to reduce material



Pixel - Data transmission scheme

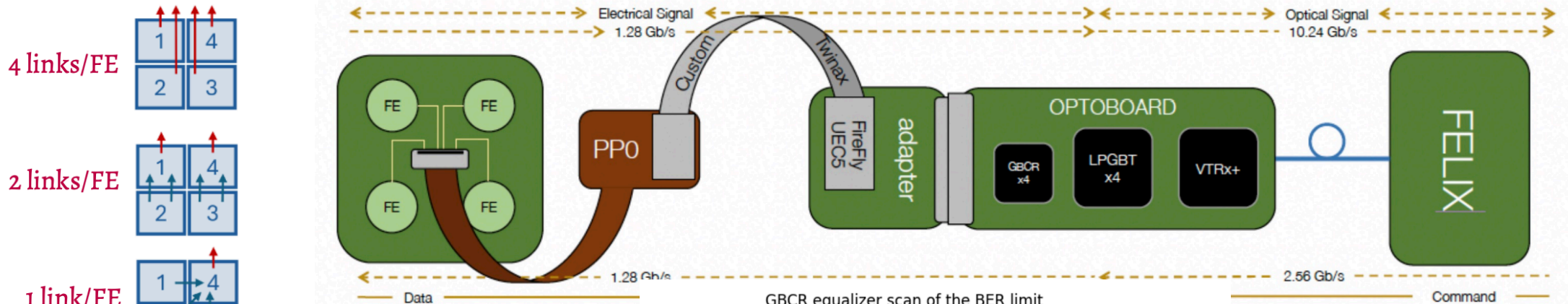
Link sharing on all layers to reduce material



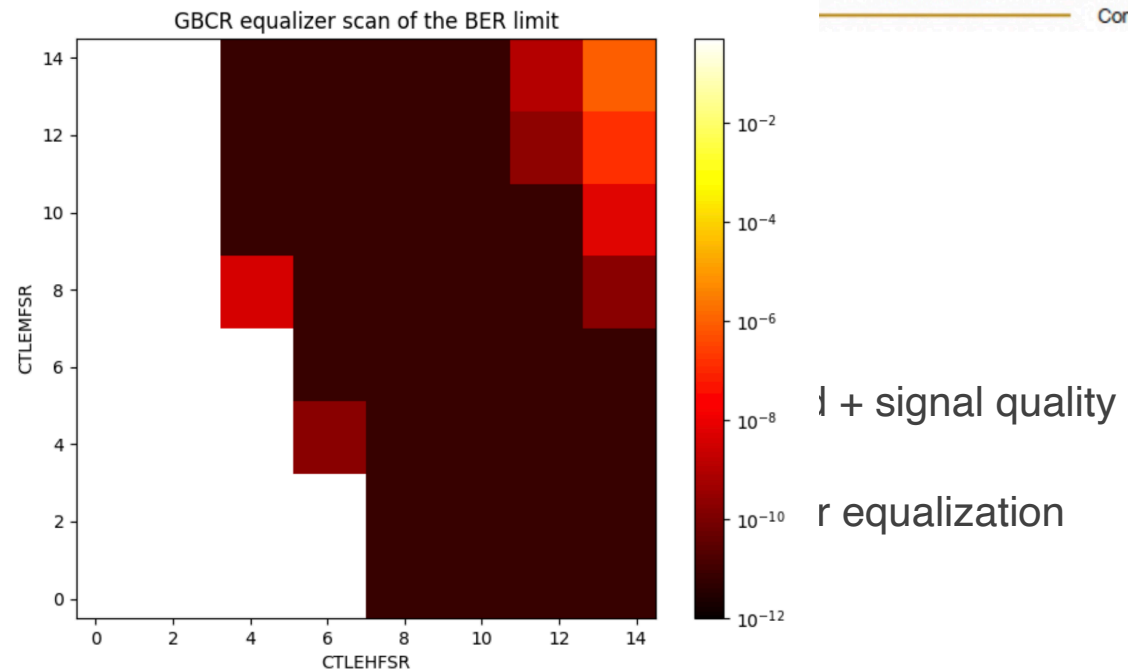
- Module: 1–4 FE links → consolidated into 1–3 × 1.28 Gb/s outputs.
- IpGBT/GBCR: up to 6 module inputs → multiplexed onto 1 × 10.24 Gb/s fiber.
- CMD: 1 × 2.56 Gb/s link per IpGBT/GBCR → fanout to 1–6 modules.
- **Transmission:** custom 34 AWG twinax (≤ 6 m) with polyethylene dielectric for rad-hard + signal quality < 20 dB loss @ 640 MHz (FE → GBCR).
- Aggregation + electro-optical conversion: IpGBTx + VTRx+, with recovery at GBCR for equalization

Pixel - Data transmission scheme

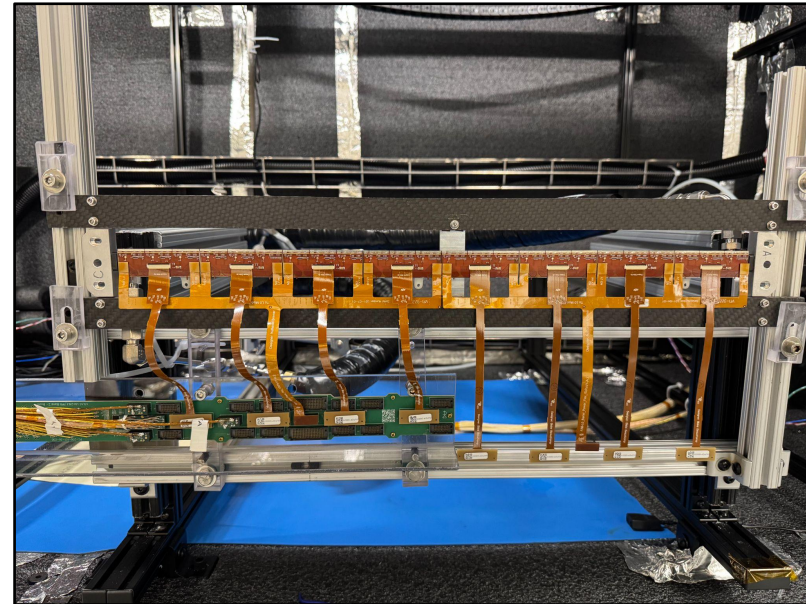
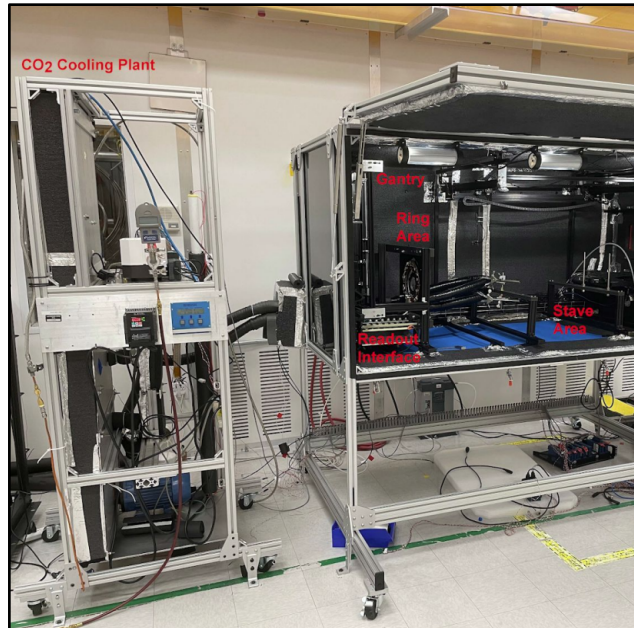
Link sharing on all layers to reduce material



- Module: 1–4 FE links \rightarrow consolidated into
- IpGBT/GBCR: up to 6 module inputs \rightarrow n
- CMD: 1 \times 2.56 Gb/s link per IpGBT/GBCF
- **Transmission:** custom 34 AWG twinax (\leq $<20 \text{ dB loss @ 640 MHz (FE} \rightarrow \text{Gf}$
- Aggregation + electro-optical conversion:

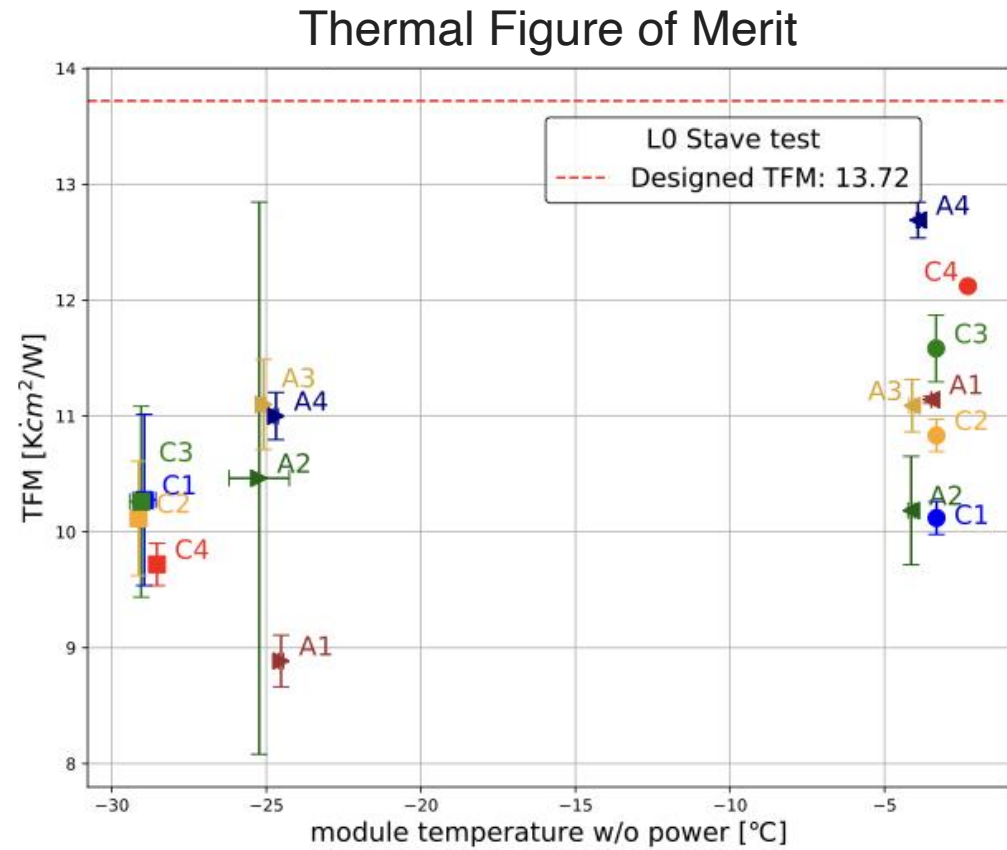
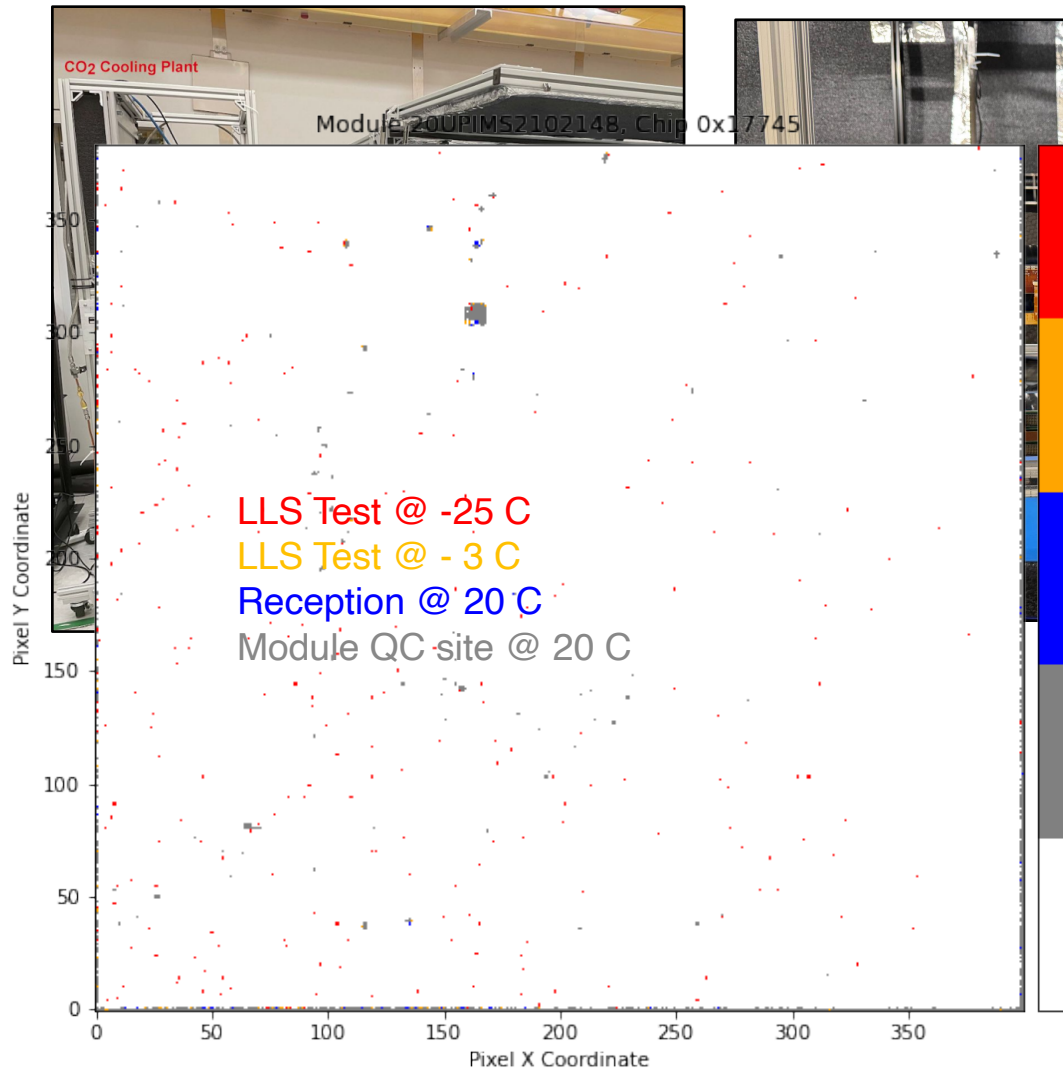


System Tests - full chain services demonstration



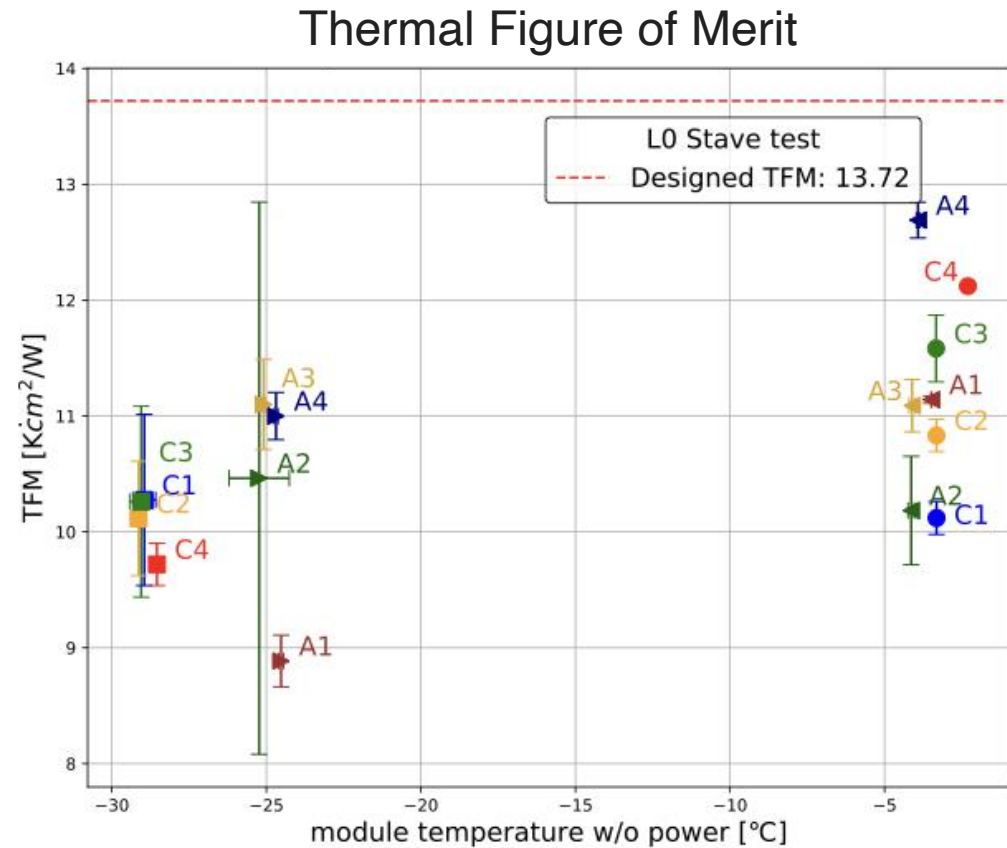
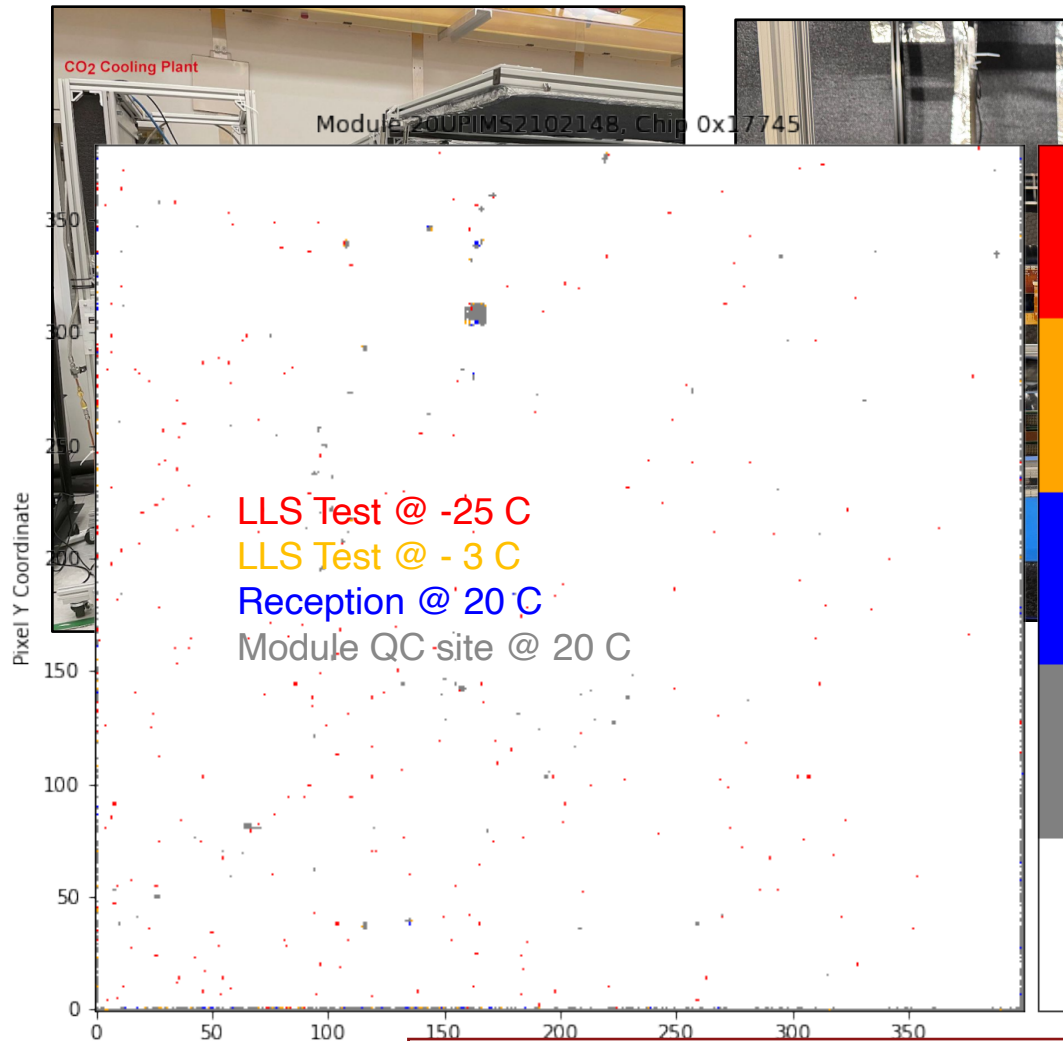
IS full validation of services chain
with pre-production parts

System Tests - full chain services demonstration



chain

System Tests - full chain services demonstration



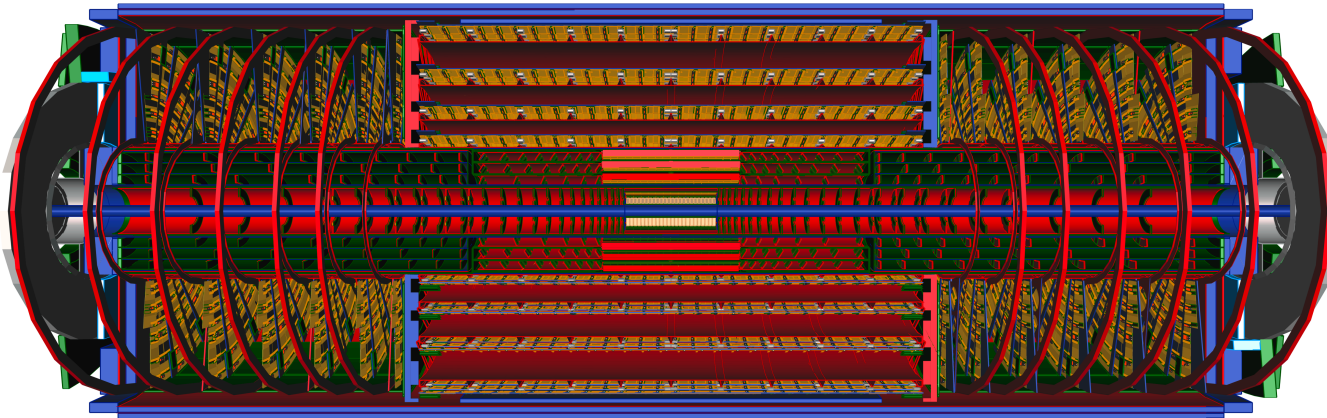
chain

Each sub-system has developed a large-scale system test setup to validate design of detector and services

Integration

Complex large assemblies for both barrel and endcaps

Mock-ups and prototypes to validate the integration sequence and data transmission

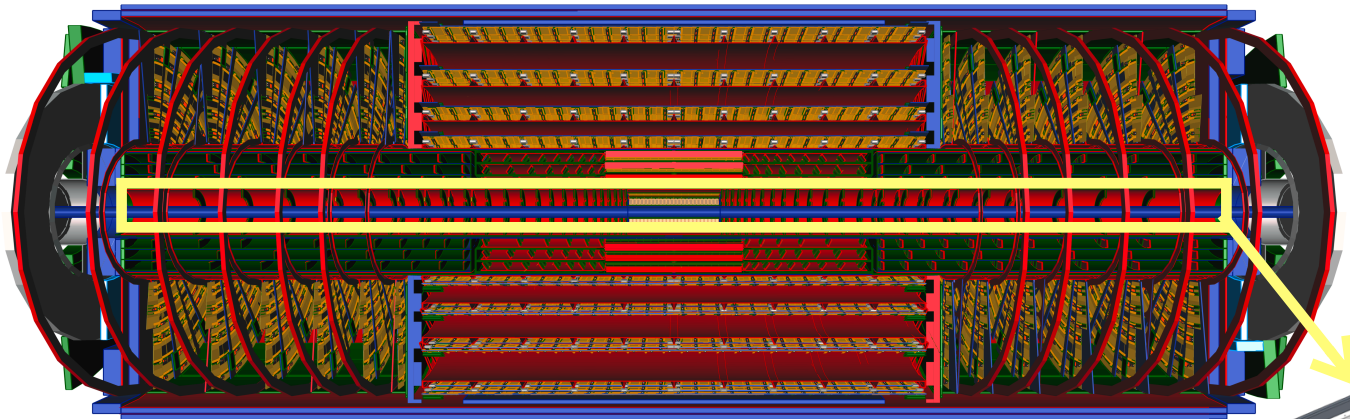


[ATL-PHYS-PUB-2021-024](#)

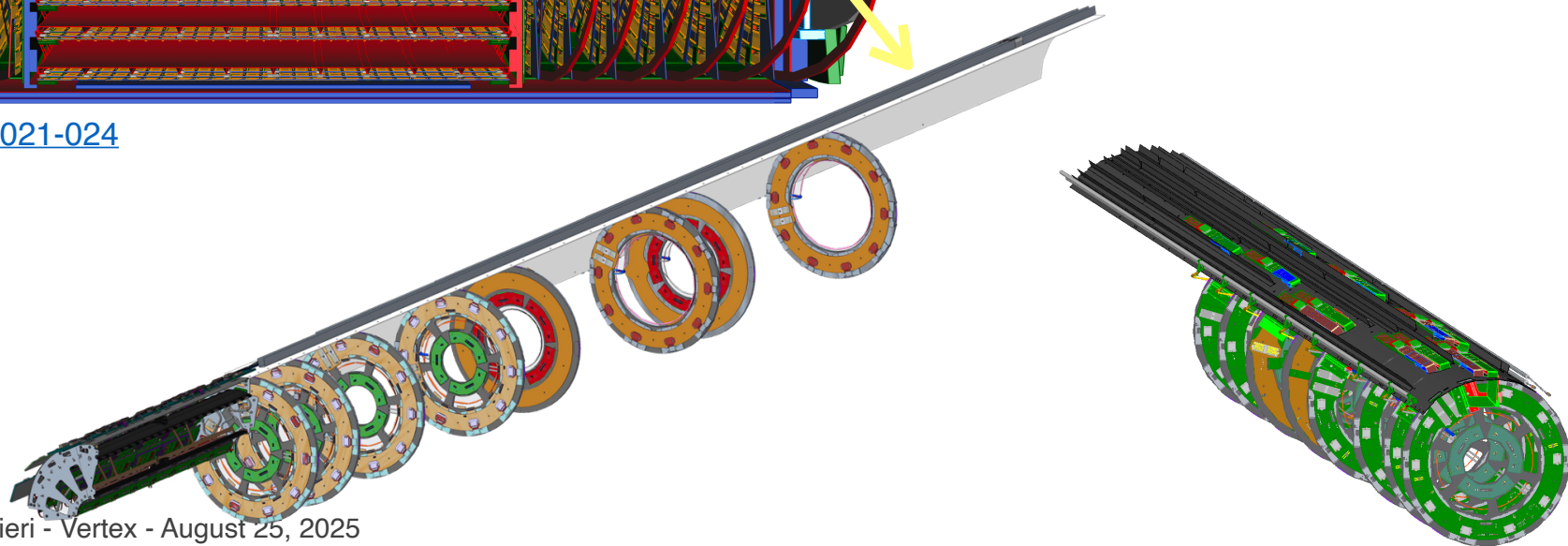
Integration

Complex large assemblies for both barrel and endcaps

Mock-ups and prototypes to validate the integration sequence and data transmission



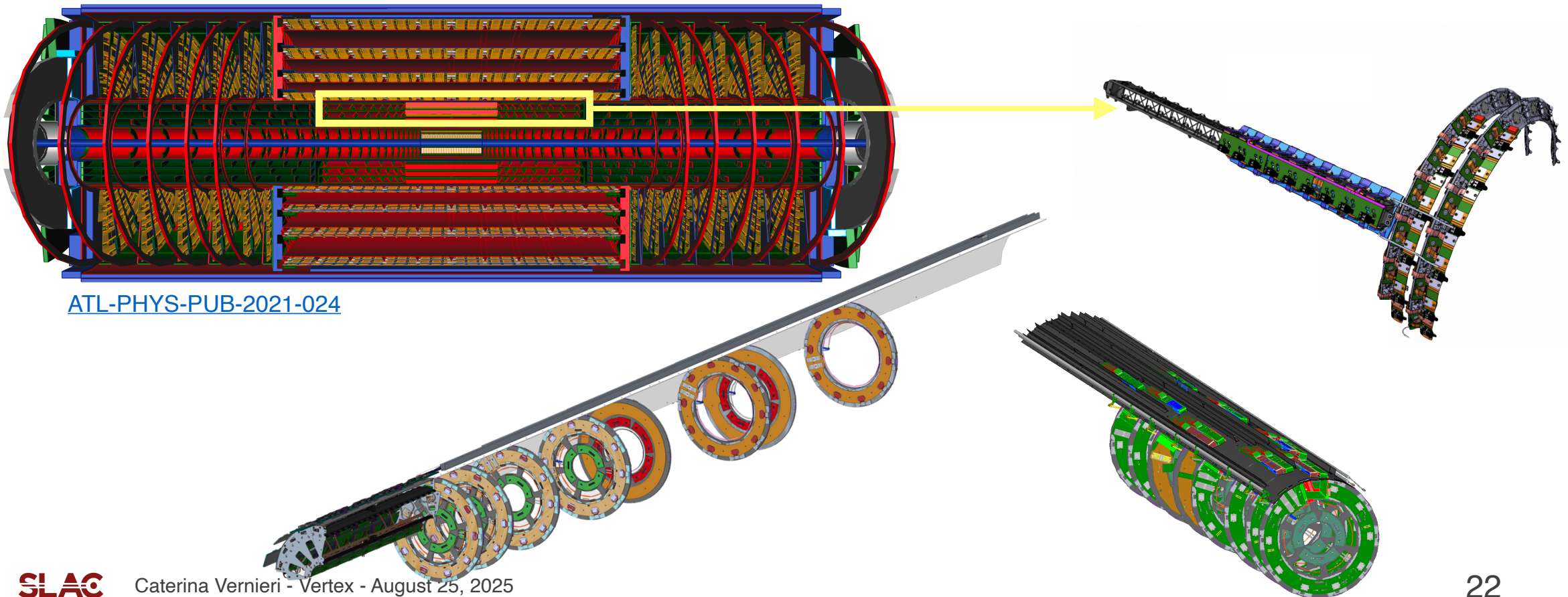
[ATL-PHYS-PUB-2021-024](#)



Integration

Complex large assemblies for both barrel and endcaps

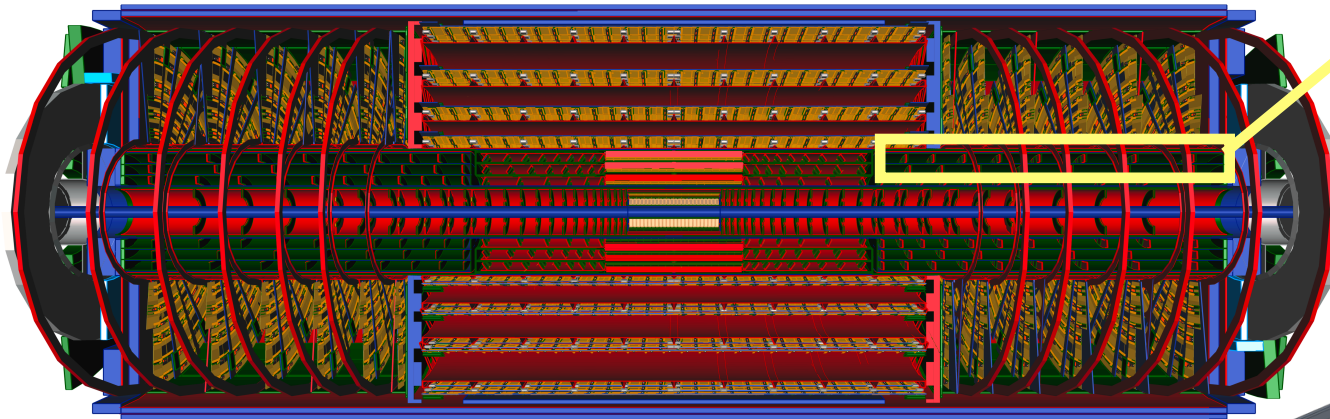
Mock-ups and prototypes to validate the integration sequence and data transmission



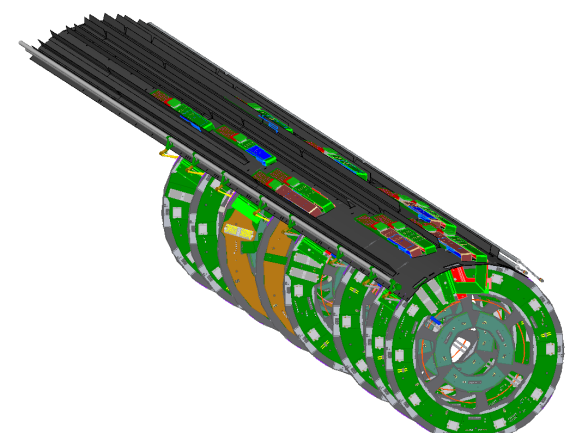
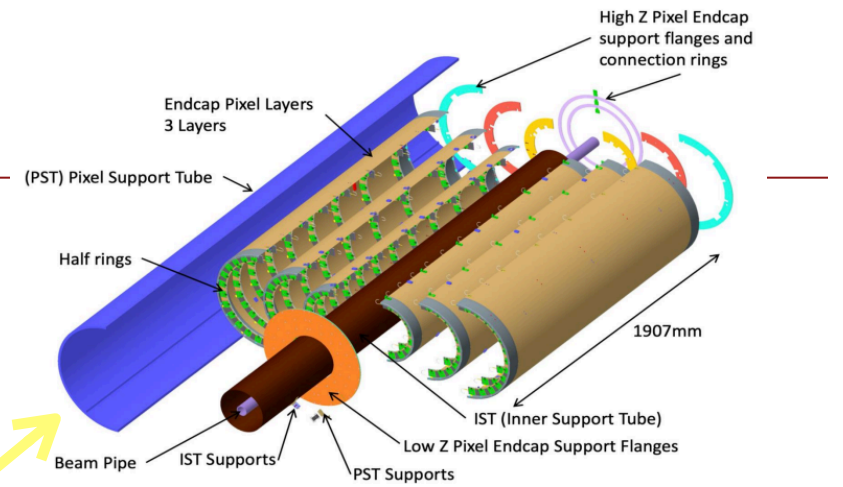
Integration

Complex large assemblies for both barrel and endcaps

Mock-ups and prototypes to validate the integration sequence and data transmission



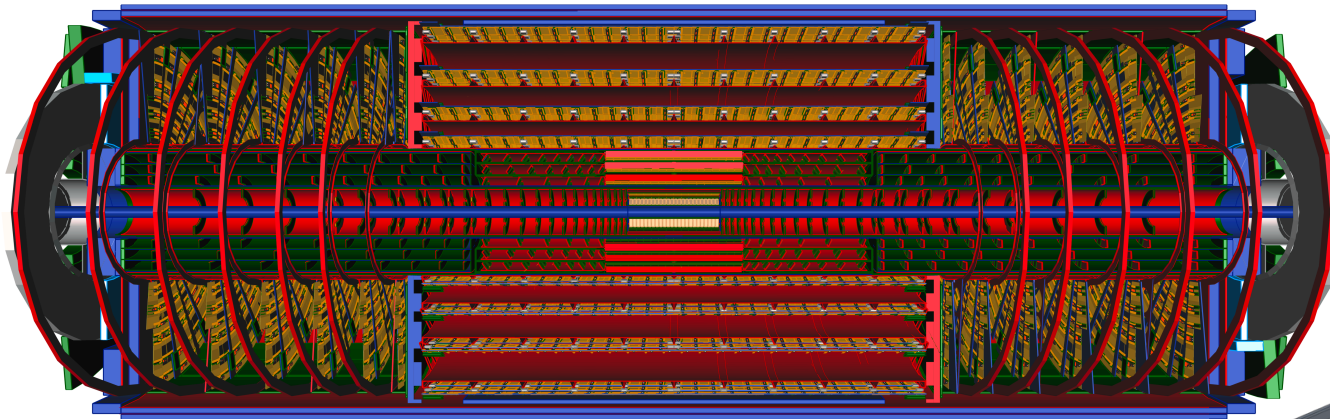
[ATL-PHYS-PUB-2021-024](#)



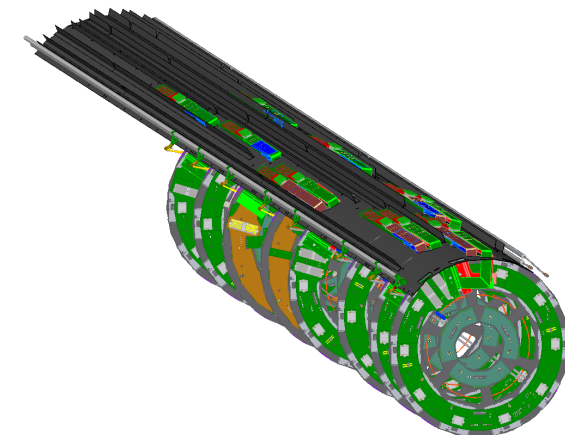
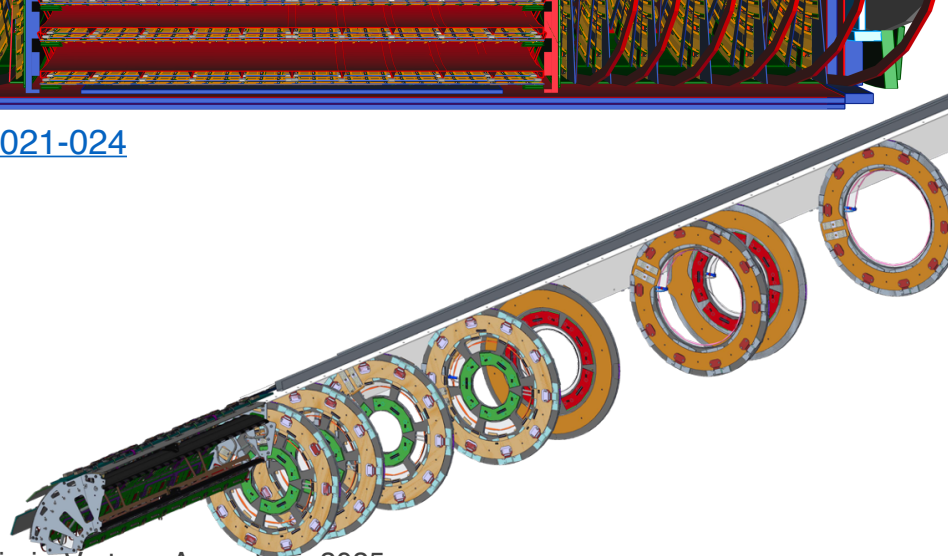
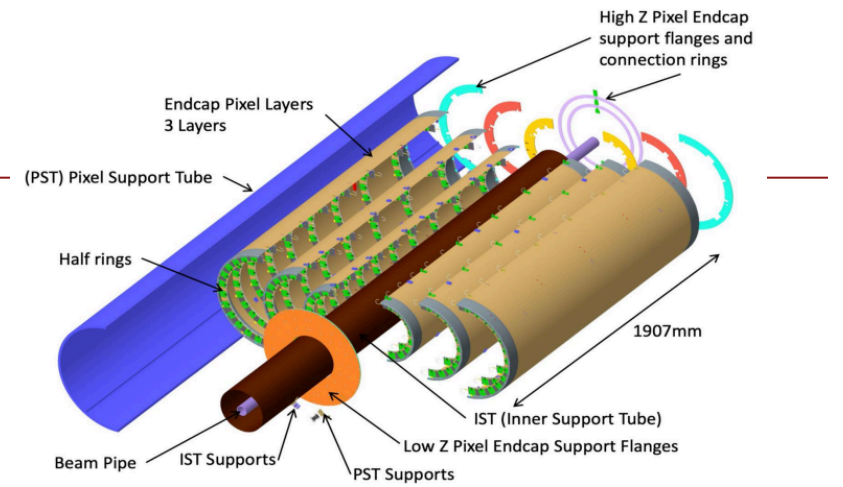
Integration

Complex large assemblies for both barrel and endcaps

Mock-ups and prototypes to validate the integration sequence and data transmission



[ATL-PHYS-PUB-2021-024](#)

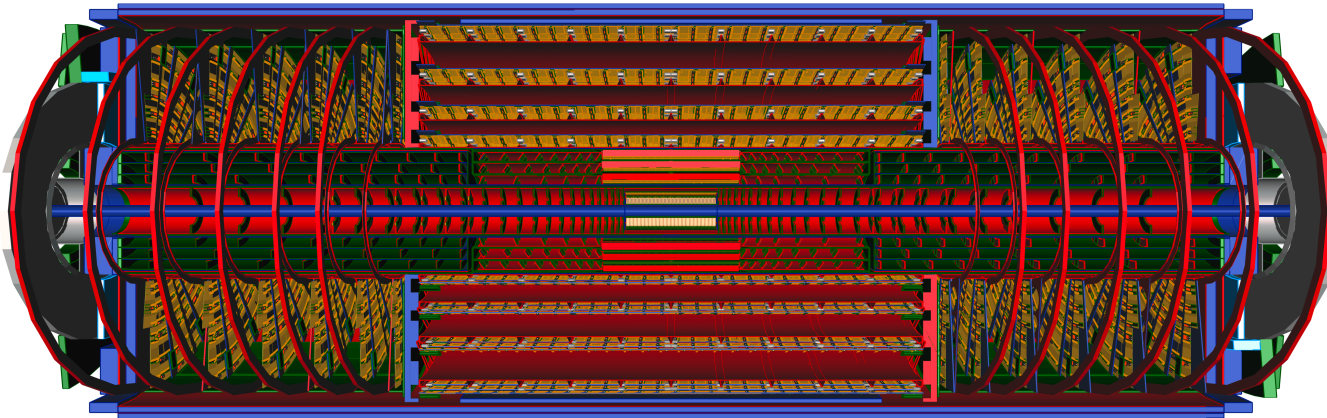


Integration cont'd

[ATL-ITK-PROC-2024-016](#)

Complex large assemblies for both barrel and endcaps

Mock-ups and prototypes to validate the integration sequence and data transmission



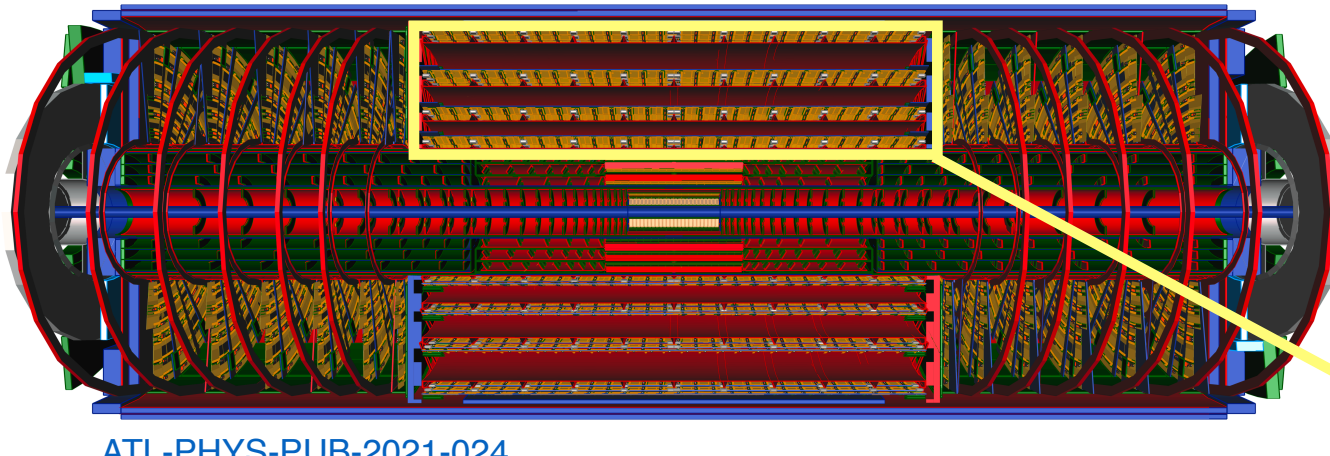
[ATL-PHYS-PUB-2021-024](#)

Integration cont'd

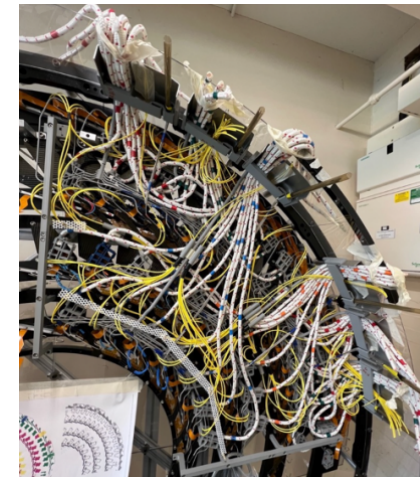
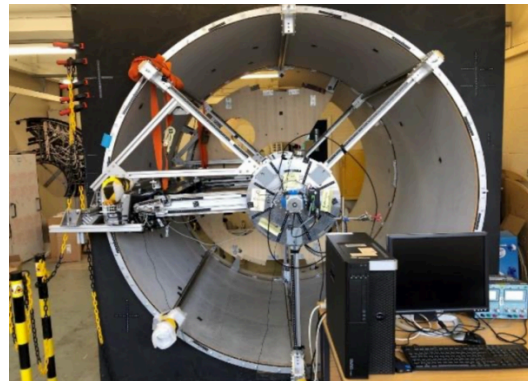
[ATL-ITK-PROC-2024-016](#)

Complex large assemblies for both barrel and endcaps

Mock-ups and prototypes to validate the integration sequence and data transmission



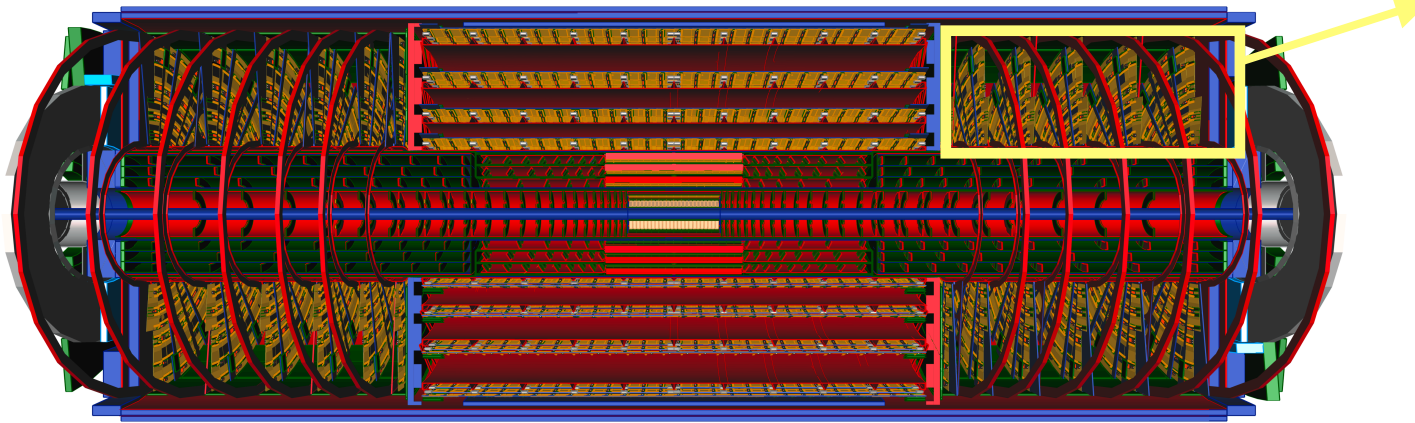
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Integration cont'd

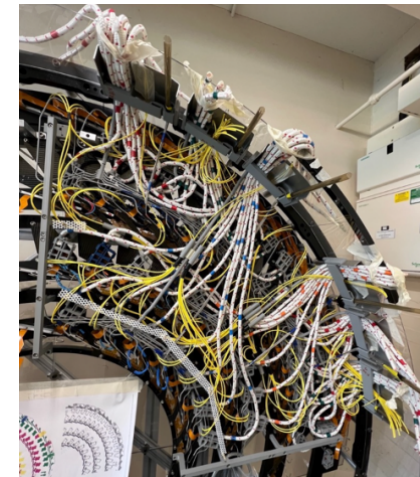
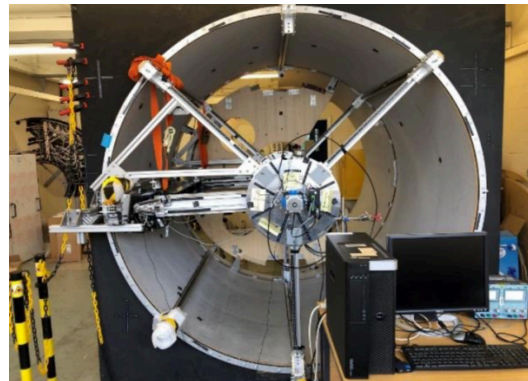
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[ATL-PHYS-PUB-2021-024](#)

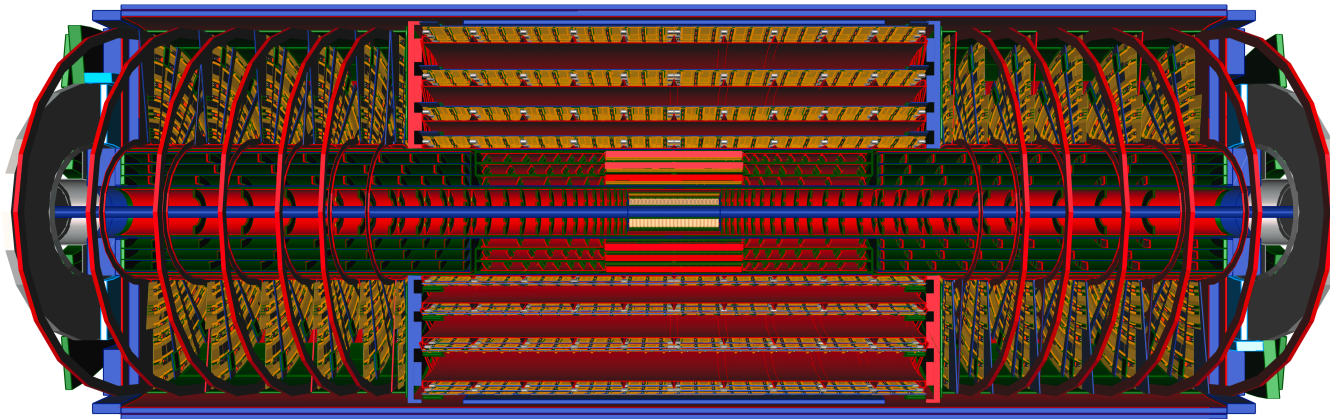
[ATL-ITK-PROC-2024-016](#)



Integration cont'd

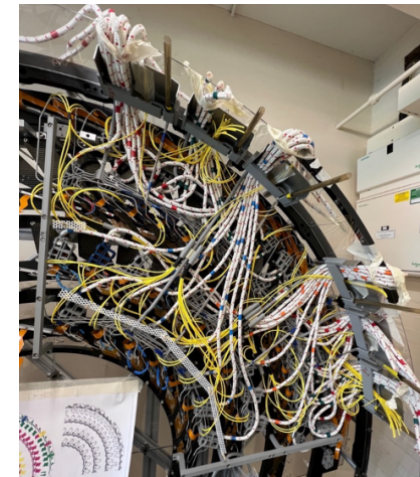
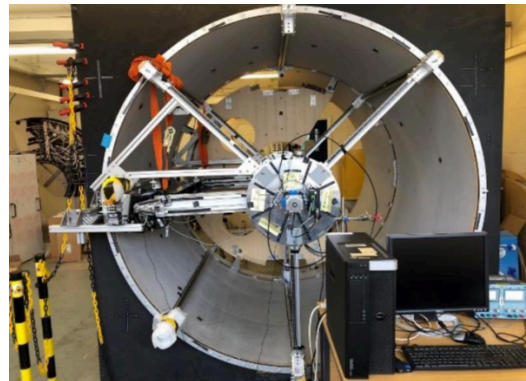
Complex large assemblies for both barrel and endcaps

Mock-ups and prototypes to validate the integration sequence and data transmission



[ATL-PHYS-PUB-2021-024](#)

[ATL-ITK-PROC-2024-016](#)



Mockups ...

Learning how to manage all the cables



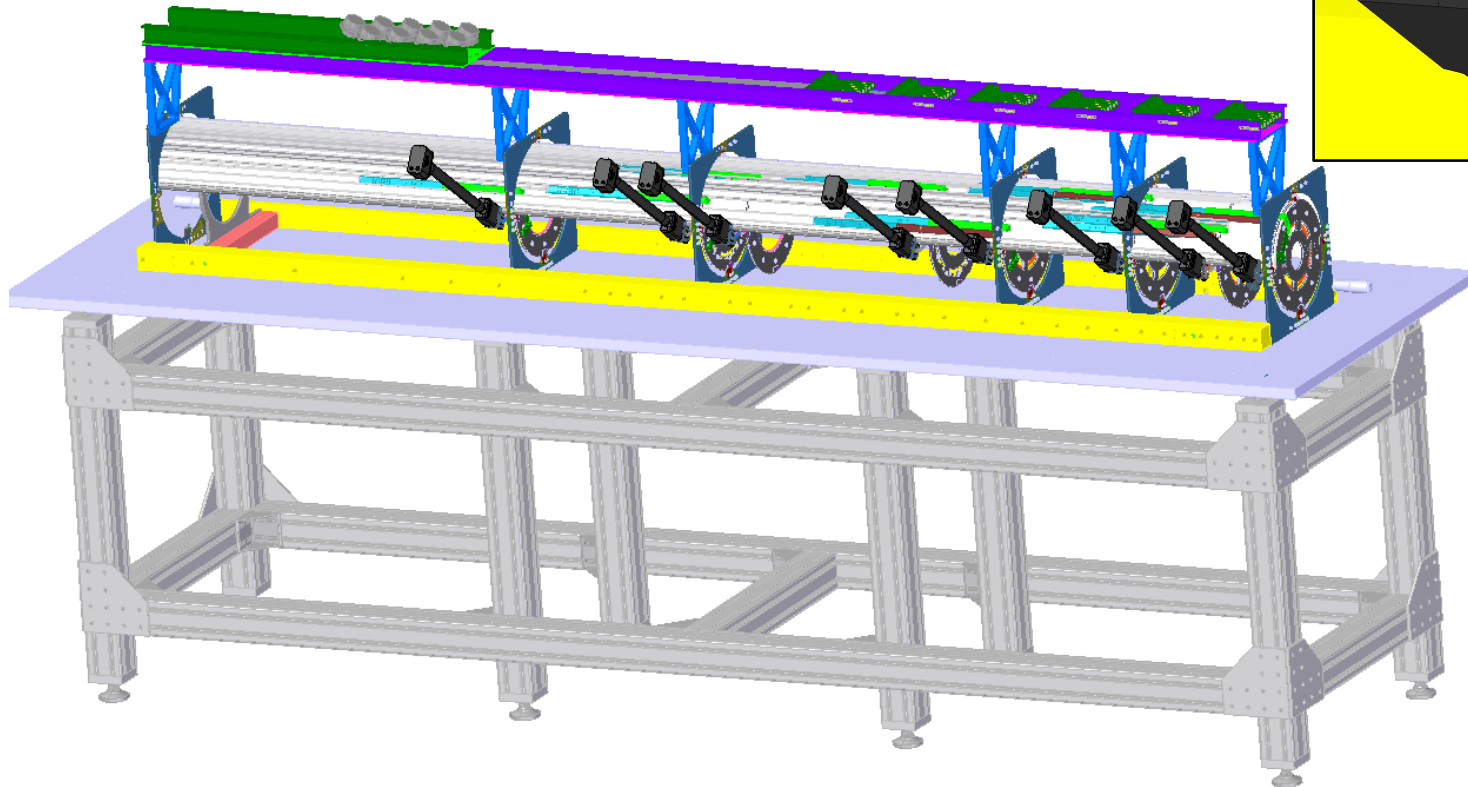
Mockups ...

Learning how to manage all the cables

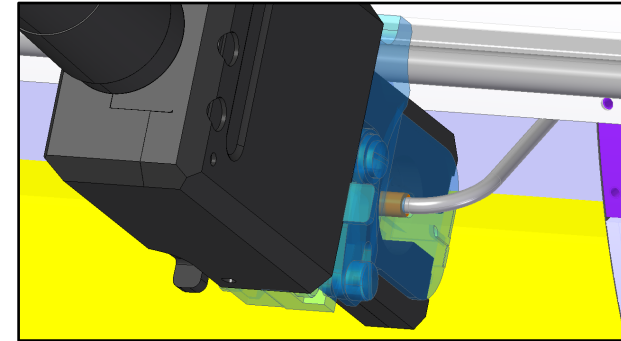


IS Endcap integration

One quarter shell at the time



CAD representation of the Quarter Shell assembly for the IS

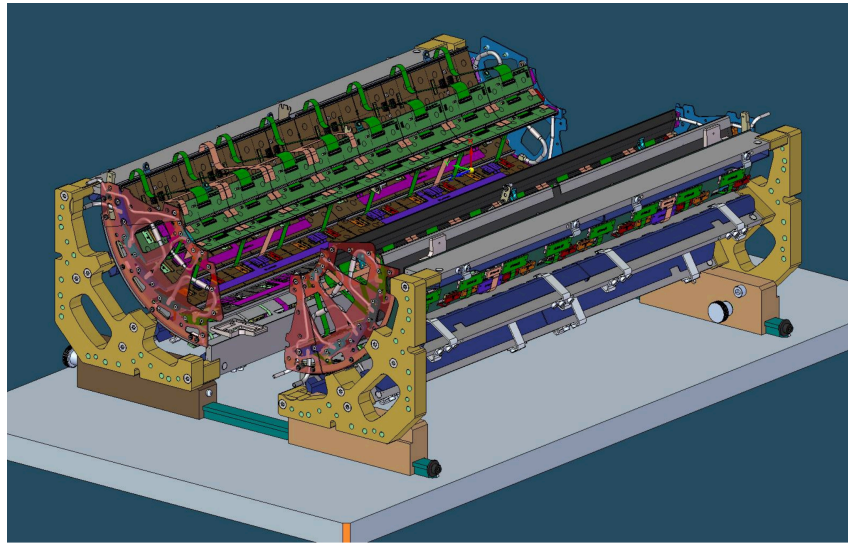


Weld Approach Angle is 35 Degrees

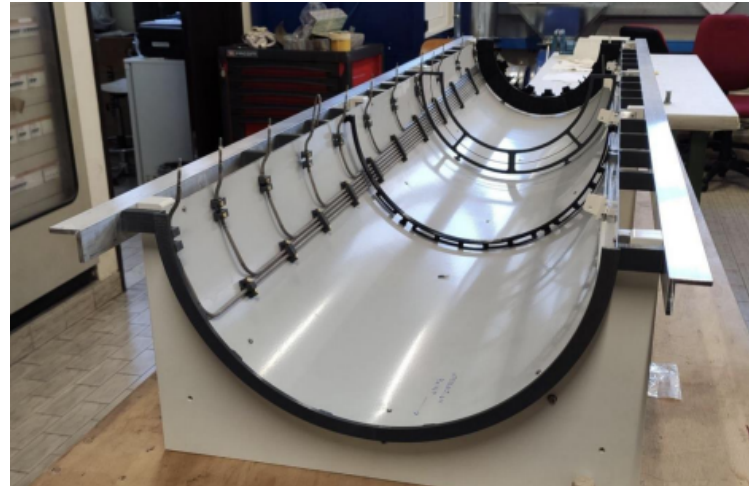


Mockup test

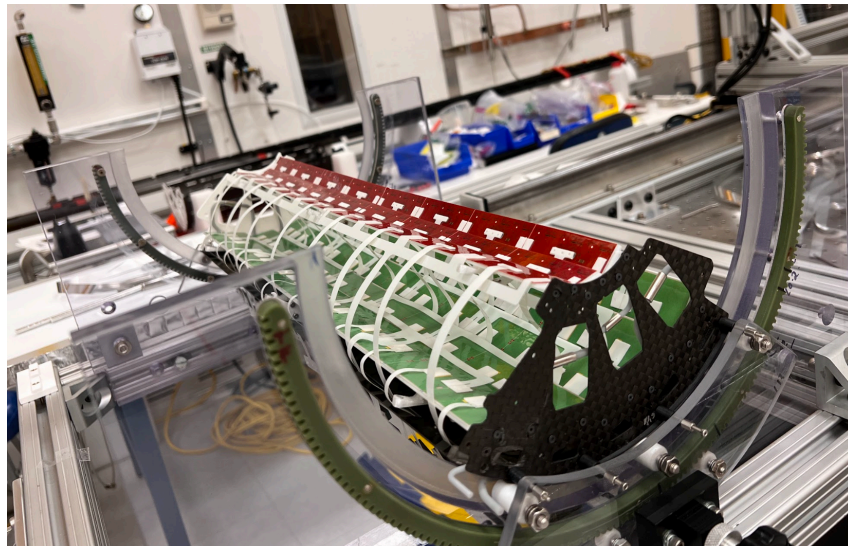
More Stages of integration



Integration test of L0+L1 barrel with 3D printed parts



Integration test of L2 cooling system on mockup half shelf

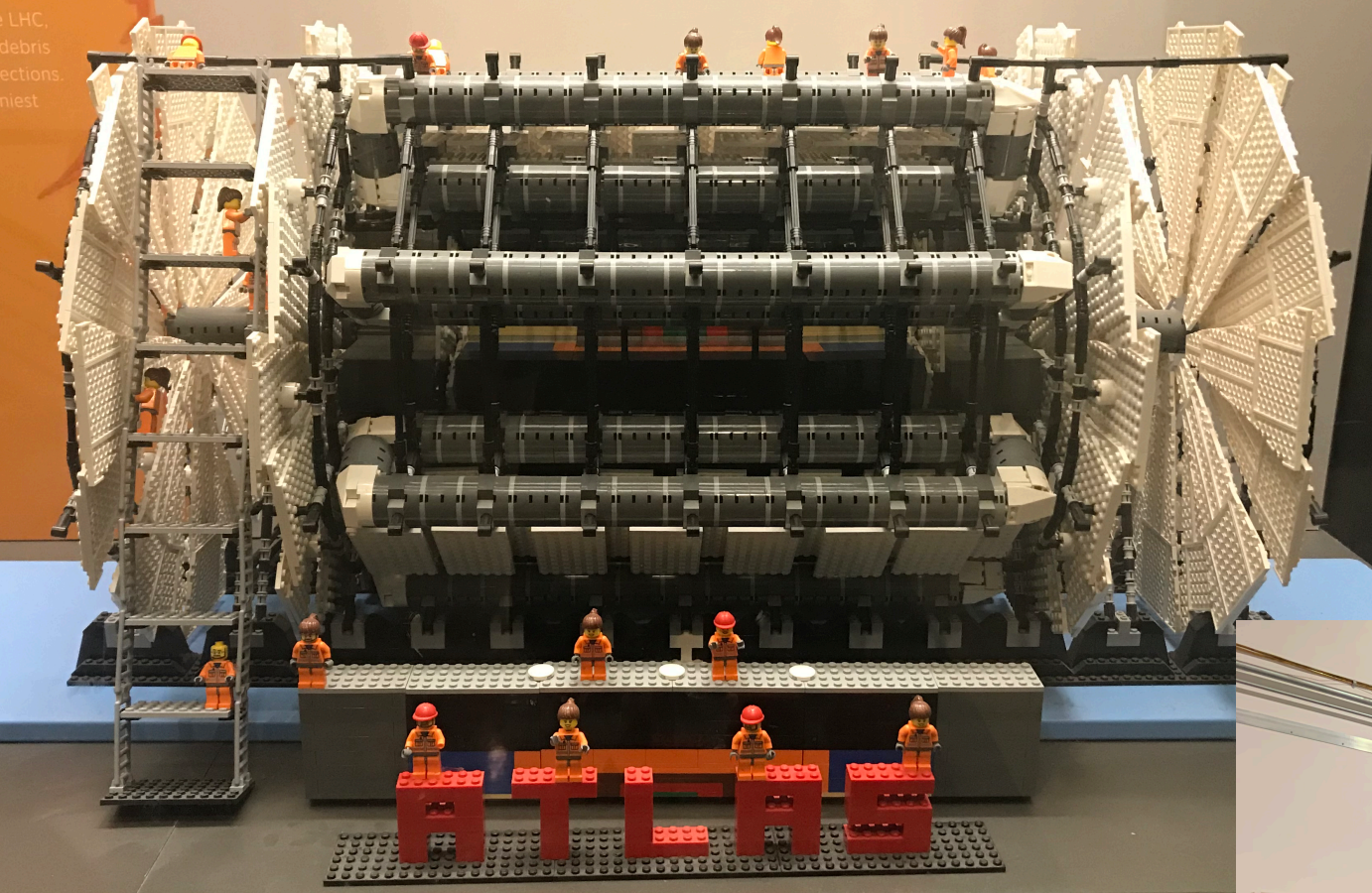


PP1 Glenair connector like mockups

Conclusions and perspectives

A new ATLAS detector for HL-LHC with the largest silicon detector ever built

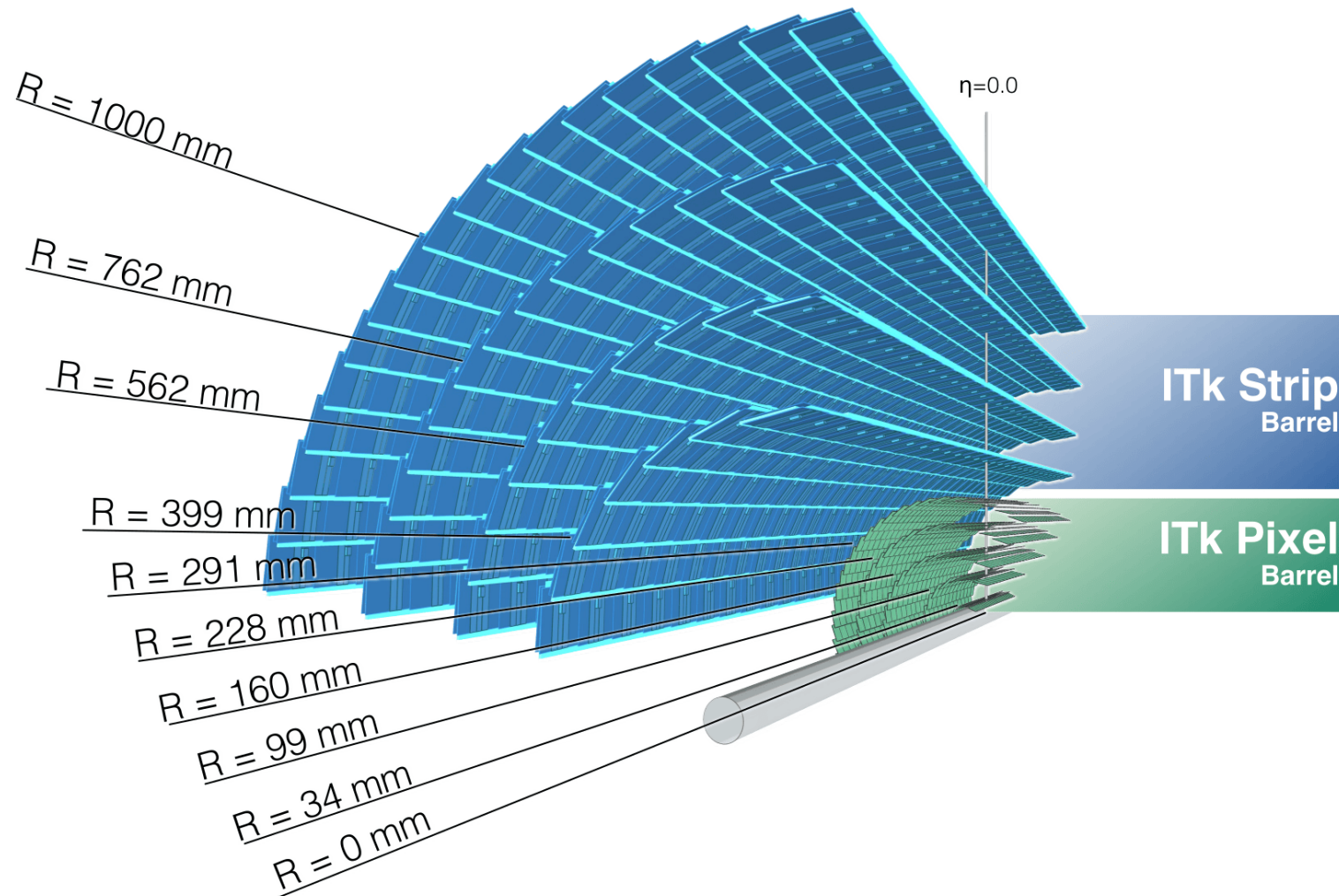
- An all silicon tracking system is being developed for the ATLAS experiment upgrade at the HL-LHC to cope with increased particle multiplicity and radiation levels.
 - **ITK will provide increased acceptance up to $\eta \sim 4$, a large number of points per track, high granularity and radiation hardness with minimized material budget.**
- The ITK systems have finalized an extensive prototyping & pre-production phase and have recently started production of some components.
 - System tests and demonstrators for all subsystems
 - Finalize production version of readout chip, services, loading and integration procedures.
 - Production will start by the end of 2025 and end by 2027 (pixel) / 2028 (strips)
 - Integration in 2028
 - **Commissioning starts in 2029**



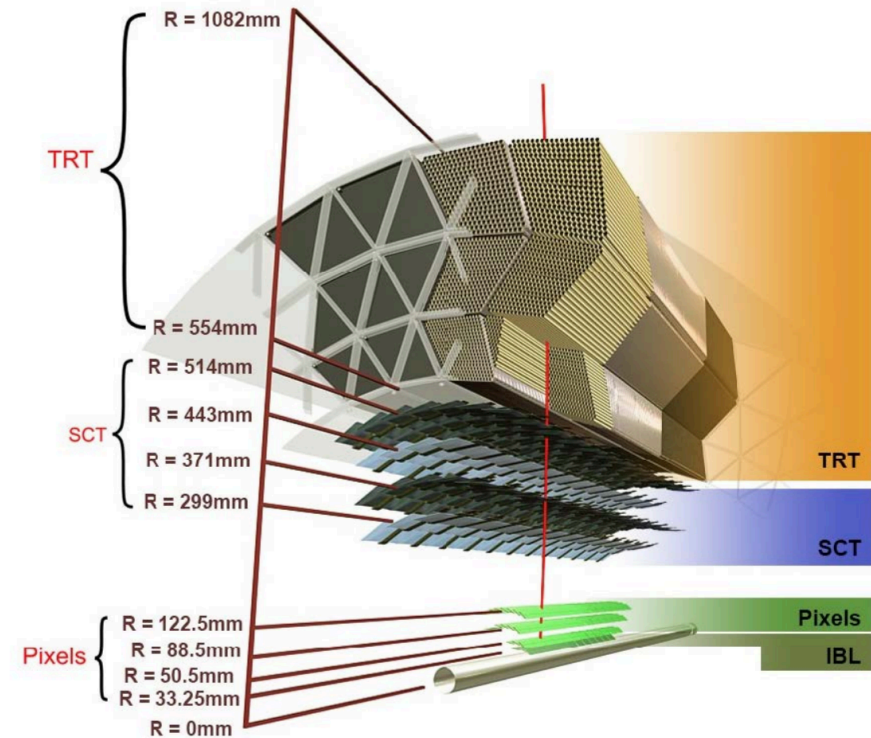
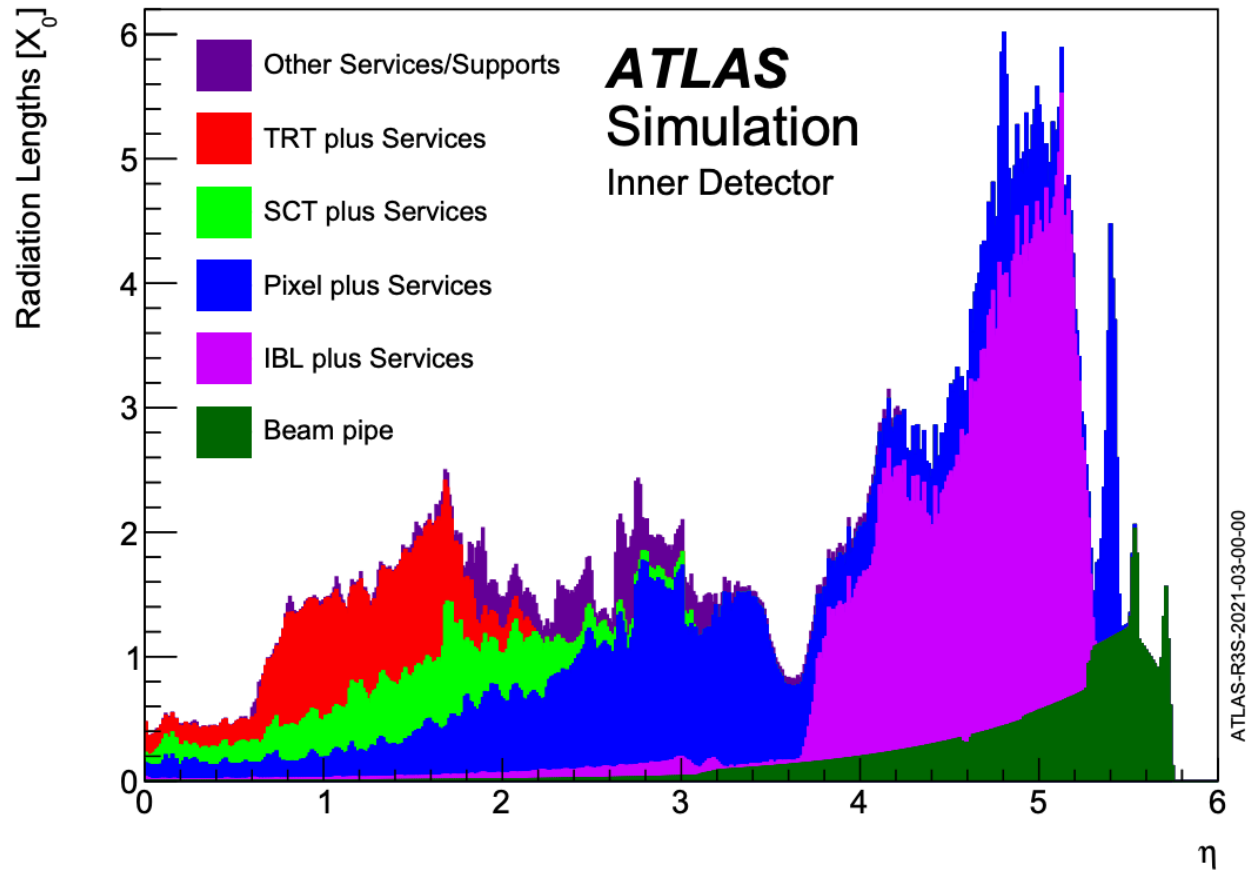
thank you!

ITk layout - R view

[JINST 20 \(2025\) P02018](#)

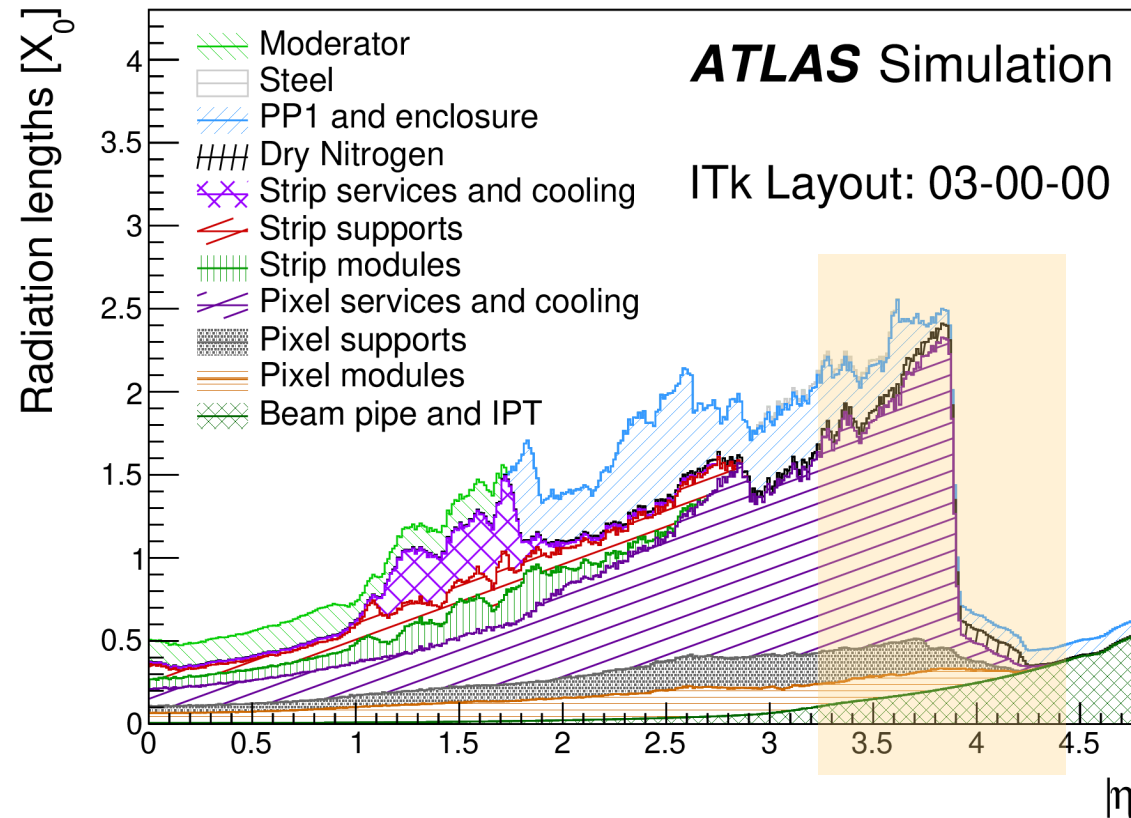


Current ATLAS detector



One more challenge: Material Budget

Lower material budget than ATLAS ID, from 1.6 → 0.6 X_0 at $\eta \sim 1$

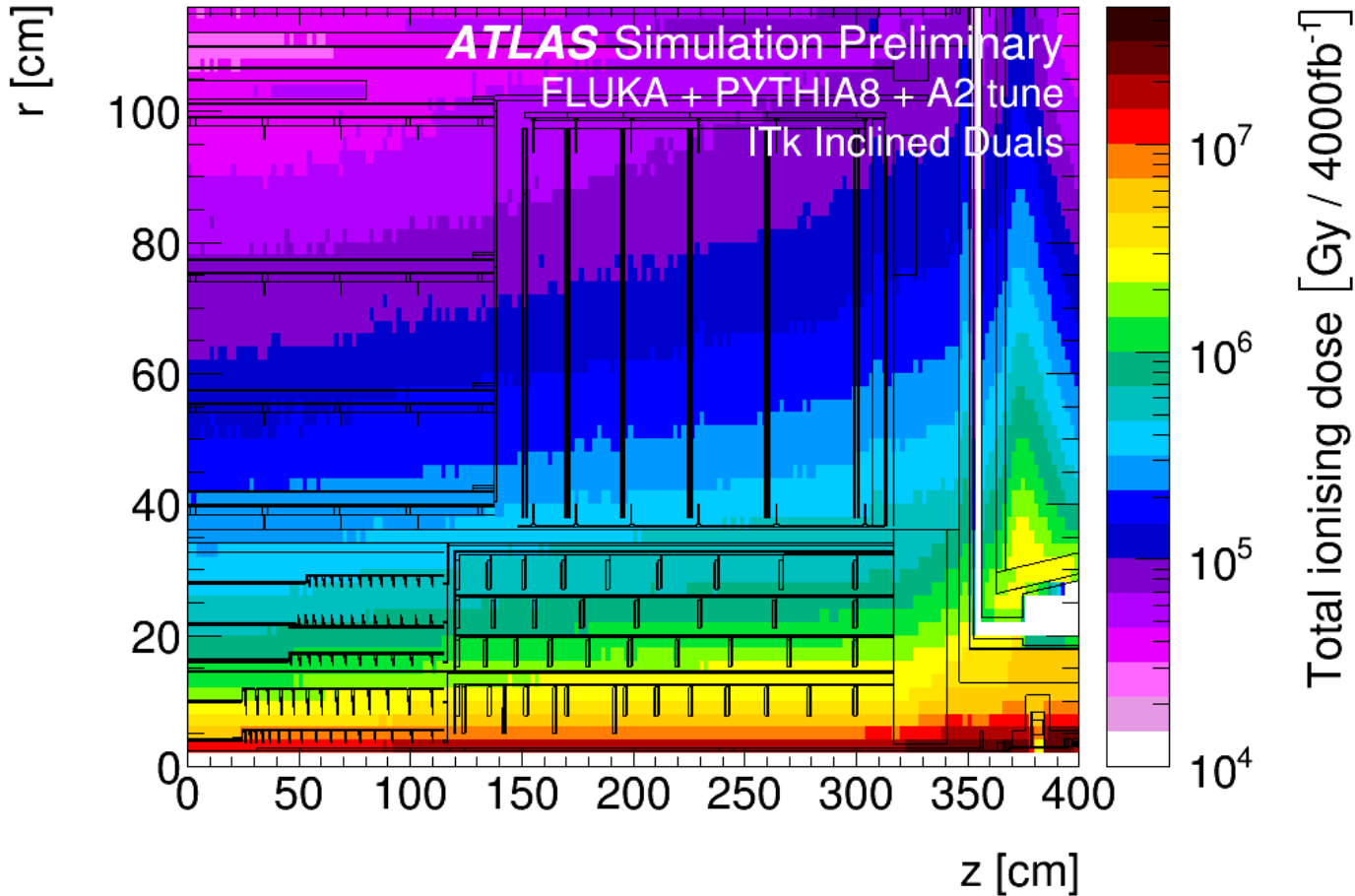


- **CO₂** two-phases cooling system
- **Carbon fiber structures** for local supports
- **Link sharing and serial powering** to reduce number of readout and power cables respectively

Pixel services: optical conversion outside the detector volume

Challenge

Radiation levels are unprecedented x 10 increased with respect to LHC



- For 4000/fb 2×10^{16} n_{eq} / cm^{-2} and [15 MGy](#)
- **Fluence** decreases as we move to large radius
 - The Inner system - first two layers - designed for up to **2000/fb**
 - ITk will be operated at -35C to mitigate radiation-induced damage and prevent thermal runaway

Wish list for the glue

The adhesive used for module loading should satisfy certain properties

Chemical cure (not solvent evaporation)

Minimum pot life 30 min

Cures at or close to room temperature

Good thermal conductivity ($> 1\text{W/mK}$)

Electrically insulating

Viscosity suitable for deposition with a standard commercial dispenser

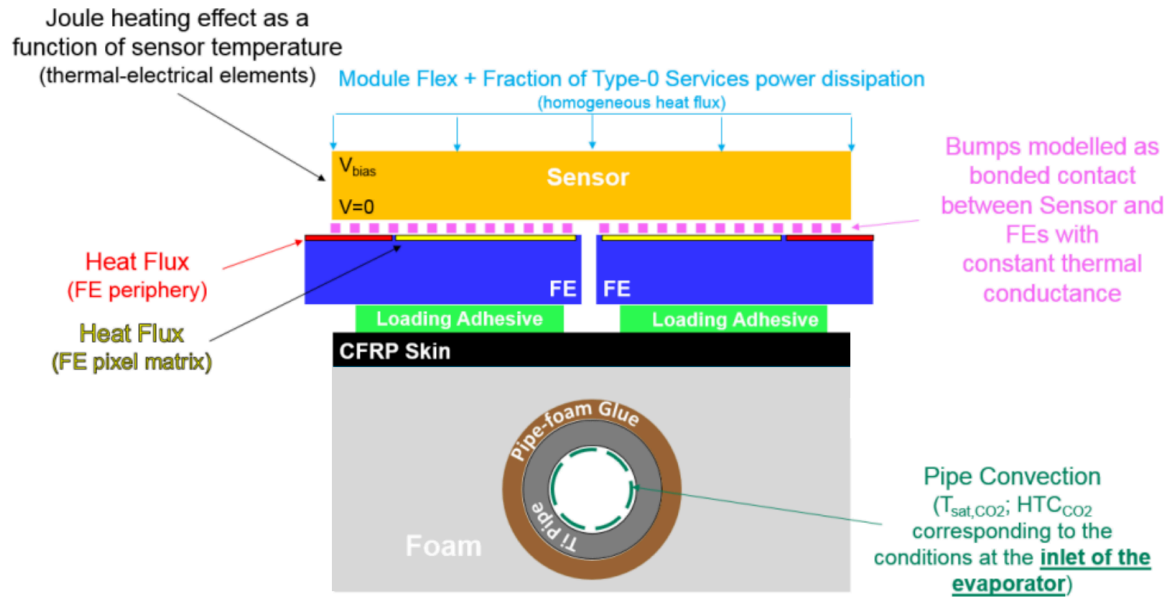
Viscosity low enough that excessive pressure is not needed to push the module onto the adhesive.

Reworkable – this in general implies softness/flexibility, a result of a low TG. Moderate heating may be used to soften such adhesives during rework.

Radiation hard – Lap joints, DCB and thermal conductivity to be tested.

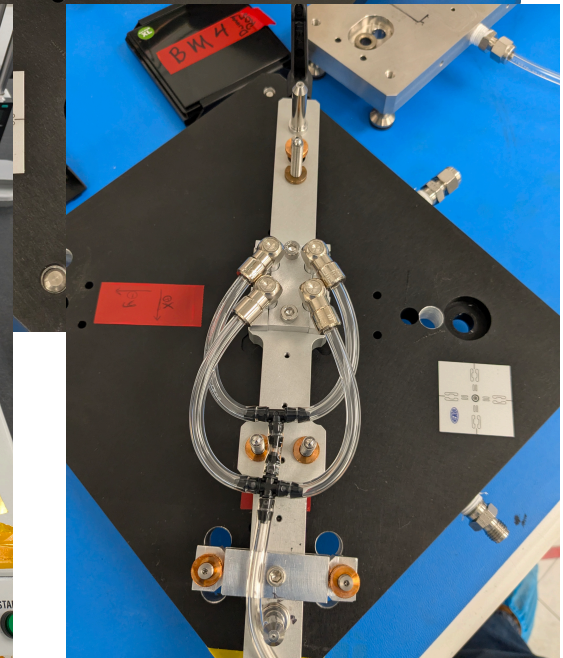
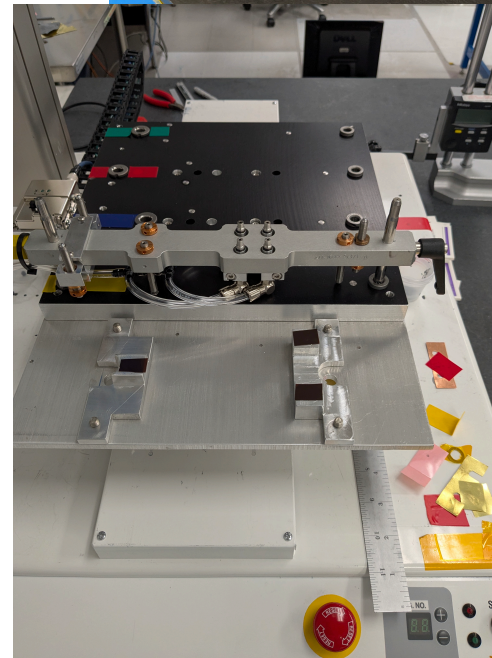
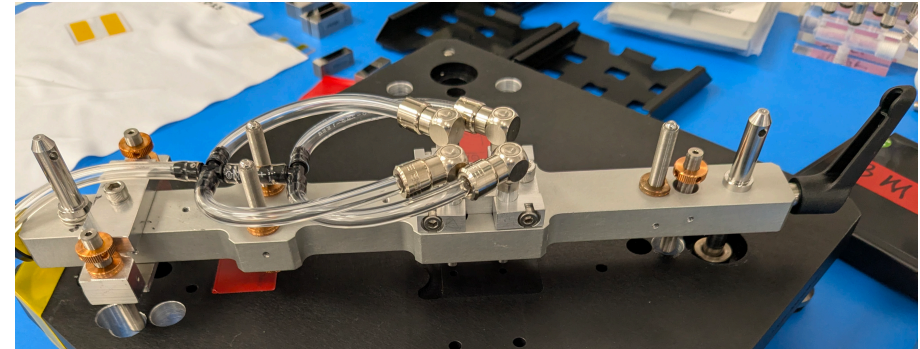
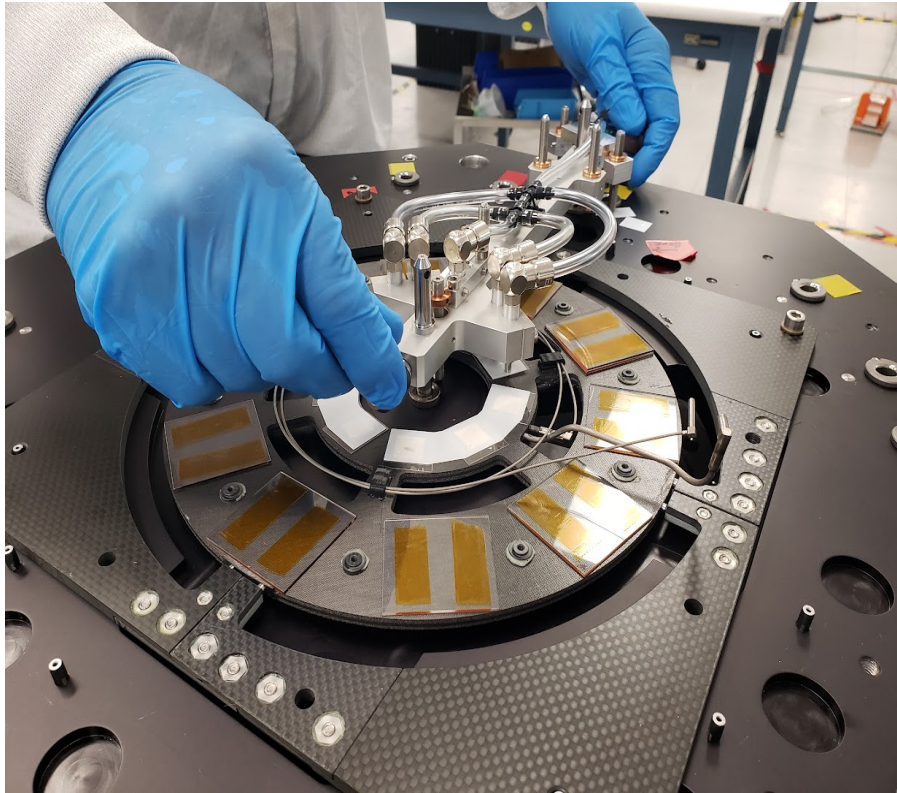
Cooling ITk - CO₂

- Two-phase properties allow efficient, stable heat removal with small tube diameters, low material budget, high radiation hardness, and minimal environmental impact.
 - Min cooling temperature during operation: -45C (100 cycles by end of life)
 - Min cooling temperature during a failure: -55C
- Simulations were used to derive the tube inner/outer diameters, the bending radius, and to validate the manifold structure through thermo-electric and thermo-fluidic modeling.
- The non-homogeneous power dissipation of the FE chip requires further optimization of the bending radius of the local supports.



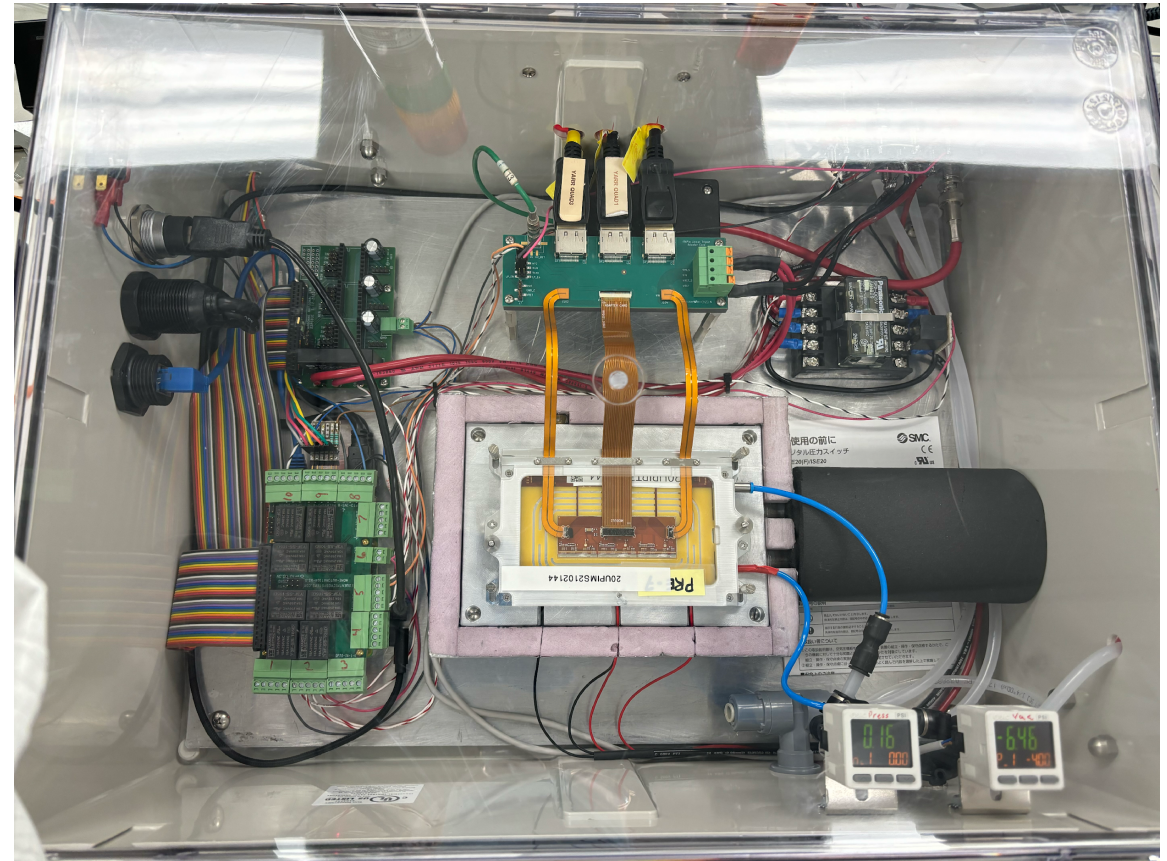
	Case 1		Case 2	
Sensor	Matrix	Periphery	Matrix	Periphery
3D	0.8	0.8	0.33	4.16
Planar	0.8	0.8	0.30	3.75

Ring & L1 tooling



Reception area

- We have 3 boxes from Argonne for module testing
 - One for each module flavor (L0, R0/R05, Q)
 - They can be operated in parallel
 - YARR readout
- Following module QC recommendations
 - Readout at 1.28 Gbps
 - Powering triplet at 5.5A (2V)
 - Module temperature $\sim 20^{\circ}\text{C}$ w/ water cooling
 - YARR software v1.5.2, firmware v1.4.0



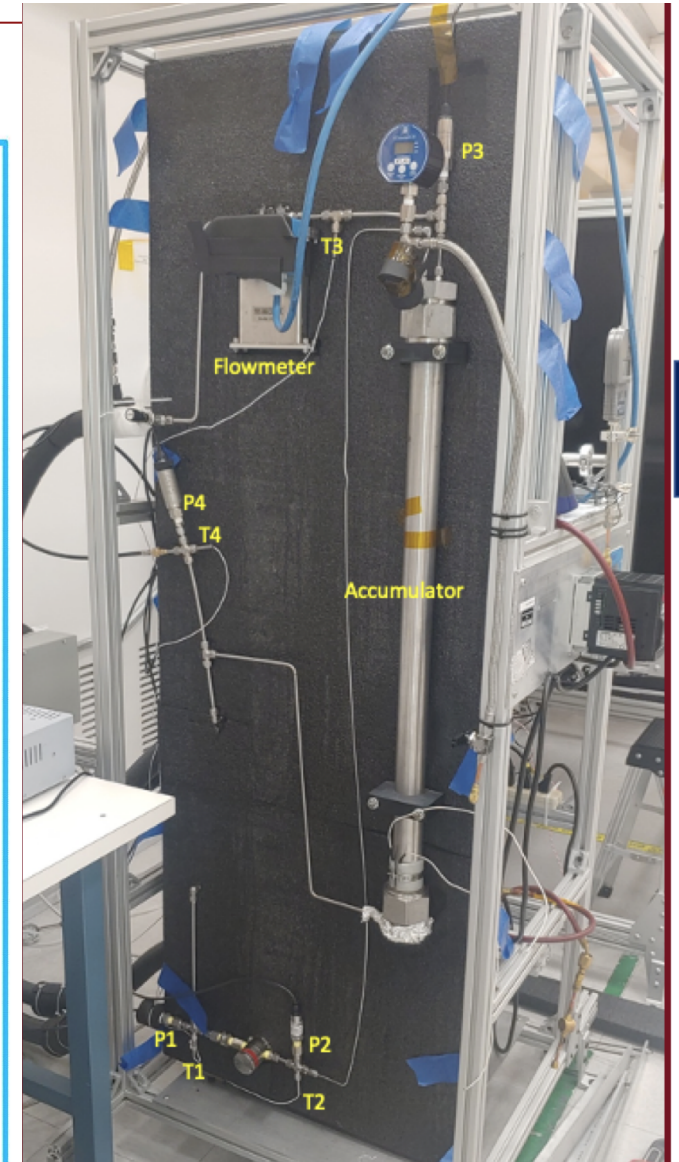
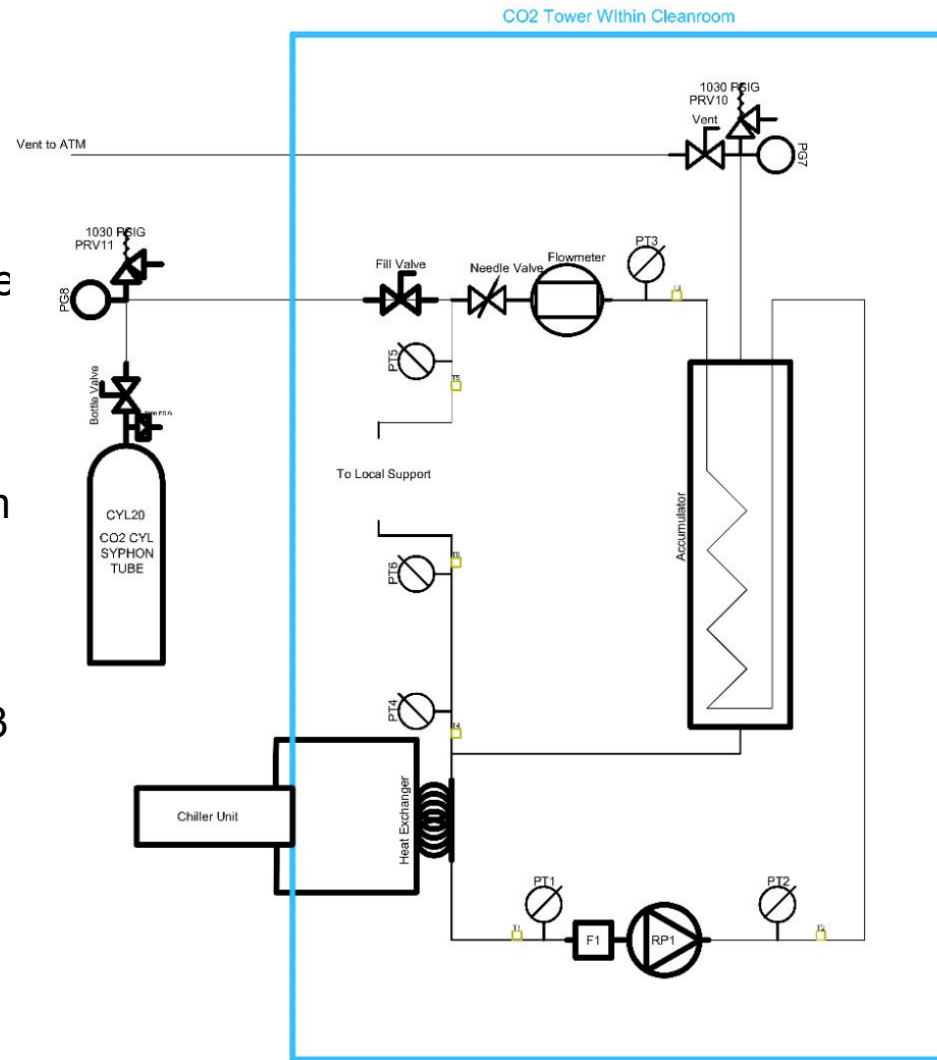
Module Reception tests at SLAC

List of tests we perform at SLAC as part of module reception

- Visual inspection :
 - One photo for full module, zoomed photo for each chip, and additional photos of notable features (checking for damage to wirebonds)
- At room temperature ~20C
 - Sensor I-V Scan
 - Digital, analog and threshold scans, Time-over-Threshold (ToT), and disconnected bump bond scan (i.e. both *Minimal Health Test* and *Pixel Failure Analysis*)
 - Using module's last configuration and thresholds - as derived during the module QC and uploaded to the ProdDB by the testing sites.
 - These results are then uploaded onto the production database and compared against the module QC results from the module QC sites.
 - Any significant deviations is investigated and reported
 - SLDO verification

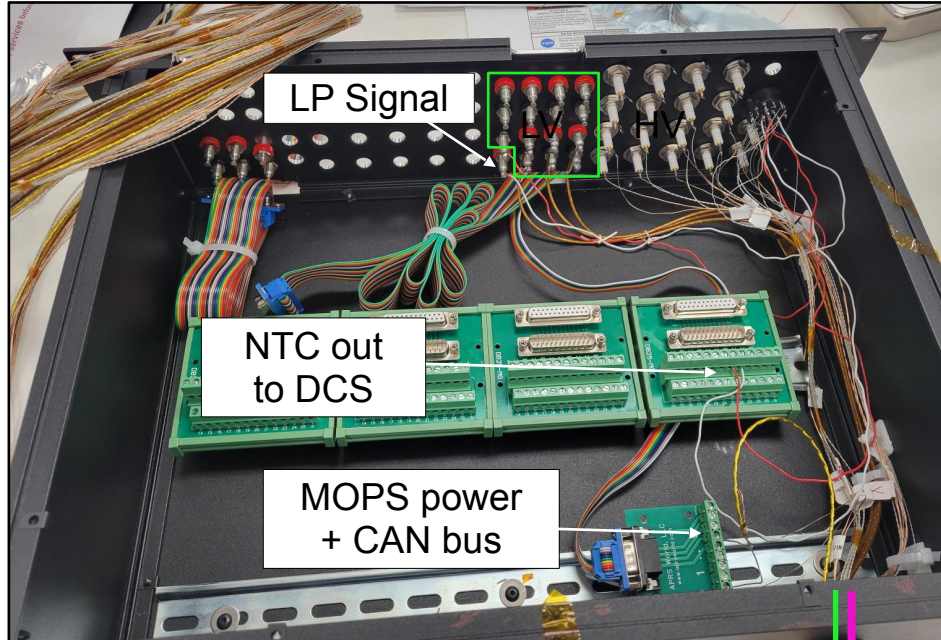
CO2 Cooling Plant at SLAC

- **Upgraded CO2 Plant**
 - New max ΔP 14 bar
 - Sufficient for ring capillarie
- Test Box dew point ~ -60 °C using dry-air
- Nominal CO2 pressure at room temp ~ 800 psi
- CO2 plant pump VFD ~ 12 Hz
- L0 Testing flow rate $1-2$ g/cm³

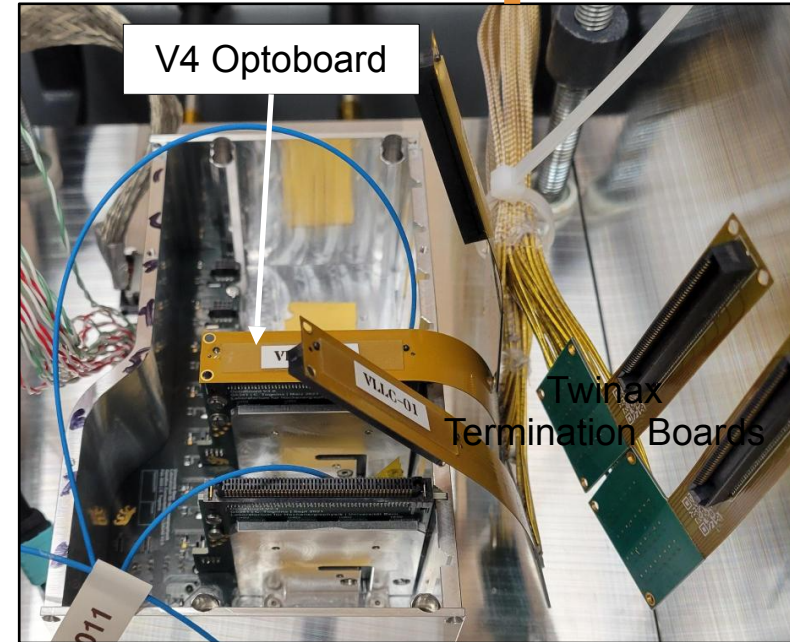


LLS Test Infrastructure - Type-1 Services + Data

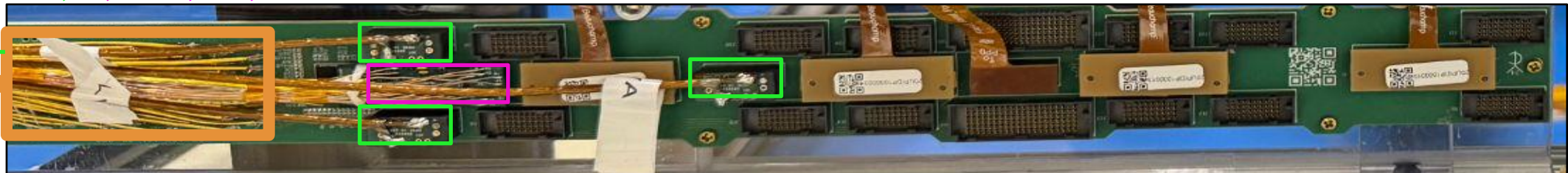
Type-1 Services Breakout Box



Optobox



Type-1 Services Bundle →
LV Power, HV, MOPS, NTC, LP Mode



Data Twinax Bundle →

L0 - disconnected bumps

