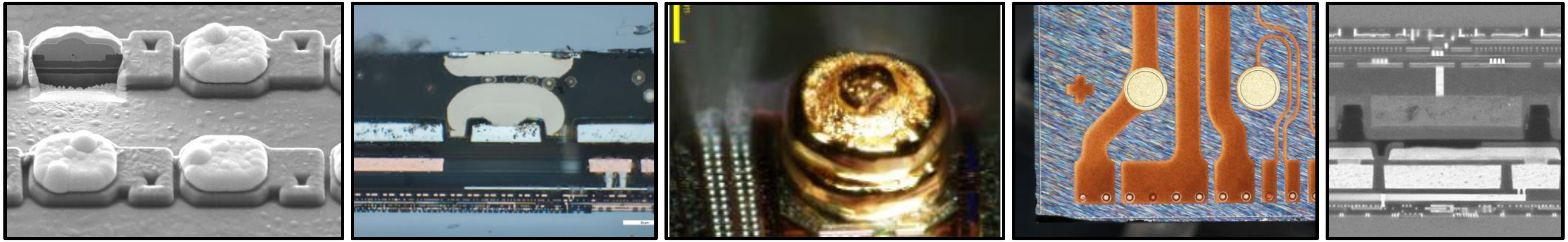
EP-DT
Detector Technologies

UNIVERSITÉ
DE GENÈVE
FACULTÉ DES SCIENCES

Novel interconnections for semiconductor detector modules



VERTEX 2025 – Knoxville, TN
28/08/2025

Mateus Vicente
on behalf of a large team at CERN and UNIGE

Introduction

1. Hybridization of pixel detectors and TSV integration
2. Beyond hybridization: Integration of MAPS and advanced modules
3. Hybrid with CMOS ("MAPS") sensors

Work from collaborations across multiple institutes and R&D programmes

Horizon 2020 program

CERN DRD 3 WG 7

CERN EP R&D WP 1.3

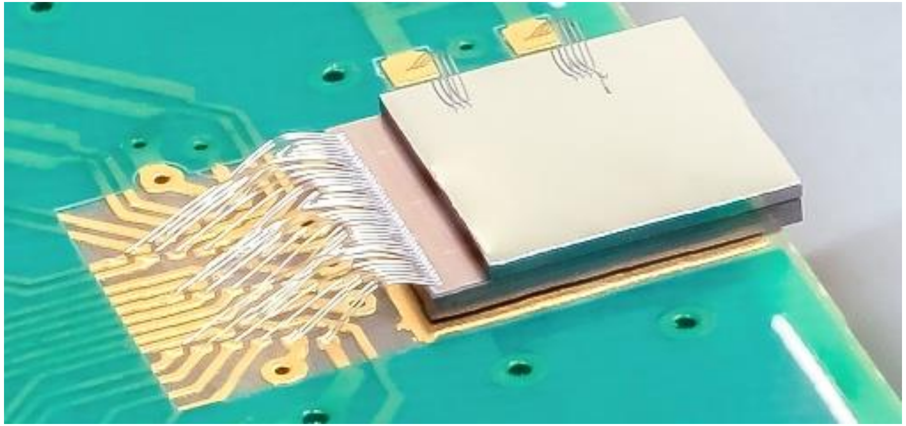
Semiconductor pixel detectors

Hybrid design

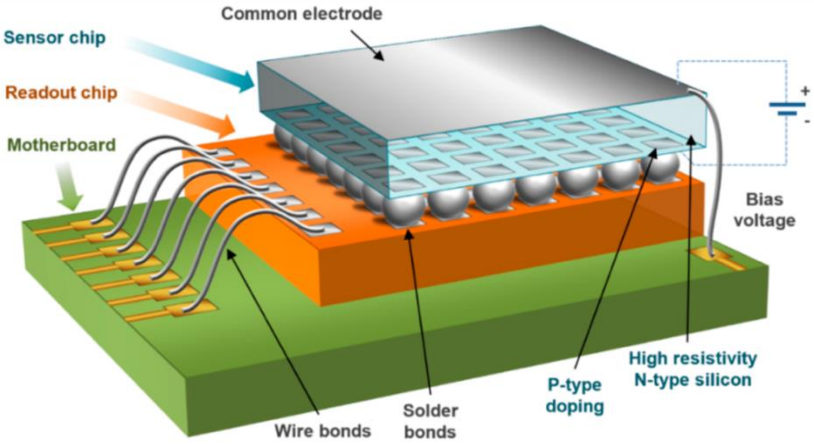
A hybrid design allows the optimization of the sensor and read-out chip (ROC) independently

- **Sensor:** matrix of multiple ~μm^2 collection electrodes for particle signal detection
  - Planar (Si, SiC, CdTe, GaAs), 3D, LGAD, SiEM, etc…
- **Read-out** mixed-signal ASIC: independent electronic cells/pixels to record the signal from each sensor electrode

CLICpix2 bump-bonded to Si sensor



Hybrid pixel detector illustration



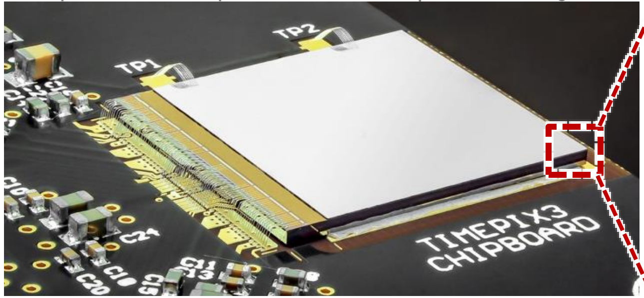
Hybrid pixel detectors

Bump-bonding interconnection

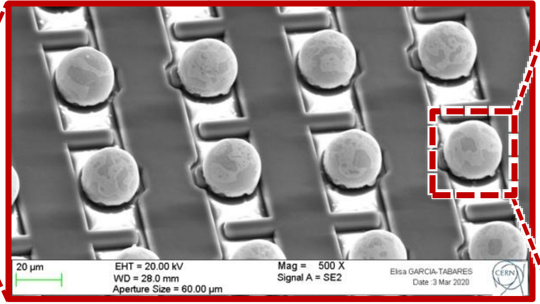
Standard interconnection technology ➔ **Bump-bonding**

☐ Photolithographic process; requires **full wafers**

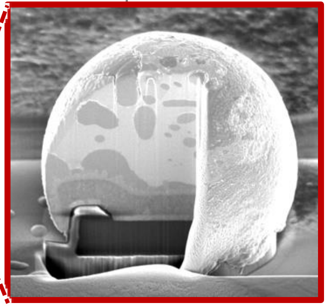
Timepix3 ROC bump-bonded to a 50 µm active edge silicon sensor

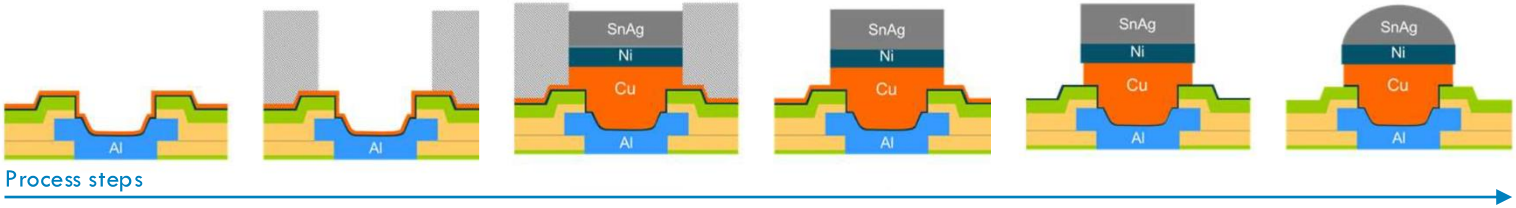


Solder bumps on the Timepix3 pixel matrix



Bump cross-section





Hybrid pixel detectors

Bump-bonding interconnection

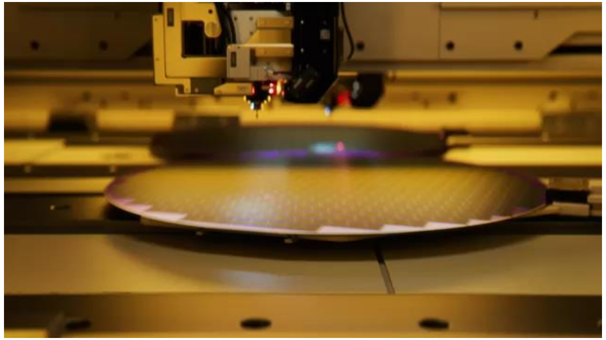
Standard interconnection technology ➔ **Bump-bonding**

- Photolithographic process; requires **full wafers**
- **Complex** and **expensive** → process can cost 10+ times more than the ASIC and sensor
  - **Not suited** for an **R&D** phase and **Multi-Project Wafer (MPW)** productions

Wafer processing line

Robotic wafer handling

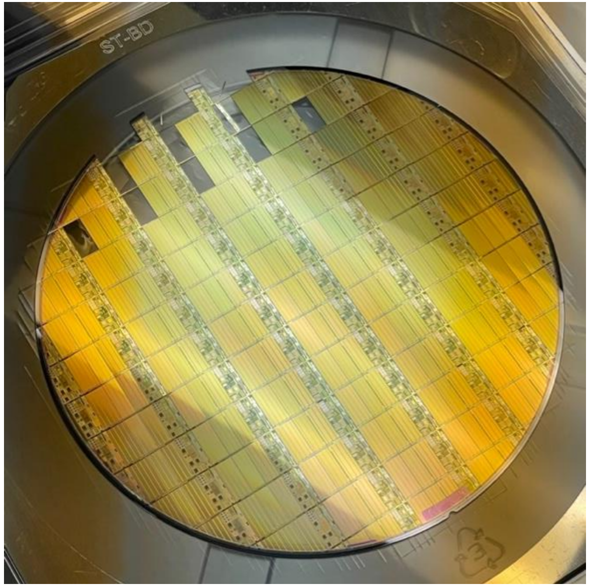
Wafer-level chip processing



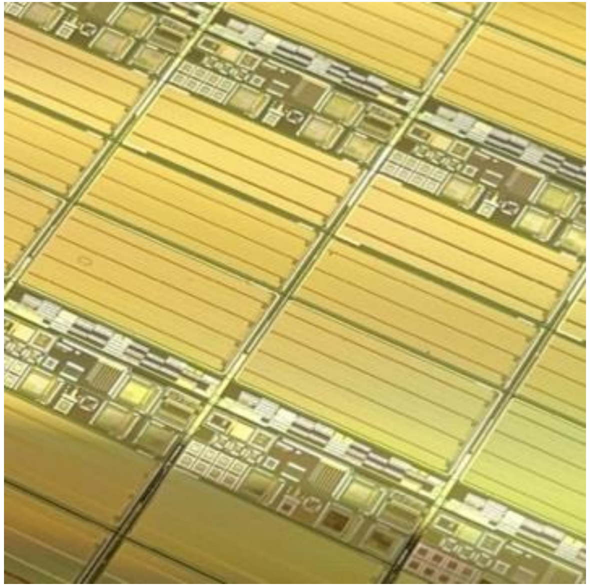
Getting the MPW ASICs and sensors

On **R&D** and **MPW** productions, we (usually) have access to singularized dies from a full wafer

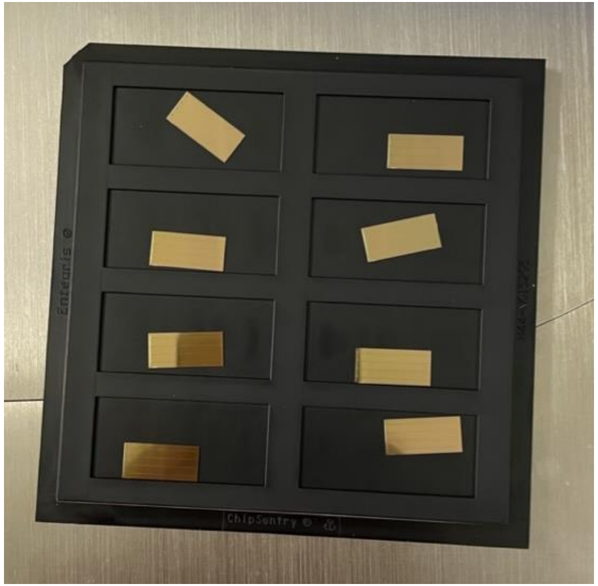
Wafer with multiple chips (FASER and ATLAS chips)



Zoom in wafer reticle with chips from multiple projects



FASER chips diced on waffle pack tray



Processing the MPW ASICs and sensors

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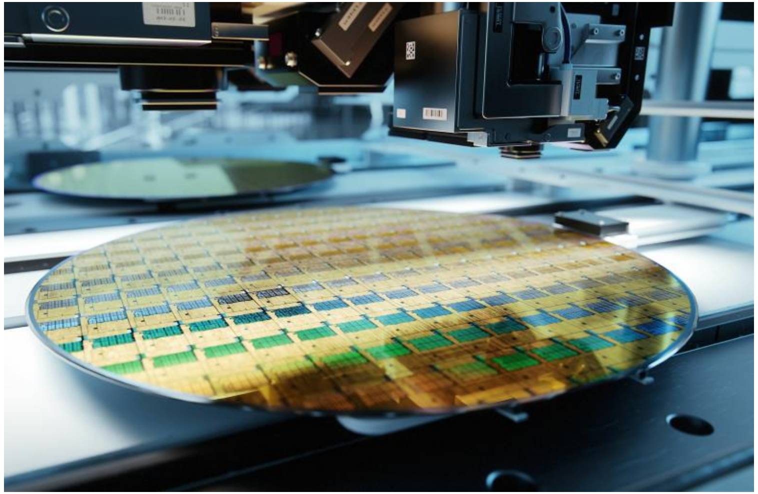
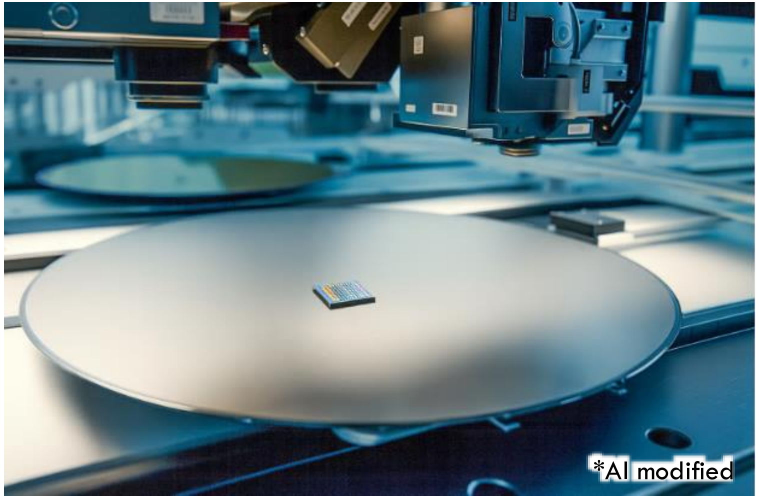
On **R&D** and **MPW** productions, we (usually) have access to singularized dies from a full wafer

☐ As we need wafer-level processes, we must rely on the same foundries

☐ They will use support wafers to adapt the process to singularized chips

☐ Price for 10s devices can go from **10k to 100k EUR**

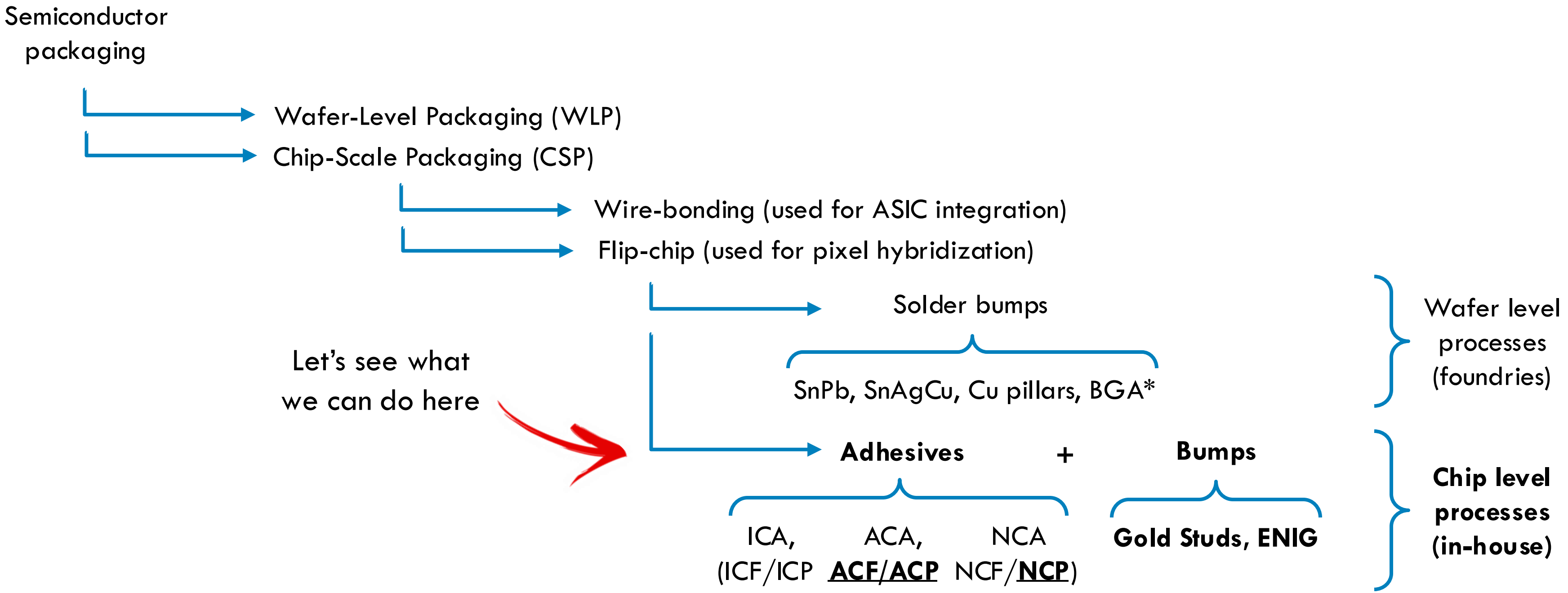




*AI modified

What else can we do?

Interconnection landscape



- Semiconductor packaging
  - Wafer-Level Packaging (WLP)
  - Chip-Scale Packaging (CSP)
    - Wire-bonding (used for ASIC integration)
    - Flip-chip (used for pixel hybridization)
      - Solder bumps: SnPb, SnAgCu, Cu pillars, BGA*
      - **Adhesives** + **Bumps**
        - Adhesives: ICA, (ICF/ICP), ACA, (**ACF/ACP**), NCA (NCF/**NCP**)
        - Bumps: **Gold Studs, ENIG**

Wafer level processes (foundries)

Chip level processes (in-house)

Let's see what we can do here

I = Isotropic A = Anisotropic N = Non
C = Conductive A = Adhesive F = Film P = Paste

*for large pixels, and also for ASIC integration

Anisotropic Conductive Adhesives

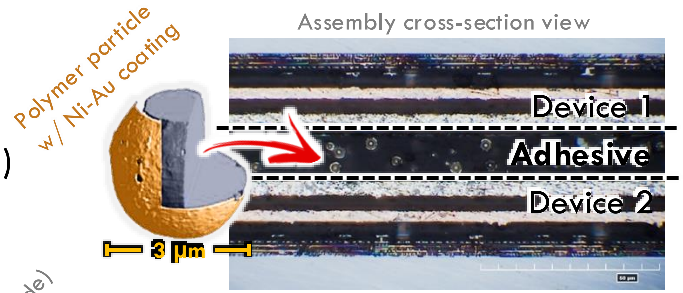
Typical application: Consumer electronics (COB, COF, COG, BOF, FOB, FOG…)

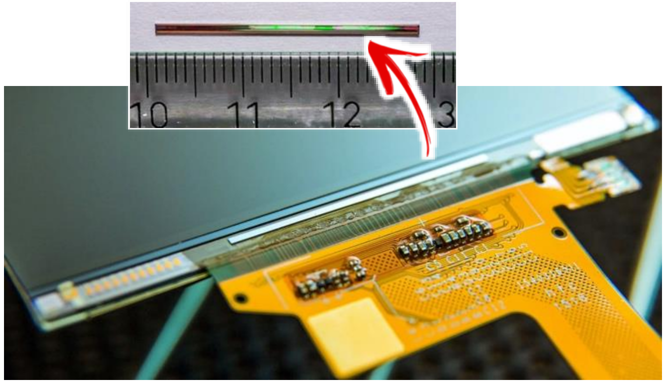
Narrow display driver ICs and long rows of connections

Adhesive film (ACF) or paste (ACP) embedded with **Conductive Particles** (CP)

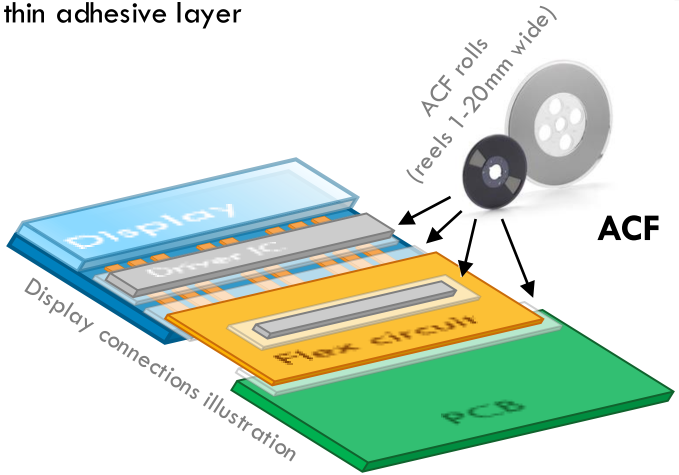
- **Vertically compressed** CP connect electrically the pads of the devices
  - **Mechanical bonding** is achieved with the thin adhesive layer

Assembly cross-section view



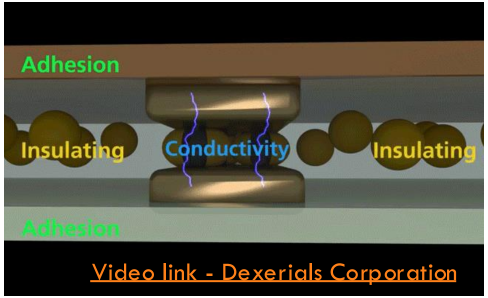


From: https://www.synaptics.com/products/display-drivers



Display connections illustration

ACF on contact pads



Video link - Dexerials Corporation

Bonding topology/interface for ACA

ENIG – Electroless Nickel Immersion Gold

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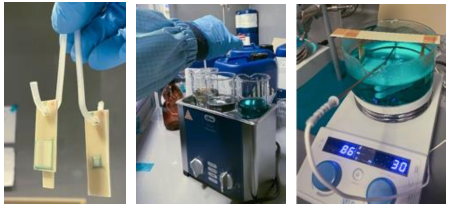
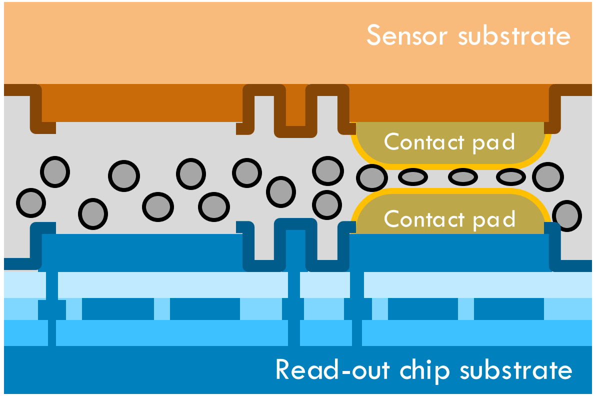
Elevated pads are needed to **pinch** the ACF particles and establish the electrical contact

- ENIG is a **wet chemical** deposition of **Ni** and **Au** (without external electrical current)
  - Self-patterning on exposed metal contacts under **passivation layer openings**
    - **Maskless chip-level "Under Bump Metallization" process ➔ Low cost**

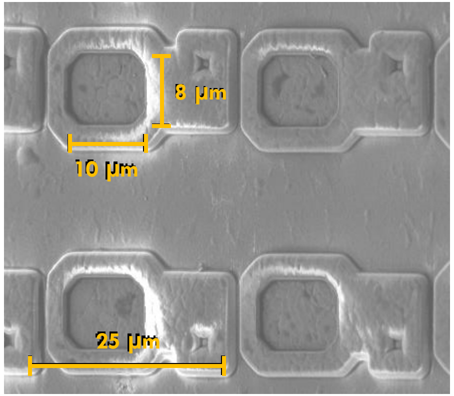
Samples and chemical baths



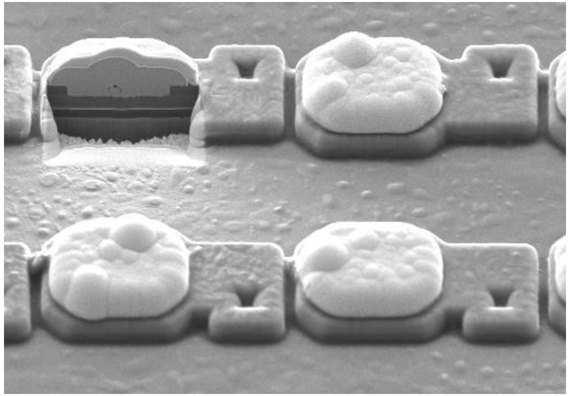
Plated *VS* Unplated pixels



Bare CLICpix2 pixel matrix

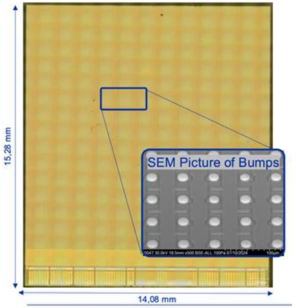


CLICpix2 pixels after ENIG

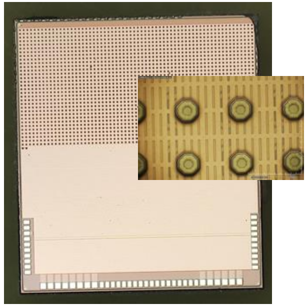


ENIG plating at CERN

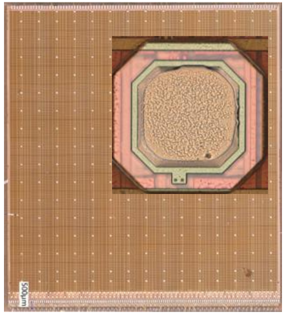
Timepix3



SPHIRD

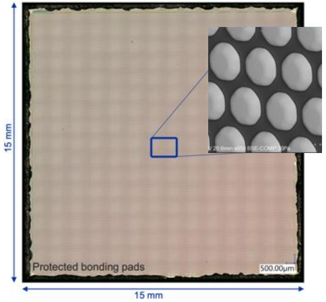


ALTIROC

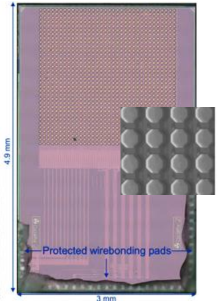


SiGE KEK

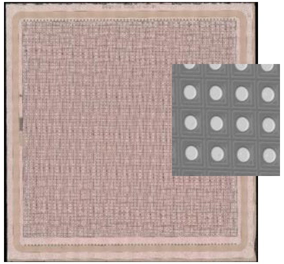
XPOL-III



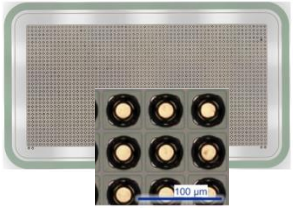
COLORPIX



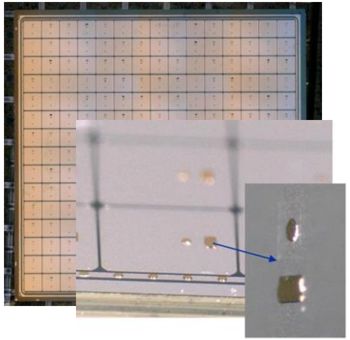
Ti-LGAD sensor



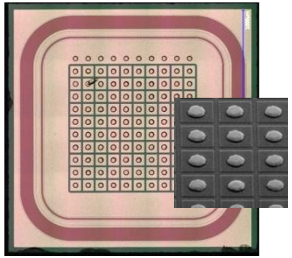
Silicon sensor



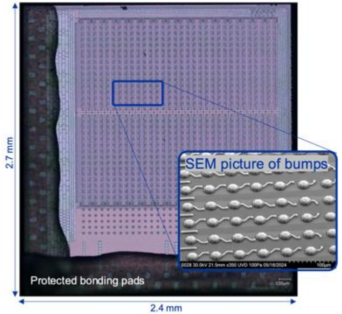
LGAD sensor



LGAD sensor

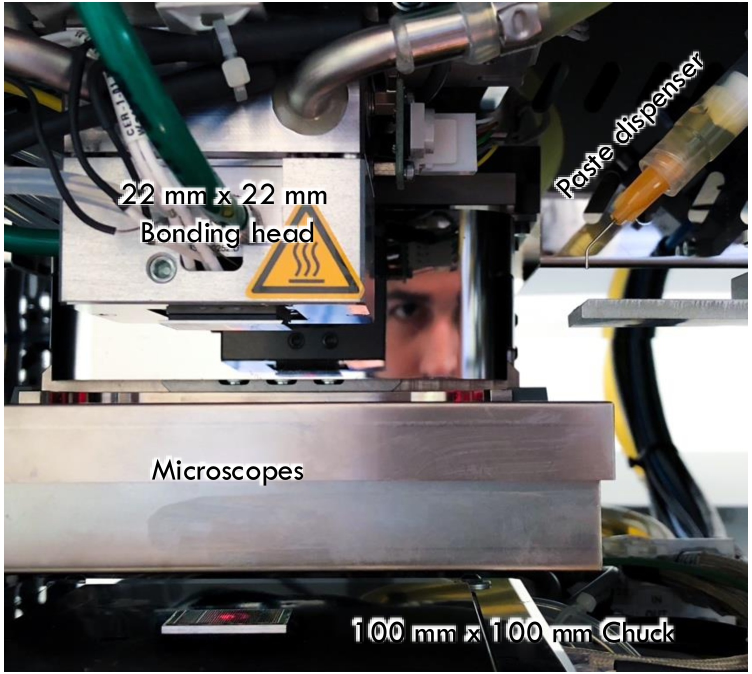


TimeSPOT



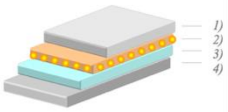
Flip-chip device bonder

- **Semi-automatic flip-chip** bonder, installed at Geneva University
  - Post-bonding accuracy **~2 µm** achieved and planarity **< 100's µrad**
  - Heating up to **400 ℃** and force applied by bonding arm up to **100 kg**



Flip-chip bonder

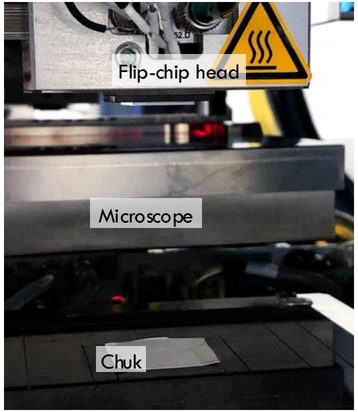
ACF thermocompression bonding

Structure and thickness	1) Cover film / color	25µm / transparent	
	2) ACF-layer	8µm	
	3) NCF-layer	10µm	
	4) Base film / color	38µm / white	
Conductive particles	1) Material	Ni plated polymer	
	2) Insulator coated	Yes	
	Particle diameter	3µm	
	Particle density	71.2k pcs/mm^2	*Design value. Calculated in ACF later*

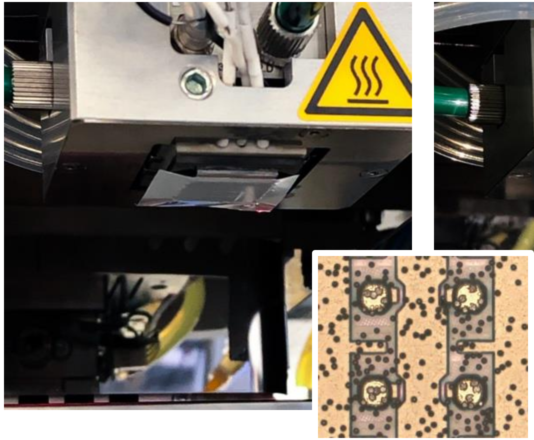
ACF laminating conditions	Temperature	50～80℃
	Pressure	0.5～1.0MPa
	Time	1～2sec
Main bonding conditions	Temperature	150℃～180℃
	Pressure	30～80MPa *
	Time	5sec

* 300–800 kgf/cm^2

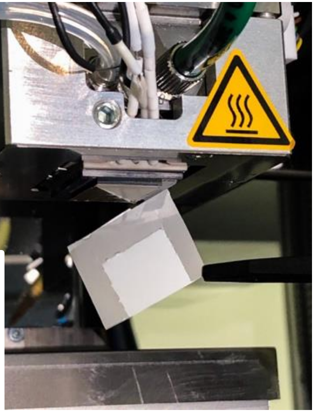
TPX3 (top) and ACF (bot)



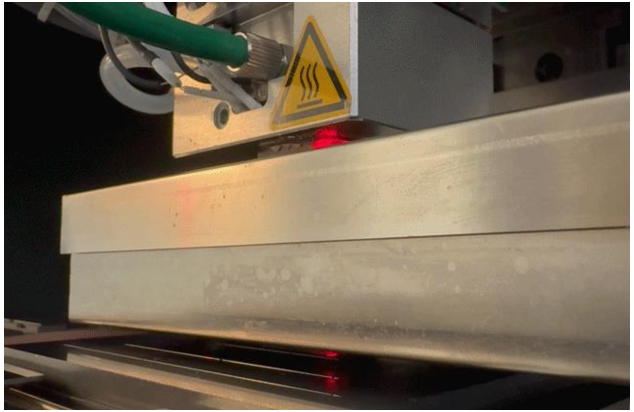
ACF lamination to ASIC



Removal of ACF protective cover film



TPX3 to sensor bonding stage with ACF in between

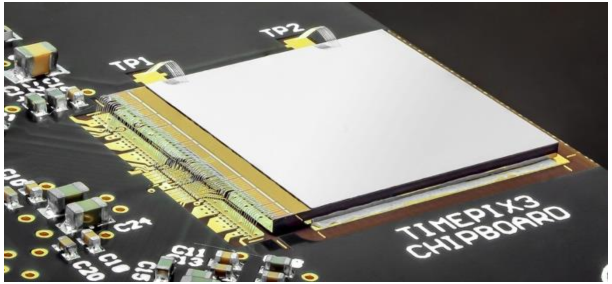


Hybrid pixel detectors

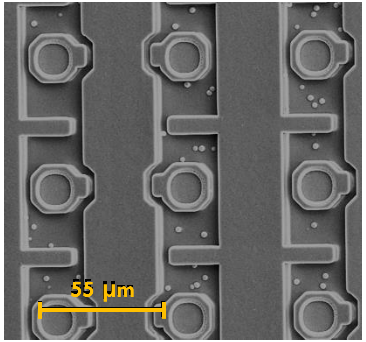
µ-particle bonding with ACF

- **Timepix3** (**+ planar Si sensor**) as a test-vehicle for ACF bonding
  - **Widely** used read-out ASIC (HEP, medicine, space, education…)
  - 256 x 256 pixels; 14 x 14 mm^2; **55 µm** pixel pitch; **18 µm** wide pixel pads
  - 256×256 × 320 µm^2 ≈ 0.20 cm^2 → **61–163 kgf** of bonding force

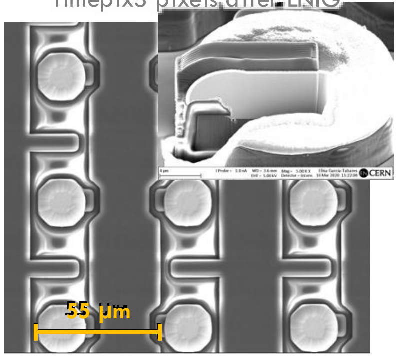
    (CLICpix2: 128×128 × 200 µm^2 ≈ 0.03 cm^2 → 9–24 kgf)



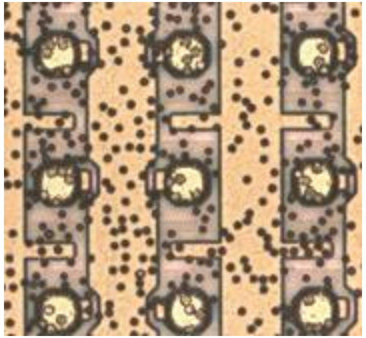
Bare Timepix3 pixel matrix



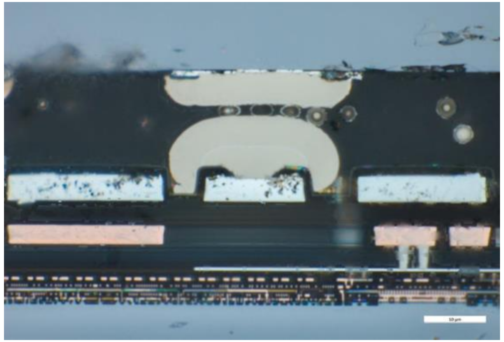
Timepix3 pixels after ENIG



Timepix3 with ACF laminated



TPX3 (bot) bonded to a Si sensor (top) w/ ACF



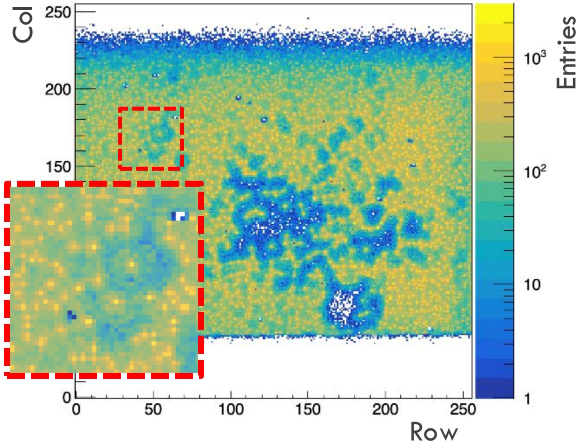
Timepix3 hybridization with ACF

First tests – Bonding tuning

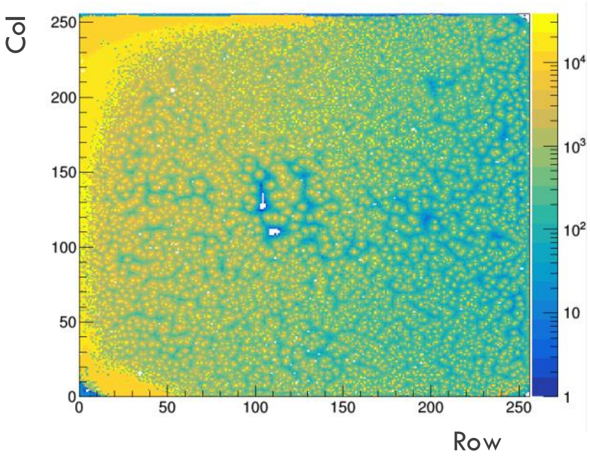
Timepix3 pixel matrix **fully covered** with ACF + default ENIG from PacTech ➔ Low connectivity yield (<20%)

- "Adjusted" bonding (same force, longer bonding) improved yield (but outside ACF specifications)
- 200 kg bonding force increased the yield, but a large area remains unconnected

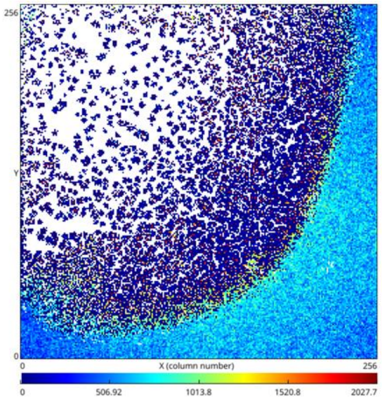
100% ACF coverage
100 kg bonding force
"Technical Data Sheet" (TDS) bonding



100% ACF coverage
100 kg bonding force
"Adjusted" bonding



100% ACF coverage
200 kg bonding force
"TDS" bonding



Timepix3 hybridization with ACF

First tests – Bonding tuning

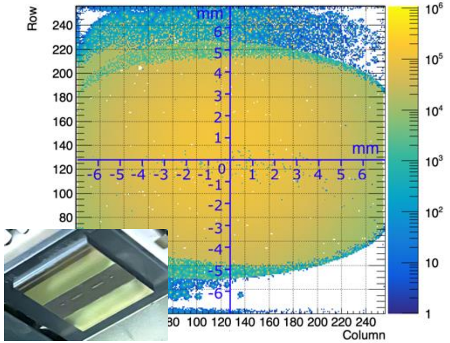
Changing the bonded area, we can achieve higher bonding pressure

- ☐ Sample covering **~30%** of the matrix ➔ **Uniform** and **high yield** connectivity
- ☐ sample with **~50%** coverage ➔ **Large area** with **good connectivity,** low yield in the central region

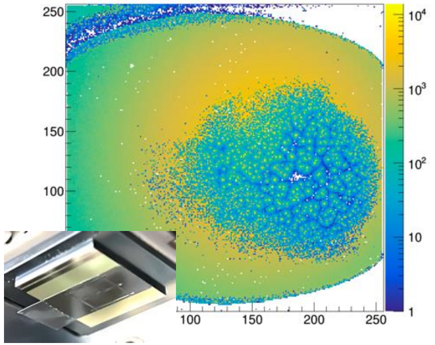
Proof-of-concept achieved: Successful pixel matrix bonding of **up to 1 cm^2** (so far)

Samples produced with ACF strips (different vendor) to test different possibilities (not very scalable…)

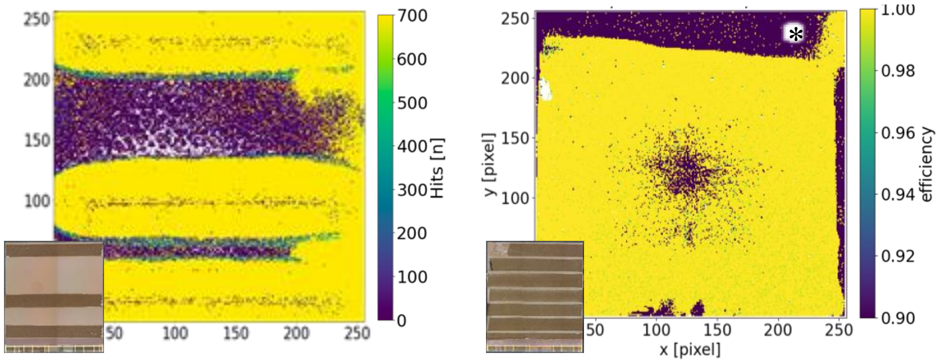
30% ACF coverage
100 kg bonding force



50% ACF coverage
100 kg bonding force



Pixel matrix coverage tests with multiple ACF strips



*plating issues on corners

Timepix3 hybridization with ACF

Interface optimization

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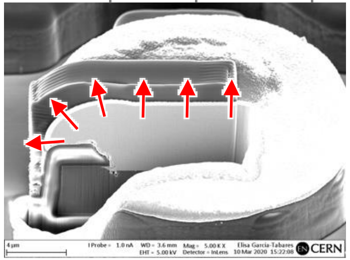
The pad was re-worked to grow taller and pierce through the adhesive film thickness

- Pad isotropic growth: +10 µm in diameter and +5 µm in height
  - Source measurement and cross-section inspection show a bonding improvement

Next: We will try a **new thinner film.** 9 µm thick (vs current 18 µm thick)

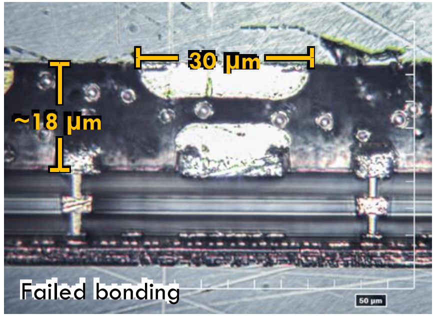
- The new ACF requires 20 MPa for bonding (vs current 30-80 MPa)

Timepix3 chip ENEPIG pad

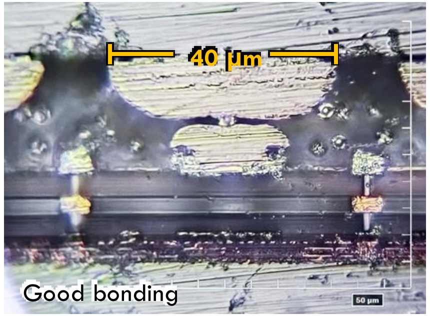


Timepix3 sensor after re-work

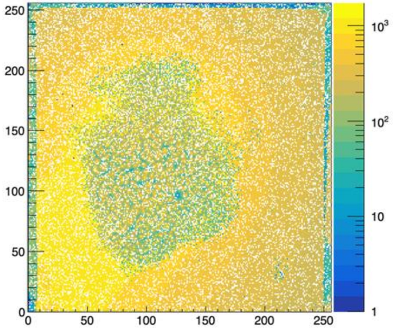
Timepix3 assembly w/ original ENEPIG



Timepix3 assembly w/ re-worked pad



100% ACF coverage
100 kg bonding force

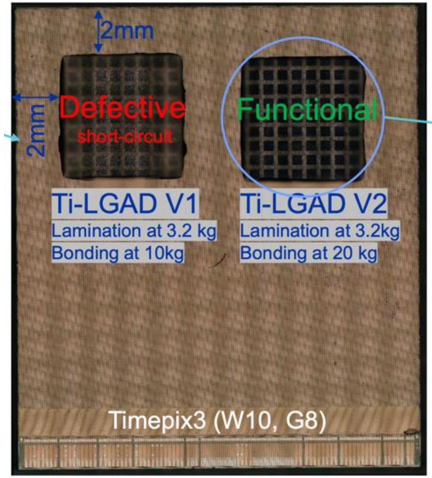


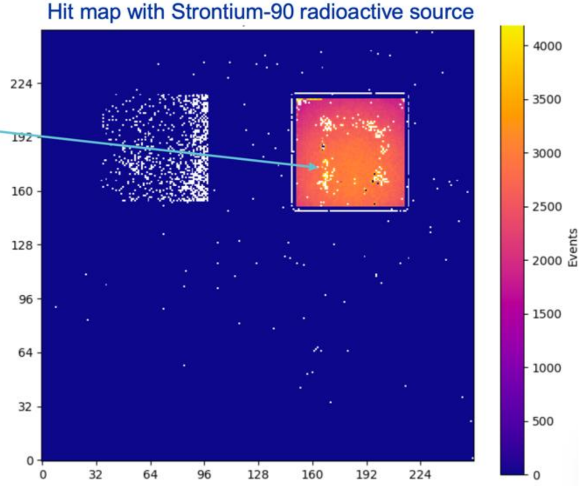
Small area hybridization with ACF

Resulting assemblies

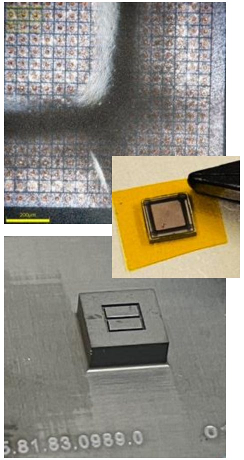
Smaller bonding areas are easier for bonding, but challenges are always present

- ☐ Visible imprint of the vacuum tool on laminated ACF, pushing out CPs during bonding
- ☐ 85-95% bonding yield consistently achieved for small devices < 1cm^2

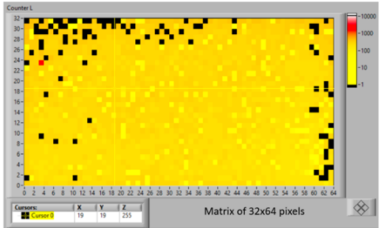




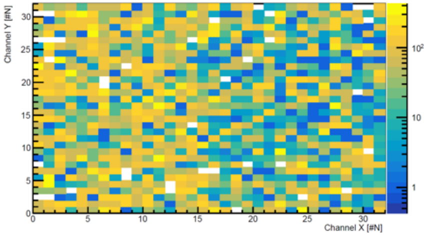
Vacuum imprint



~90% yield



SPHIRD



TimeSPOT

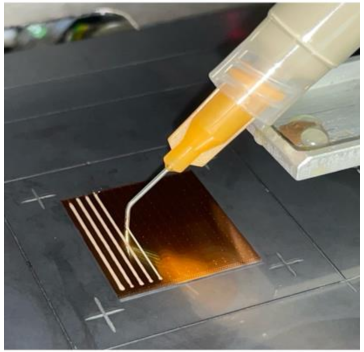
Hybridization with ACP

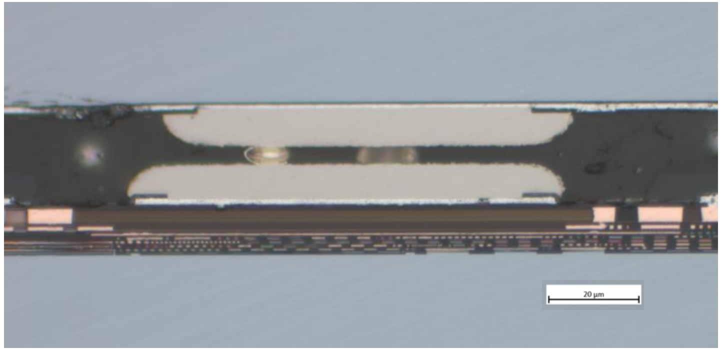
Paste format allows the use of a preferred adhesive, such as Araldite 2011, mixed with conductive particles

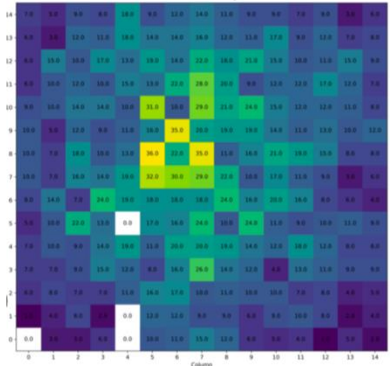
- Faster purchase of CPs, compared with ACF
- Avoid the short shelf life of ACF. No ACF lamination step.

- **ALTIROC ASICs** and **LGAD sensors** from ATLAS High-Granularity Timing Detector (HGTD)
  - **99% bonding yield** achieved over multiple samples


ACP mixing


ACP dispensing


Hybrid ACP cross-section


Pixel hit map

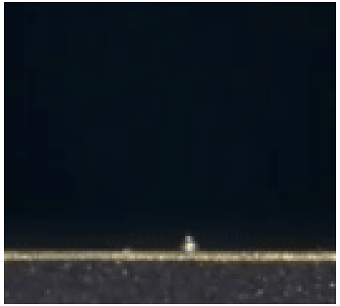
Hybridization with NCP and Au studs

For hybridization with NCP, the CPs are replaced by Au studs via Stud Bump Bonding (SBB)

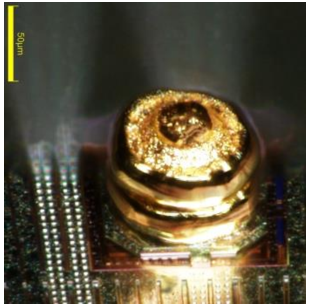
- ☐ Easier process than buying and mixing the conductive particles
- ☐ Double Au studs can be used (if a larger gap between devices is needed)
- ☐ The NCP can be chosen to allow the adhesive to cure at different temperatures/speeds

- ☐ <u>Only viable alternative for radiation-hardness qualification of LGAD sensors (60°C bonding for controlled annealing)</u>

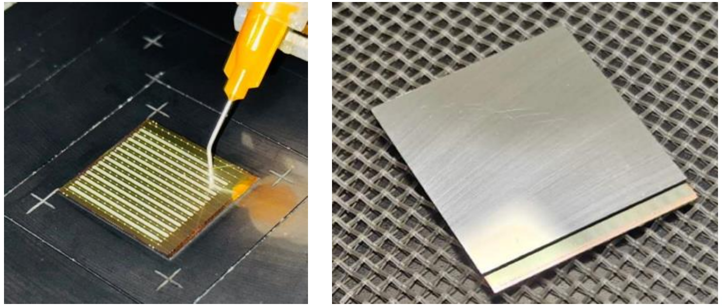
Gold Stud Bump Bonding (SBB)



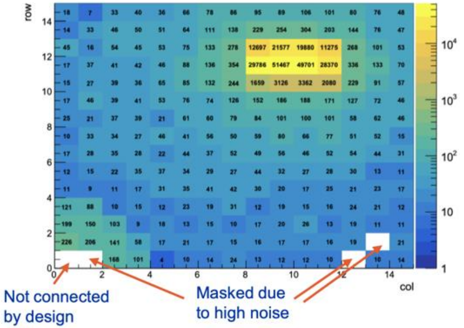
Double Au studs



NCP dispensing and thermocompression

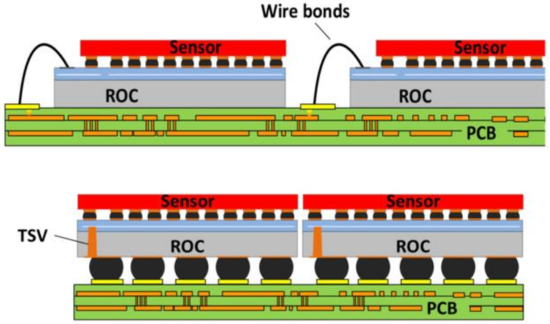


Test-beam occupancy map of ALTIROC with double gold studs + irradiated LGAD sensor



Beyond ACF and Hybridization

Through-Silicon-Via (TSV) integration



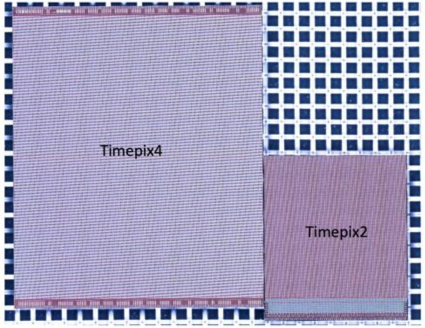
The TSV enables connections of I/Os from the top to the bottom of the ASIC

The Redistribution Layer (RDL) routes the TSVs to pads on the ASIC's bottom surface

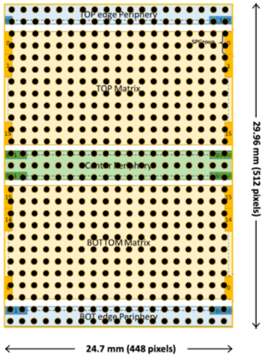
The **Timepix4** (512x448 pixels 55 µm pitch, ~7 cm2) has TSVs in 3 regions

- 3D integration with seamless 4-side tiles (no wire-bonds, minimal dead space)
- Better power distribution + Improved signal integrity

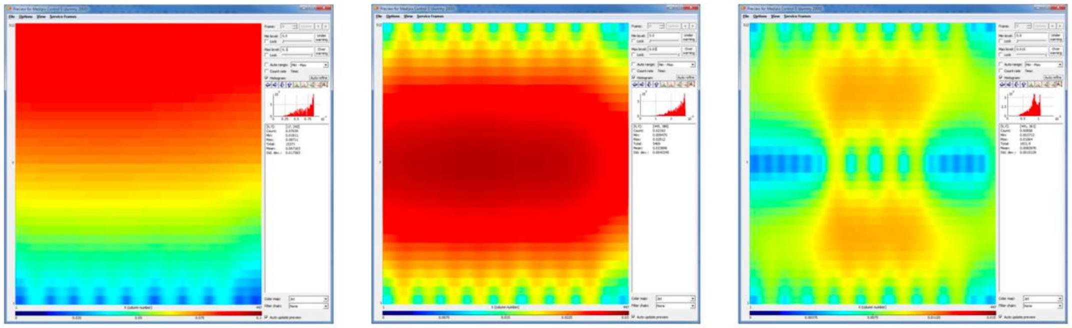
Timepix4 (and Timepix2 for comparison)



TSV regions and RDL



Timepix4 power drop simulations. Wire-bond (left), 2 wire-bonds (center) and 3 TSV regions (right)

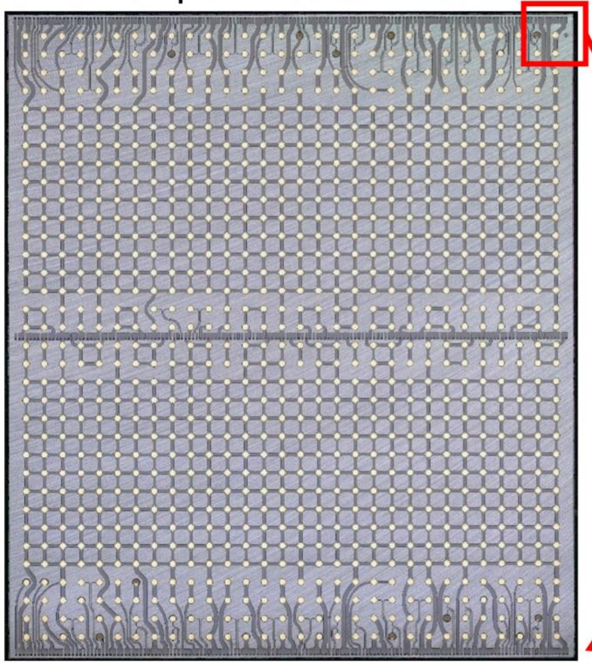


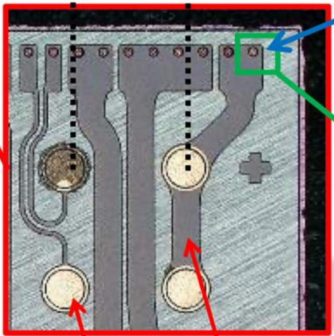
1 WB 2 WB 3 TSV

Beyond ACF and Hybridization

Through-Silicon-Via (TSV) integration

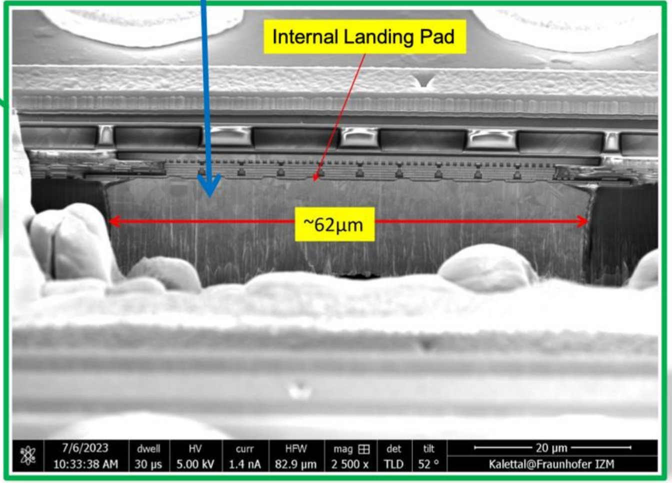
TIMEPIX4 TSV-Processed Back side
Chip thinned to ~120um





0.8mm pitch

Through Silicon Via (TSV)



x1020 BGA Pad
Diameter: 300 um

Redistribution Layer (RDL)

TSV cross section under SEM (Fraunhofer IZM)

The bondpads are diced out: 4 side buttability

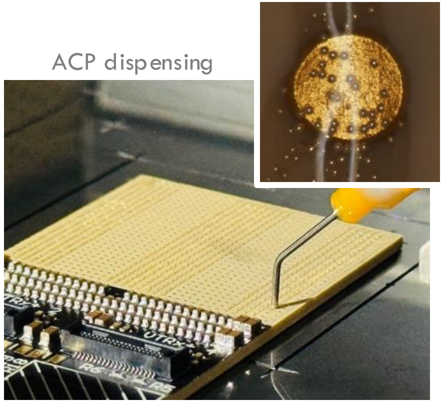
Beyond ACF and Hybridization

Through-Silicon-Via (TSV) integration

ACP bonding between RDL pads (Au coated) and ENEPIG pads from PCB (no post-process needed!)

- ☐ Data transmission is proven at gigabit rates. The eye diagram shows that the TSVs are powering the chip and delivering a good signal even at **10.24 Gbps**

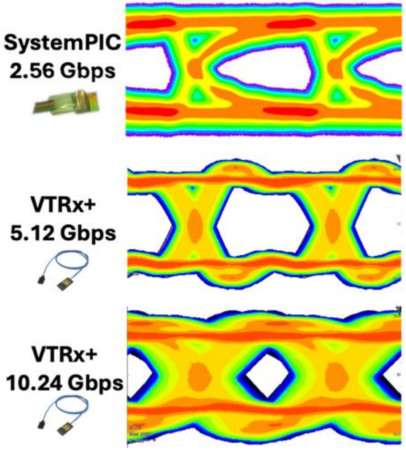
ACP dispensing



Timepix4 RDL pads

Thermocompression bonding

Eye Diagrams Through Optical Fiber



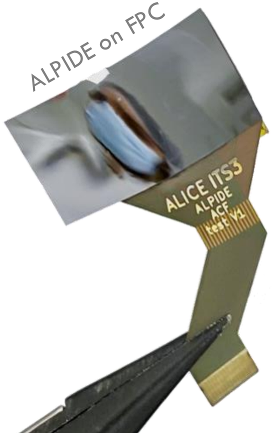
Assembled chip on "finger board"

Other detector integration with ACA/NCA/SBB

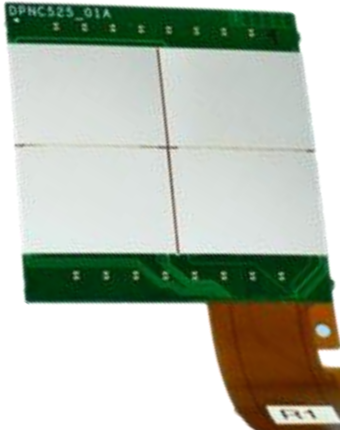
ACF is also suitable for **module integration** with ASIC-PCB/FPC assembly, **alternative** to wire bonding/BGA

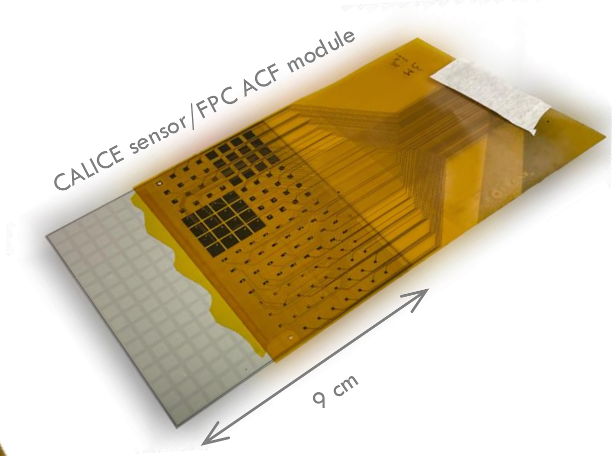
- **Ultra-low-mass** multi-chip module with the **MALTA2** pixel detector (EP-R&D, CERN)
- 50-µm thin **ALPIDE** integration to a **flexible printed circuit** (FPC) (ALICE ITS, CERN)
- **Stackable** multi-chip **MAPS module** for PET scanners (**100µPET**, UNIGE)
- **Large area** Si-sensor/FPC bonding for calorimeters (**LUXE**, DESY)


MALTA2 on FPC


ALPIDE on FPC

100µPET ASICs on FPC




CALICE sensor/FPC ACF module

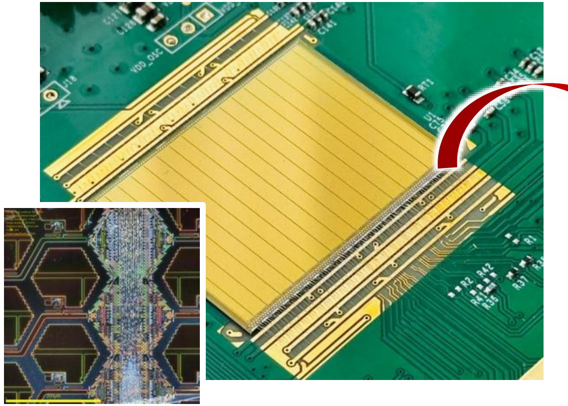
The 100μPET scanner

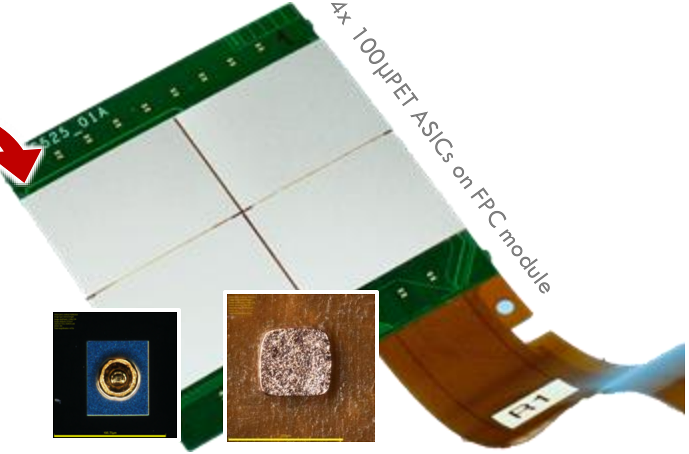
ASIC, module/layer, tower

Multi-layer stack of CMOS imaging sensors for ultra-high resolution PET imaging

- **100μPET** MAPS: **130 nm** SiGe BiCMOS; **2.3 x 3 cm^2**; **150 μm** pixel pitch; **270 μm** thick; **~0.1 W/cm2**
- Single silicon detection layer composed by **2x2 ASICs** flip-chip to a flex printed circuit, covering **24 cm^2**
- Flip-chip integration tested with ENIG+ACA and SBB+NCP

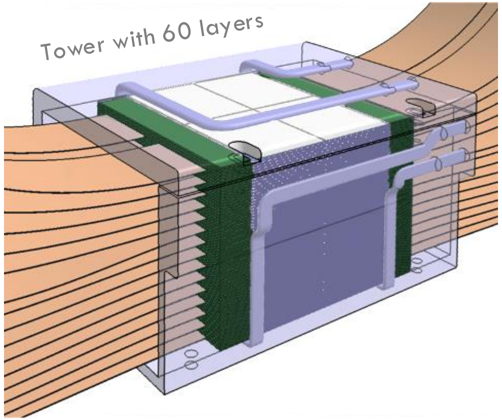
100μPET ASIC on single-chip board





4x 100μPET ASICs on FPC module

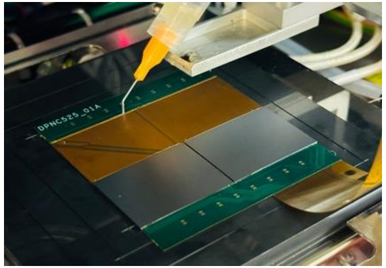
Tower with 60 layers

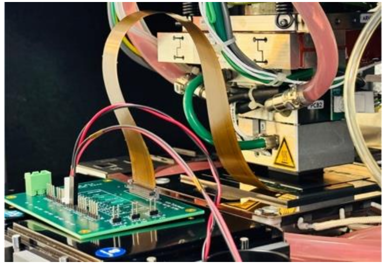


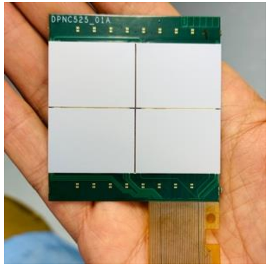
100μPET module demonstrator

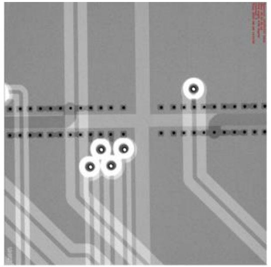
Reference module

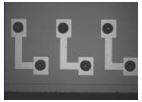
- ☐ Bond resistance of <u>**~10 mOhm**</u> and uniform over module's 4 corners and center
- ☐ Chains of pads indicating no open connection in ~1000 pads (**bonding yield >99.9%**)
- ☐ Heater system is working as expected, with <u>8°C</u> increase in temperature at <u>nominal module power (2W)</u>

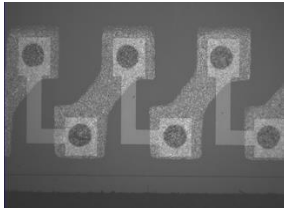


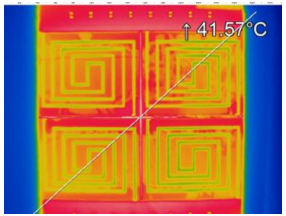












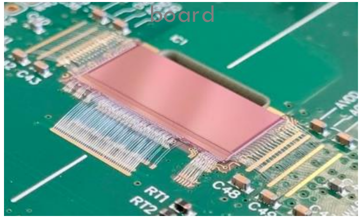
Novel Low-Mass Detector Module Flex

Flexible, low material, dense and reliable modules with the MALTA2 ASICs

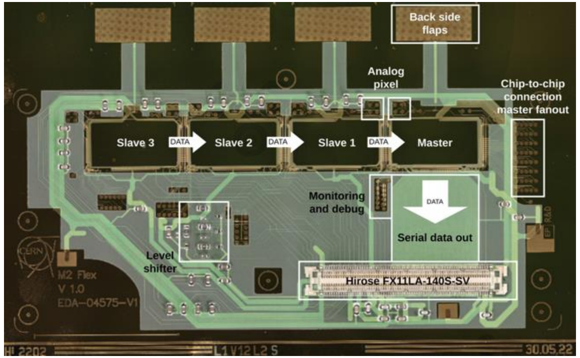
- Two-layer flex, **~30 µm thick** with **17 µm trace** width and spacing
- Individual powering with **500 mA** per chip
- Chip-to-chip data transfer

Successfull connection using ENIG+ACF/ACP and SBB+NCP

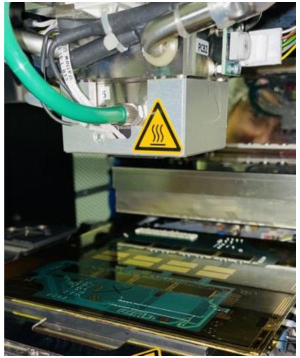
MALTA2 on a single-chip board



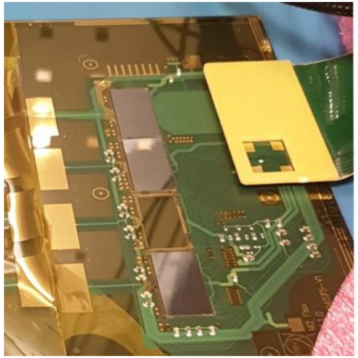
MALTA2 multi-chip flex circuit



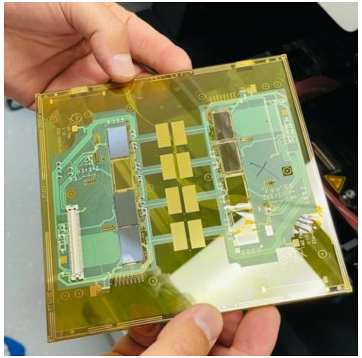
Flip-chip bonding



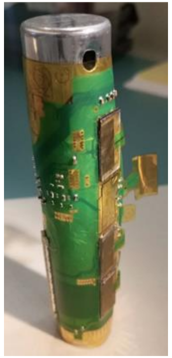
Testing bonded chips



Populated flex on support material



Flex removed from support

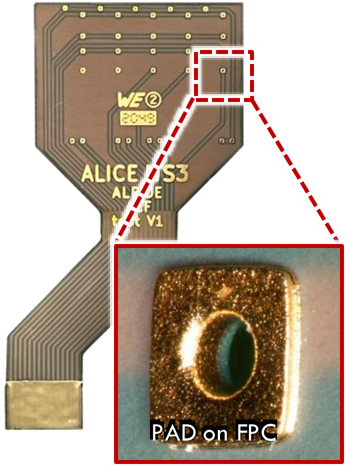


ALPIDE ACF bonding tests

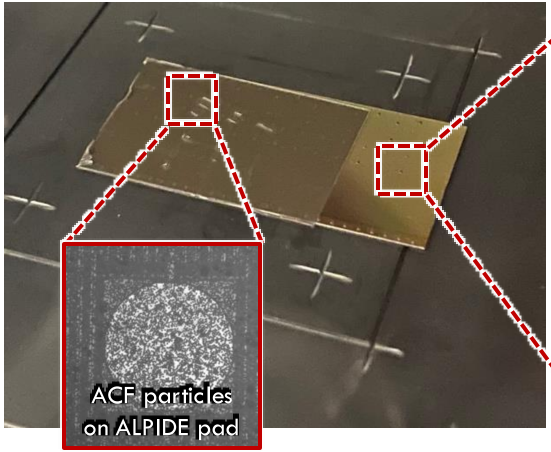
ALPIDE flex, ENIG and bonding

- **FPC** designed for the ACF bonding for ASIC integration
- ENEPIG on FPC and **In-house ENIG** plating on the ALPIDE chip for higher bonding pads
- Bonding done with **ACF** with up to <u>100 kgf</u>

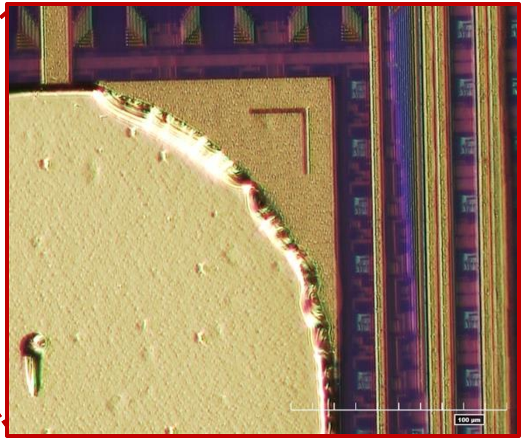
ALPIDE flex V1



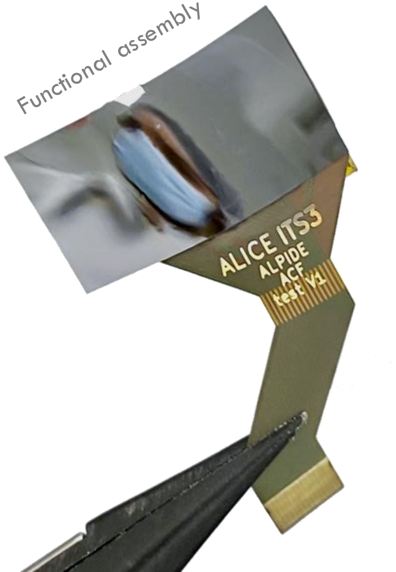
ALPIDE with ACF (partially) laminated



ENIG grown on ALPIDE interface pad



Functional assembly

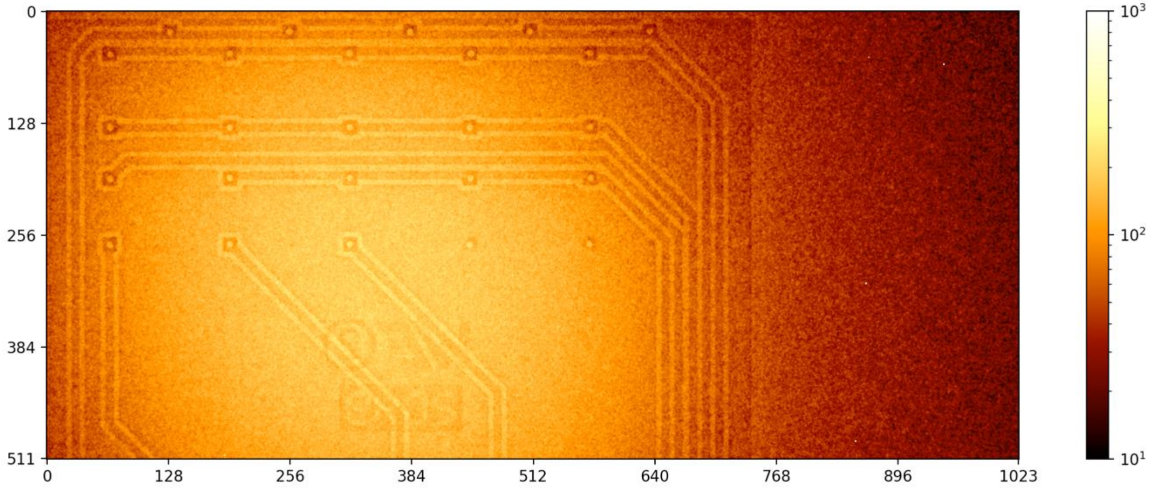


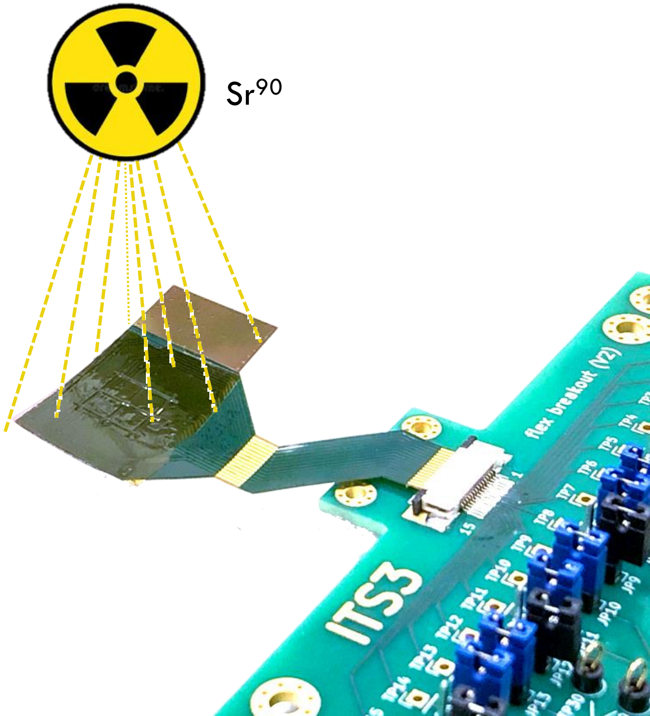
ALPIDE ACF bonding tests

Sr^{90} illumination test and next steps

- ☐ <u>Good interconnection between ALPIDE and FPC using ACF</u>
  - Very good electrical contact. **<1 Ohm** contact resistance. <u>Nominal power consumption</u>

ALPIDE hit-map with FPC shadow (1000s 1M events)





Conclusions

- ☐ We don’t need to rely only on solder bump-bonding hybridization
  - Small and large devices are being hybridized with ENIG+ACA and SBB+NCP
  - Large devices with a high-density pixel matrix (Timepix-like) are still work-in-progress
- ☐ Multiple packaging techniques can be combined and implemented
  - The ENIG and Au stud bumping, combined with adhesive bonding, brings flexible techniques suitable for detectors with mixed assembly needs
  - This allows for new architectures of pixel detectors to be envisioned