



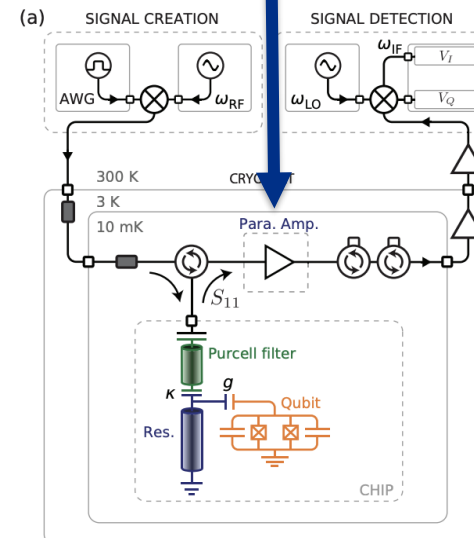
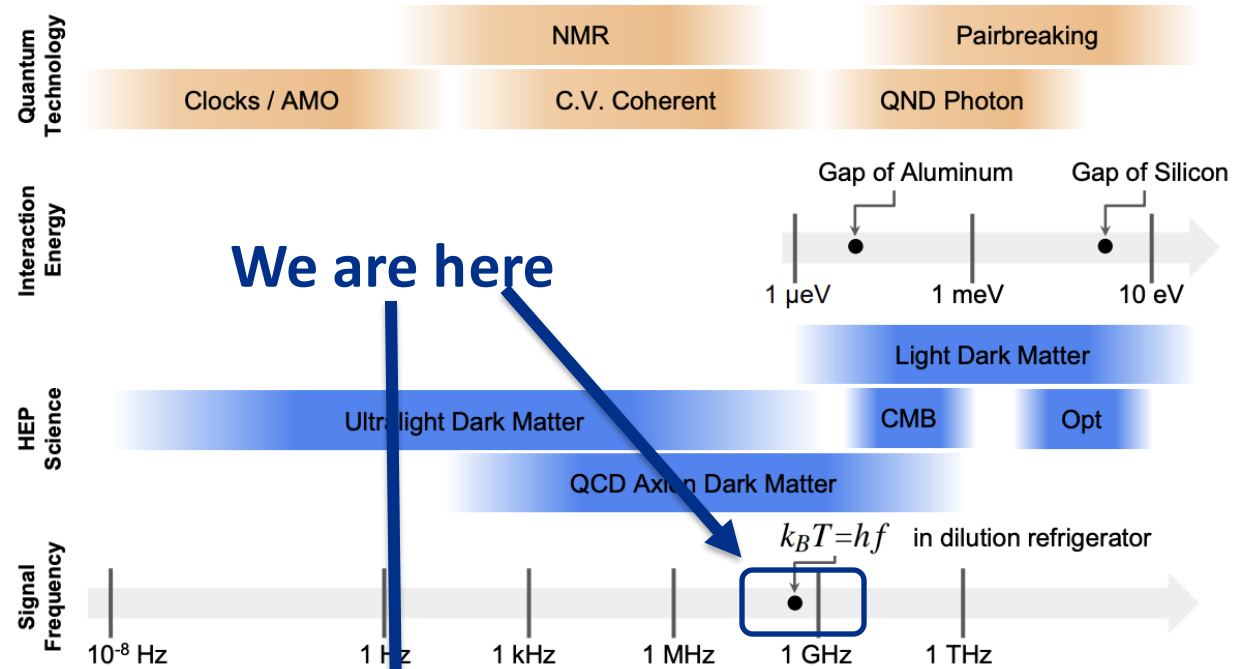
# Superconducting Parametric Amplifier Design

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# Why Parametric Amplifiers

- Experiments in HEP and QIS
- Cryogenic temperature operation
- High Quantum Efficiency
- General Purposed Quantum readout chains



Source: A Quantum Engineer's Guide to Superconducting Qubits arXiv:1904.06560

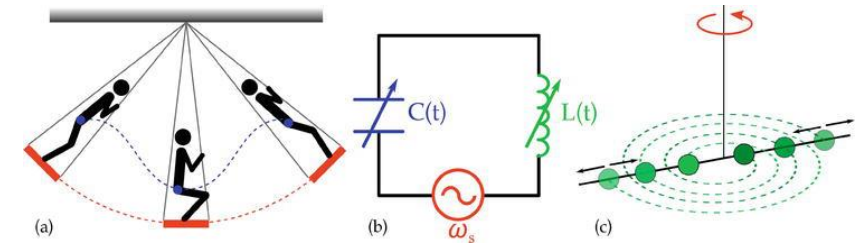


# Parametric Amplifiers At Fermilab

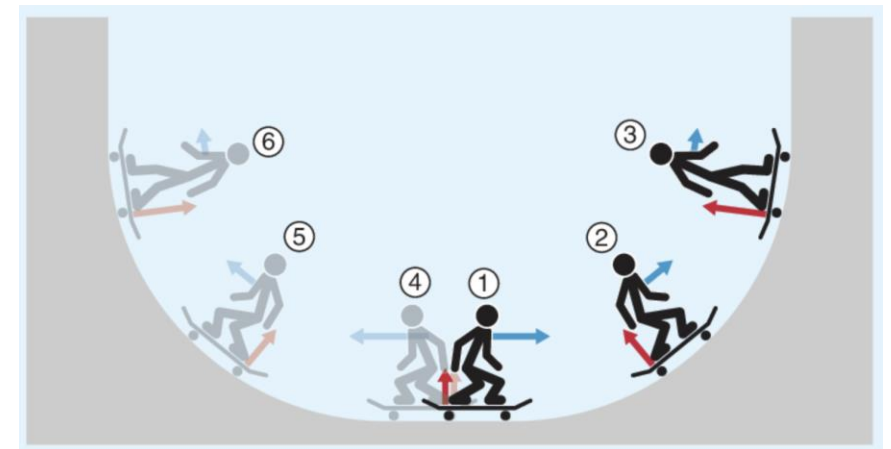
- Tape-out: March of 2023
- Fab: MIT-LL SFQ5ee [100  $\mu\text{A}/\mu\text{m}^2$ ; 8 Nb Layers]
  - Established and matured superconducting JJ process
  - Repeatable and well controlled for ASIC applications
  - Frequent MPW runs
- Chip Contents
  - 2 JPA experiments
  - 2 JTWPA experiments
  - Test Structures

# What is a Parametric Amplifier?

- RF Mixer combined with amplifier
- Parametric refers to the process of modulating a parameter of a system of equations
- Signal tone is mixed with pump tone via non-linearity
- Energy from pump is converted into signal photons
- Akin to being pushed on a swing or skating in a half pipe



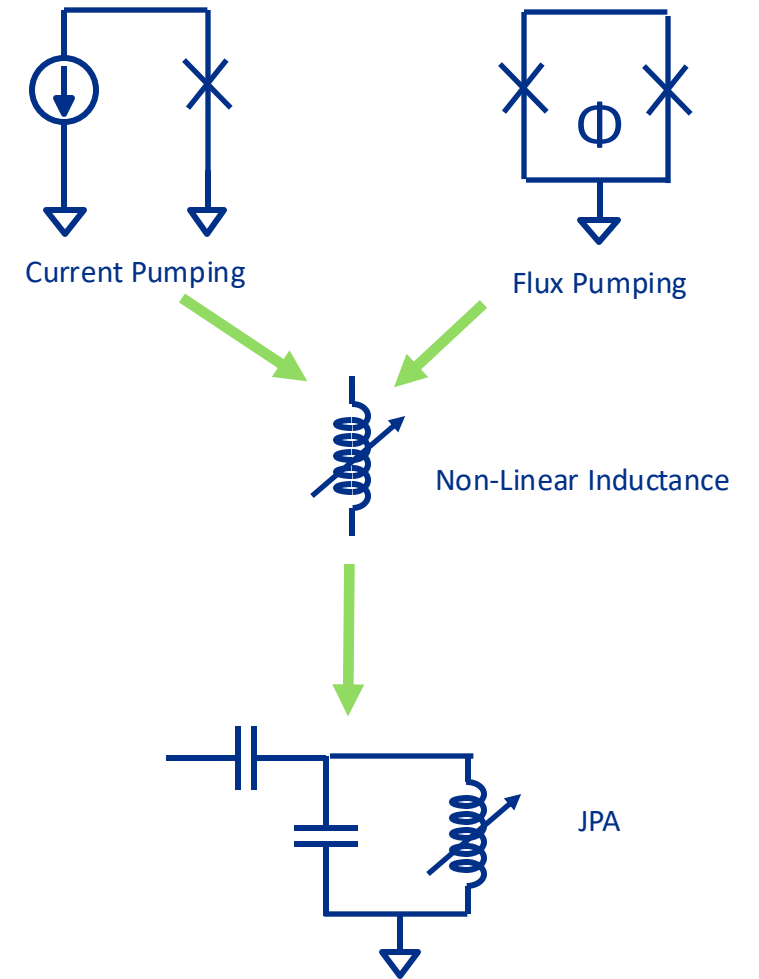
Source: Superconducting Josephson-Based Metamaterials for Quantum-Limited Parametric Amplification: A Review



Source: Superconducting Parametric Amplifiers: The State of the Art in Josephson Parametric Amplifiers  
DOI: [10.1109/MMM.2020.2993476](https://doi.org/10.1109/MMM.2020.2993476)

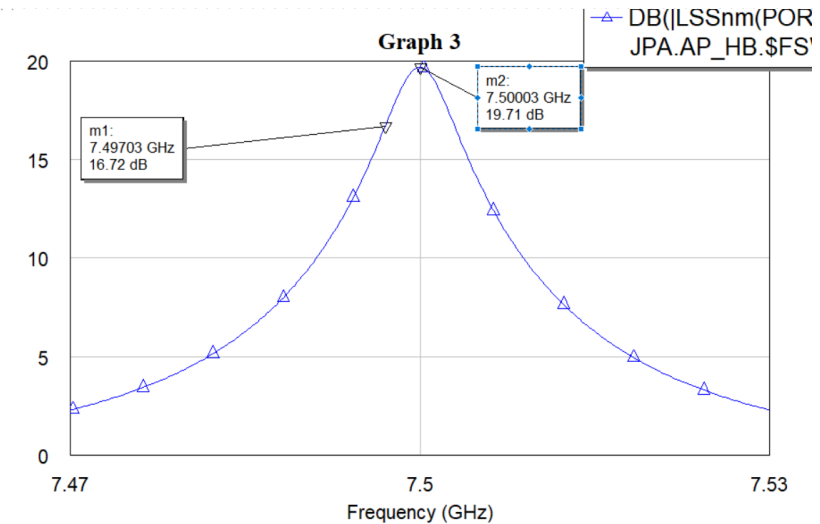
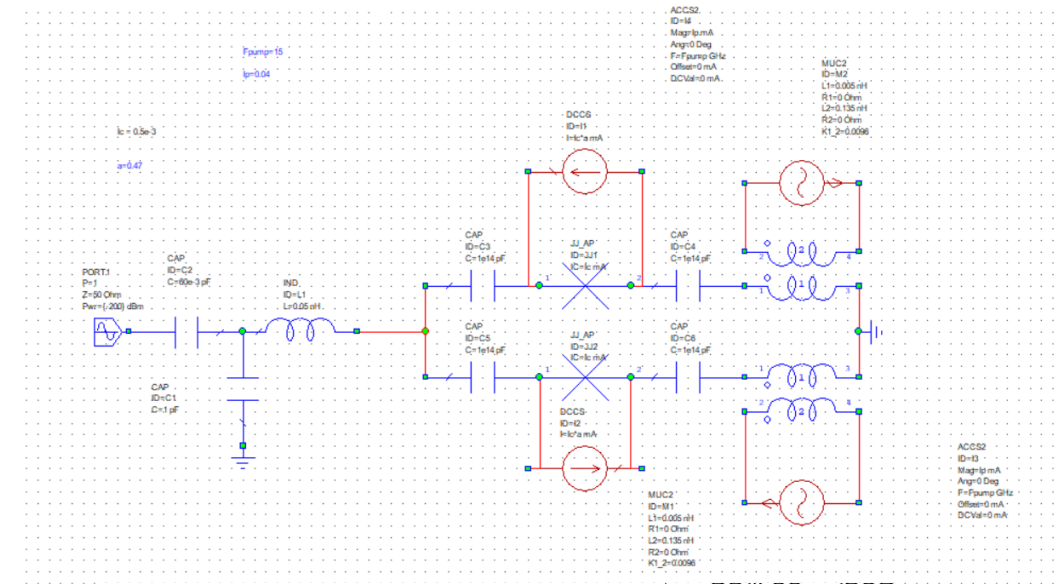
# Josephson Parametric Amplifier

- Increasing current through JJ increases the effective inductance
- Single JJ/JJ Chain = Current Pumping via modulation of the Josephson Inductance
- DC SQUID = Flux Pumping via modulation of the effective  $I_c$  of the SQUID
- 1 Port System
- Active termination
- Very small bandwidths



# JPA Circuit Simulation

- 2 different versions of JPA
  - Crossed loop (0-effective area)
  - No-crossed loop
- Original design adapted from original work by WashU collaborators
  - ADMX and BREAD
- Specifications
  - Coupling capacitance = 60fF
  - Signal Frequency = 7.5 GHz
  - Pump frequency = 15GHz
  - Pump Amplitude = 40uA
  - Gain = 20dB
  - Bandwidth = 60MHz
  - Tunable Bandwidth = <1GHz



Original Theory/Designs

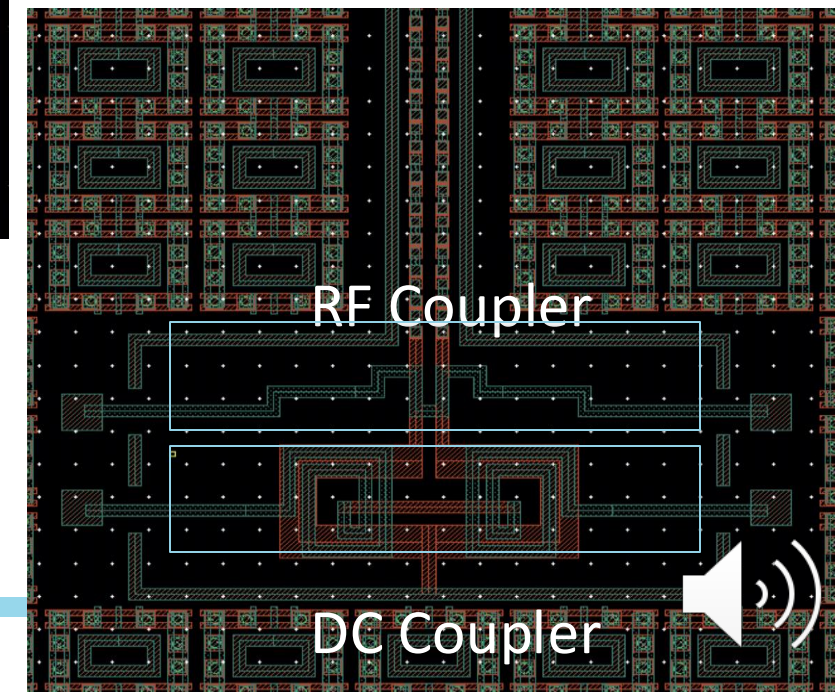
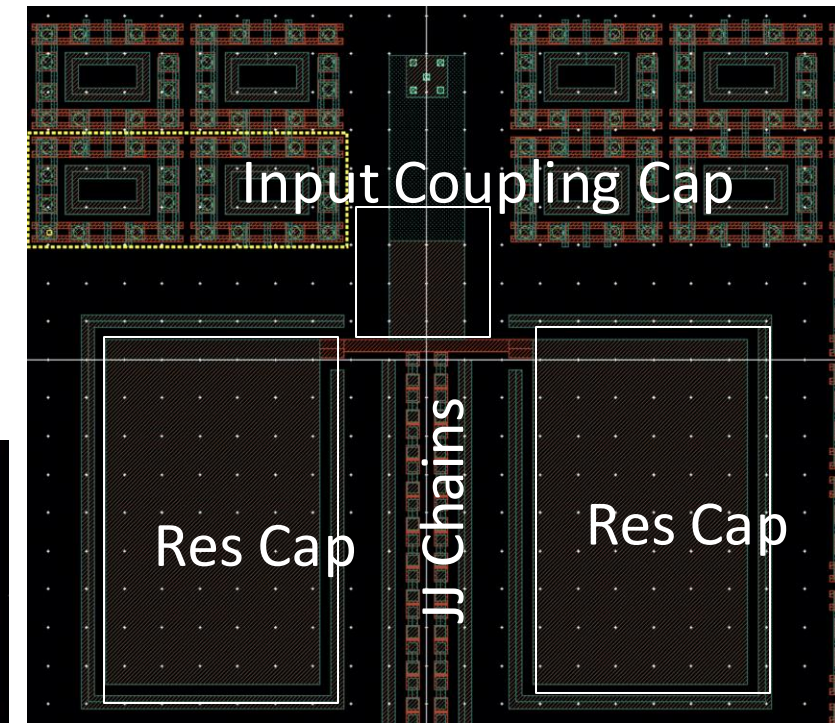
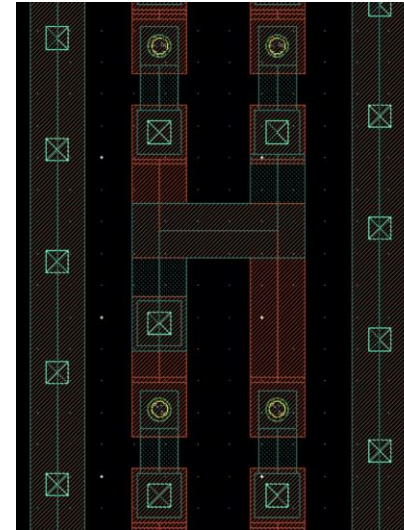
<https://arxiv.org/pdf/0808.1386.pdf>

[https://www.epj-conferences.org/articles/epjconf/pdf/2019/03/epjconf\\_gtech2018\\_00008.pdf](https://www.epj-conferences.org/articles/epjconf/pdf/2019/03/epjconf_gtech2018_00008.pdf)



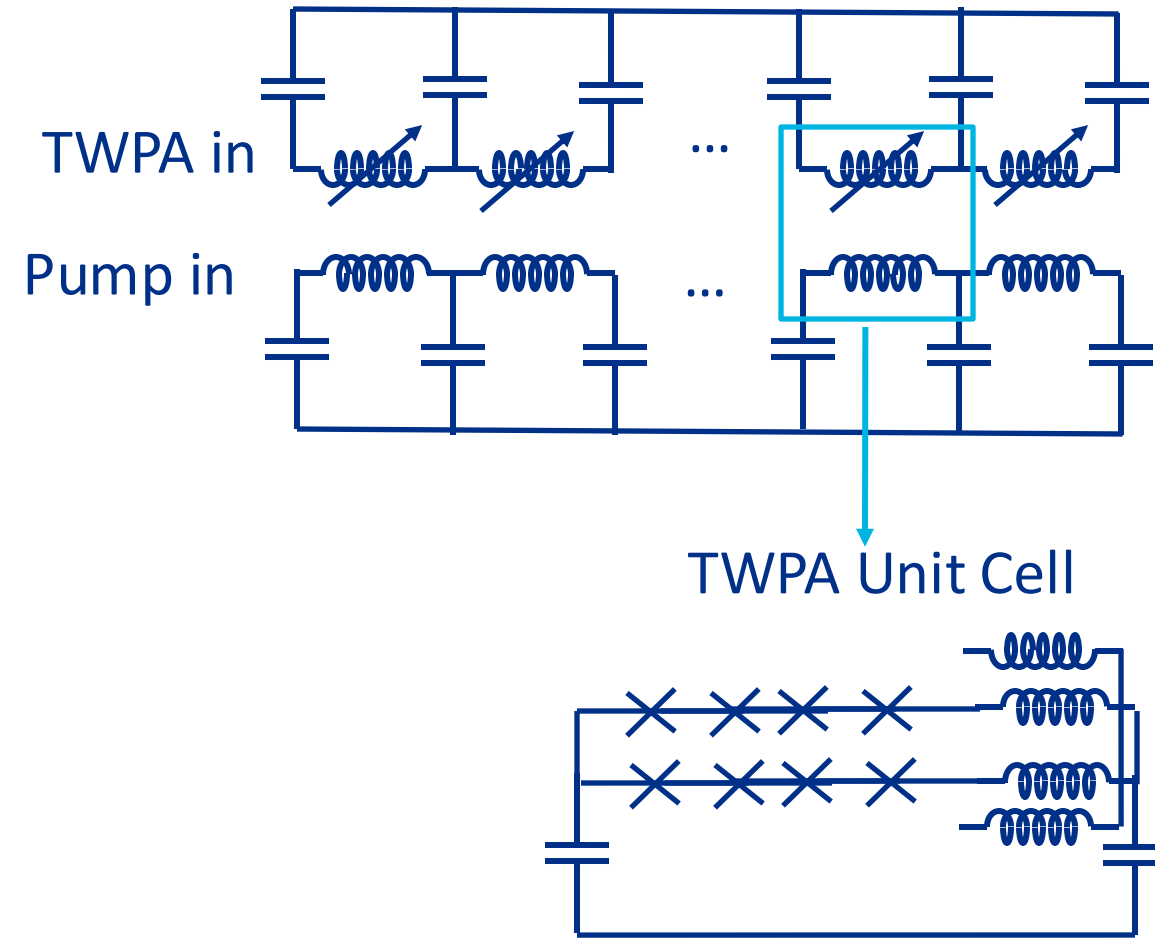
# JPA Circuit Layout

- SFQ5ee
- Original work was done with 1 layer
- RF Coupler = 0.5pH
- Minimizing capacitance between RF bias line and SQUID is essential for avoiding current pumping
- DC Coupler = 3pH



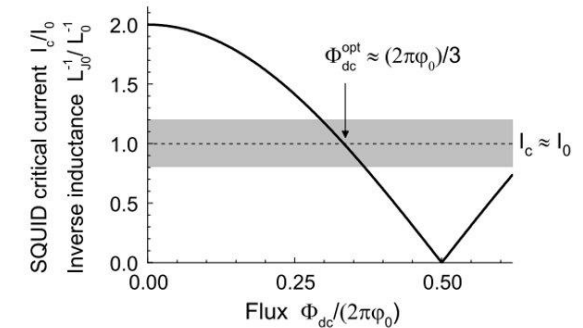
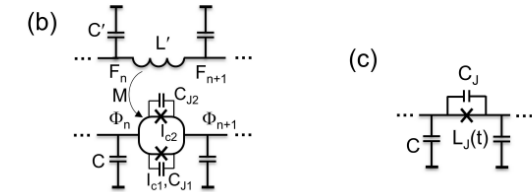
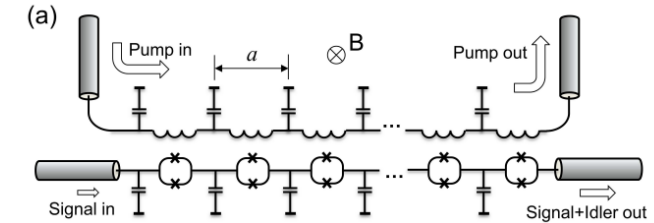
# What is a TWPA?

- AKA: JTWPA or Josephson Traveling Wave Parametric Amplifier
- A non-linear transmission line
- Phase matching (L-C's match)
- Current and Flux Pumping
- Much larger instantaneous bandwidth
- Floquet, SNAIL
- Theory first developed by Zorin 2019
- <https://arxiv.org/pdf/1804.09109.pdf>



# Dispersion Engineering

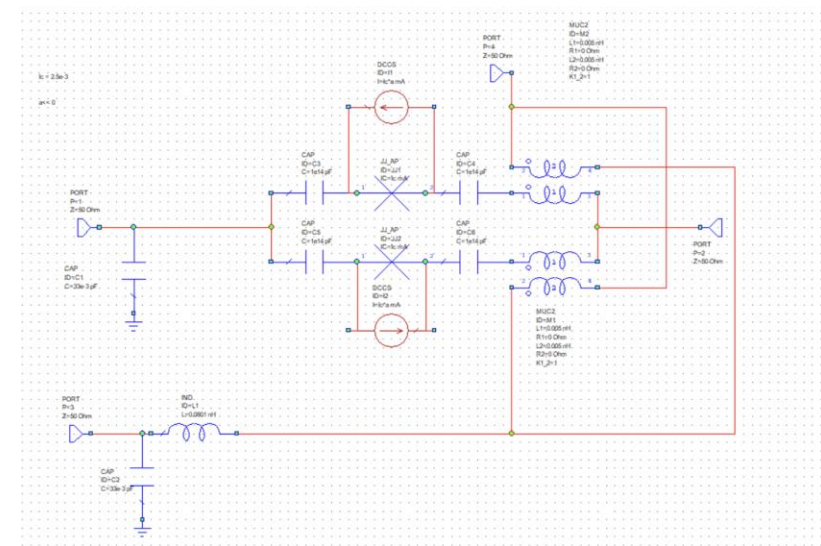
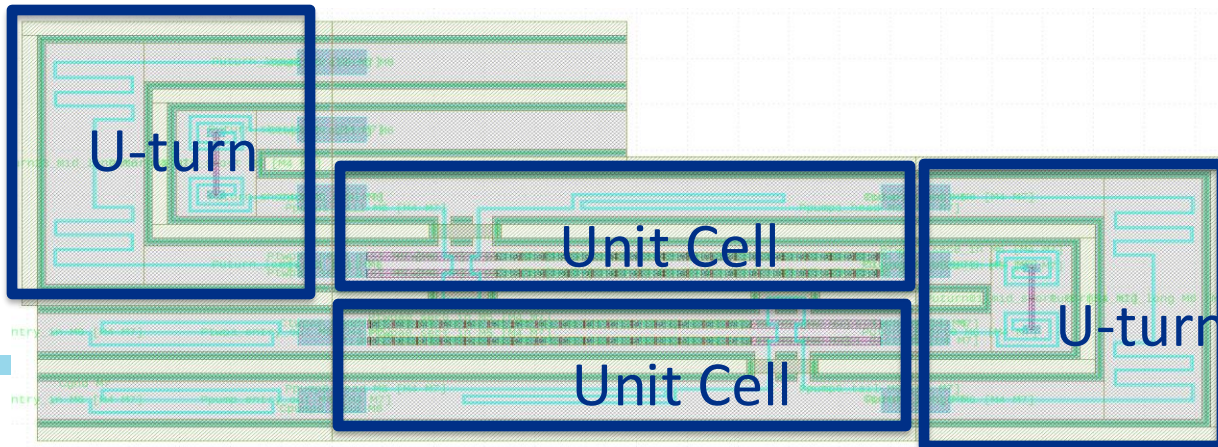
- Solutions
  - Introducing stop-bands
  - Varying size of JJ's along path
- Two parallel transmission lines
  - Pump Tone
  - Signal Tone
- Optimally bias TWPA for maximum slope of SQUID critical current



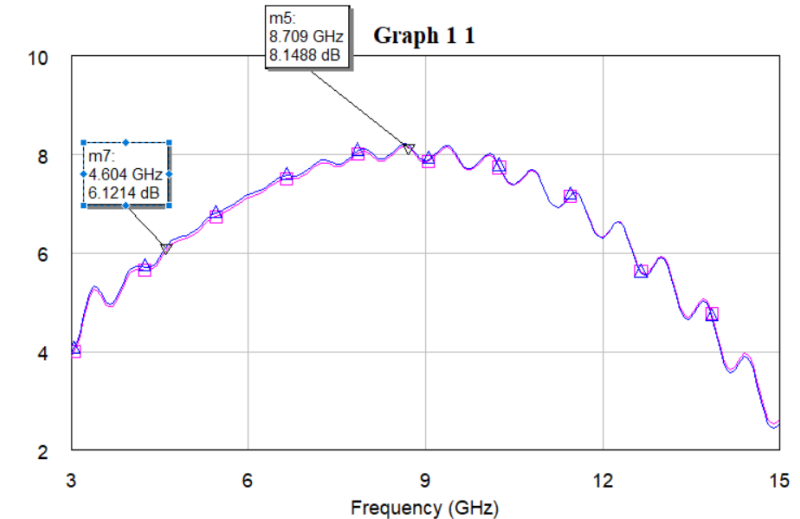
<https://arxiv.org/pdf/1804.09109.pdf>

# JTWPA Circuit Simulation

- 400x and 800x unit-cell experiments
- Dispersion/impedance engineering
  - Lumped element pump line matched to operating impedance of TWPA unit cells
- Specifications (400 unit cells)
  - Pump frequency = 20GHz
  - Pump Amplitude = 40uA
  - Gain = 8dB @ 9GHz
  - Bandwidth = 8GHz



Unit-cell Schematic



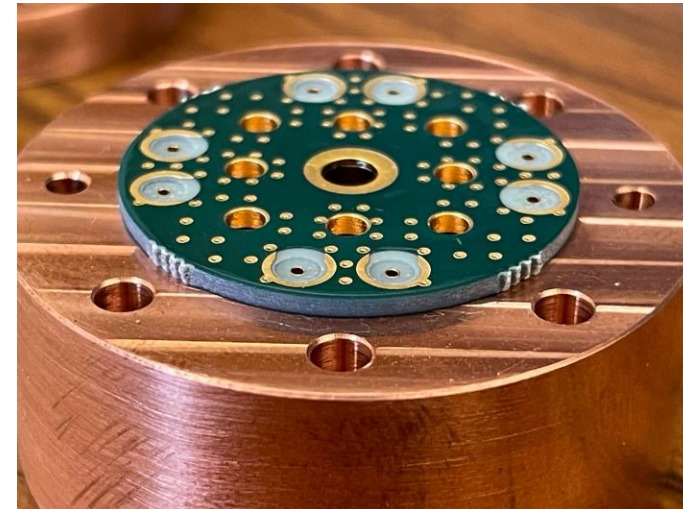
400 unit-cell Gain Simulation

# Cavity Design

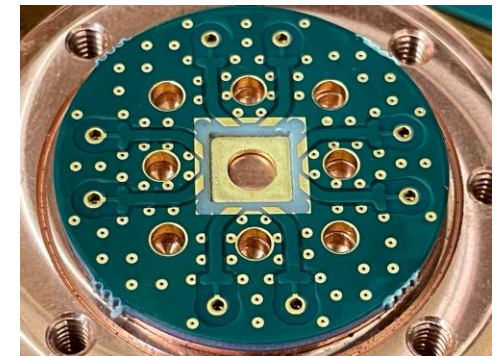
- Package modes need to be far away from amplification frequency
- Leakage is minimized at the frequency of interest.
- Flux pumping requires an inductive coupling between the flux line and the Squid chain. Pushing the cavity mode away reduces the capacitive coupling which might cause second order pumping instead of first order and can cause Kerr shift.



Left to Right: Bottom Cavity, DC Bobbin, Top Cavity



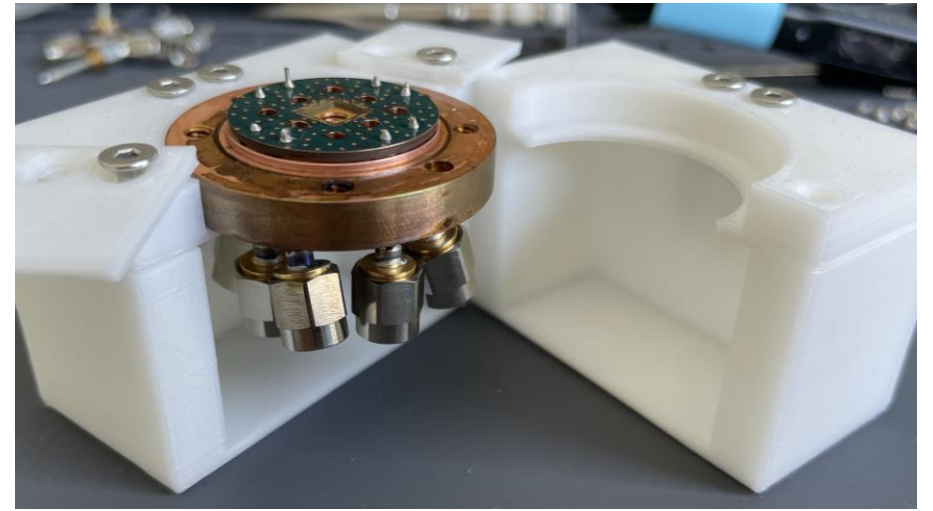
Bottom face of PCB



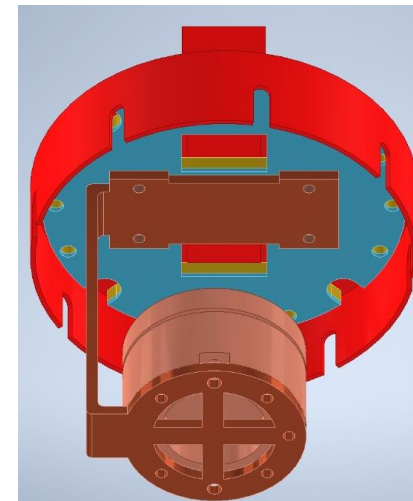
Top face of PCB

# Packaging and Assembly

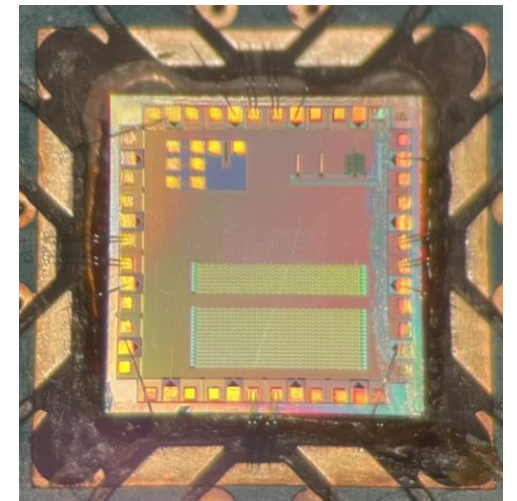
- Utilizing SiDet capabilities at Fermilab to wirebond chips to PCBs
- Working with LOUD facility at Fermilab to integrate JTWPA into existing test stands
- Mounting bracket machined to integrate the cavity into a test stand



3D-Printed Wirebonding Platform



Isometric view of mounting bracket



Wirebonded Chip

# Future Work

- 1000x and 2000x unit cells
- Mutually coupling RF clock phase as a dispersion matching technique which can increase tunable bandwidth
- Verify against open-sourced simulation tools
- Lower critical current density fabrication
  - Shrinks SQUID loops
  - Reduces the number of junctions required
  - Increases beta

