

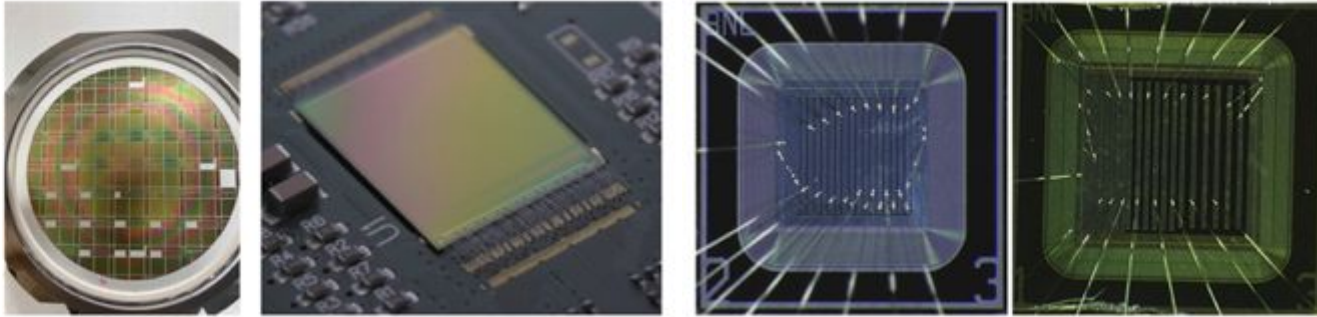


Sub-5ps Precision TDC ASIC in 22nm

Si Xie, Adam Quinn, Artur Apresyan, Cristian Pena, Davide Braga
CPAD Meeting 2024

Precision Timing Readout ASICs

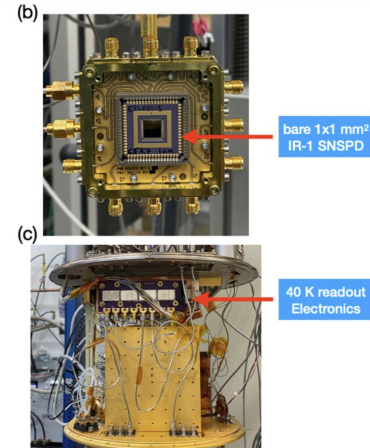
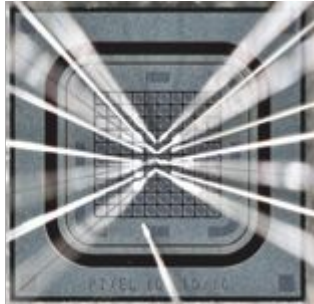
- Picosecond precision timing increasingly critical for detector systems in diverse areas of science:
 - Particle Physics, Metrology, Quantum Optics, etc.



- System **scalability** to large areas and large number of channels is key!
 - Integrated chips (ASICs) for readout of such detector systems without compromising timing precision remains a grand challenge.

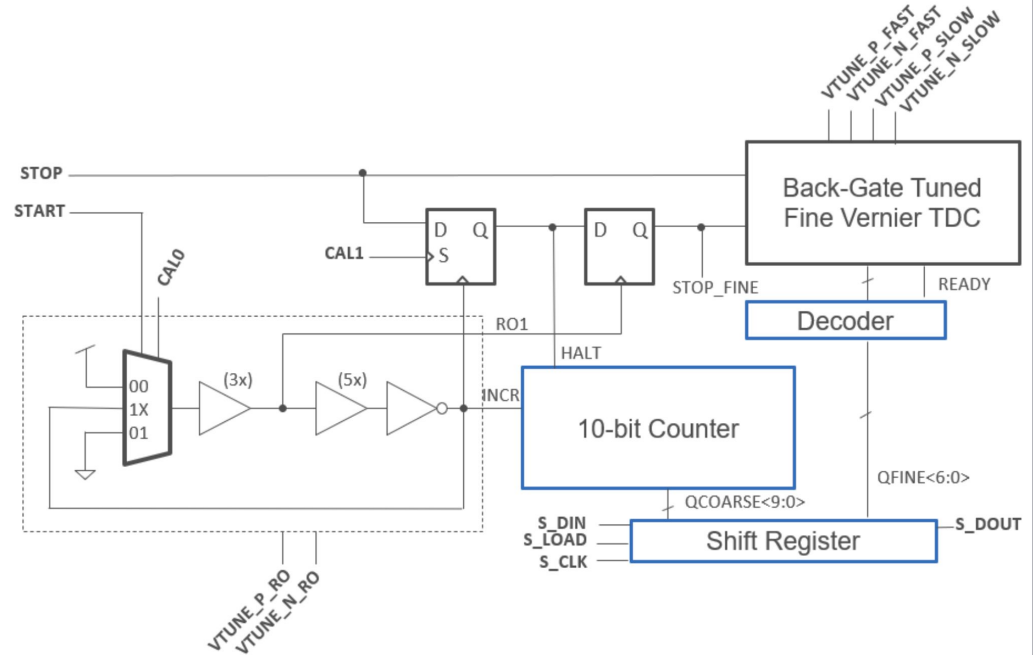
The DILVERT Time-to-Digital Converter (TDC) ASIC

- Design a versatile, compact, low-power TDC capable of handling both:
 - Harsh cryogenic detection environment, and
 - High granularity and scalability needed for particle tracking
 - Uses GlobalFoundries 22FDX platform (22nm technology)



DILVERT Architecture

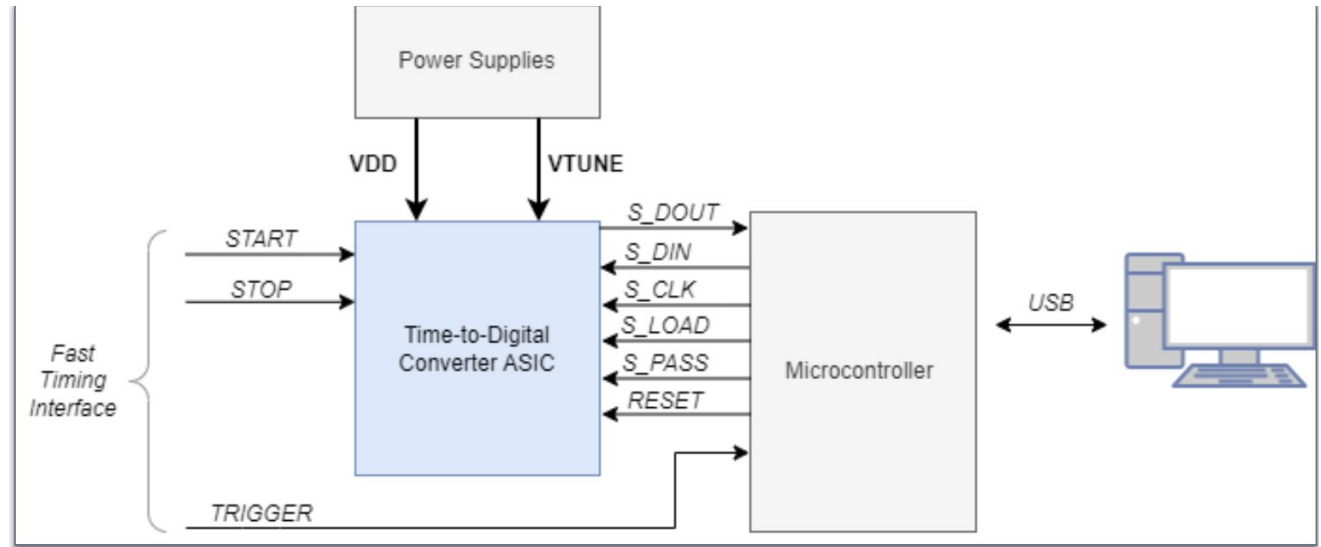
- Two-step architecture consisting of:
 - coarse (500ps) based on ring-oscillator
 - fine (5-9ps) based on linear Vernier delay line



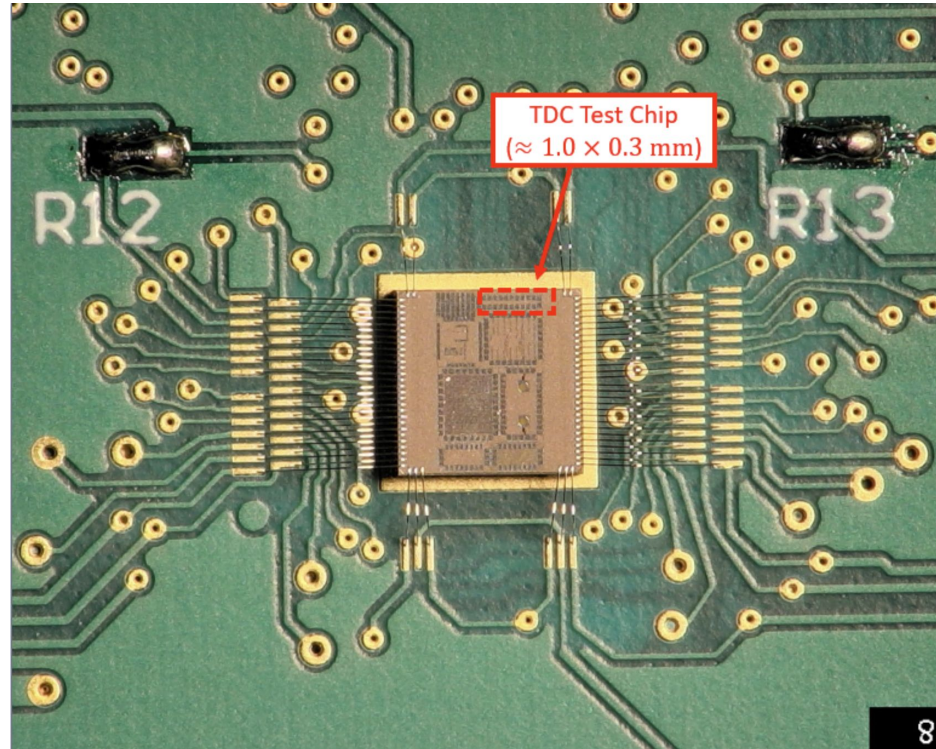
Readout & Control

- Test prototype uses Arduino microcontroller for control and readout
- Trigger signal initiates retrieval of measurement from ASIC to Arduino

- TDC operating parameters can be tuned via applied voltage to the ASIC



DILVERT Test Chip



ASIC Testing and Characterization

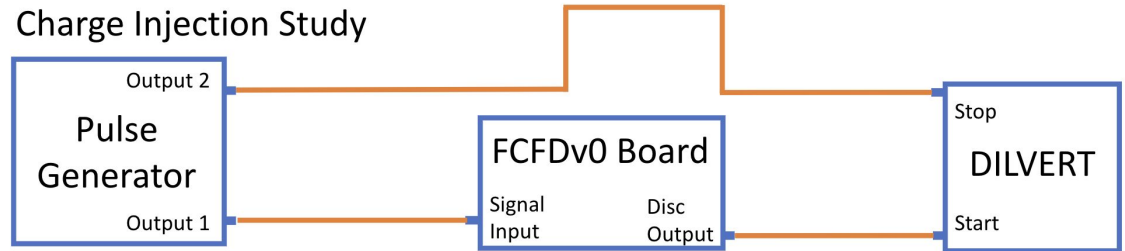
- Two Characterization measurements:

- Pulse generator Study
- LGAD-like signal injection Study

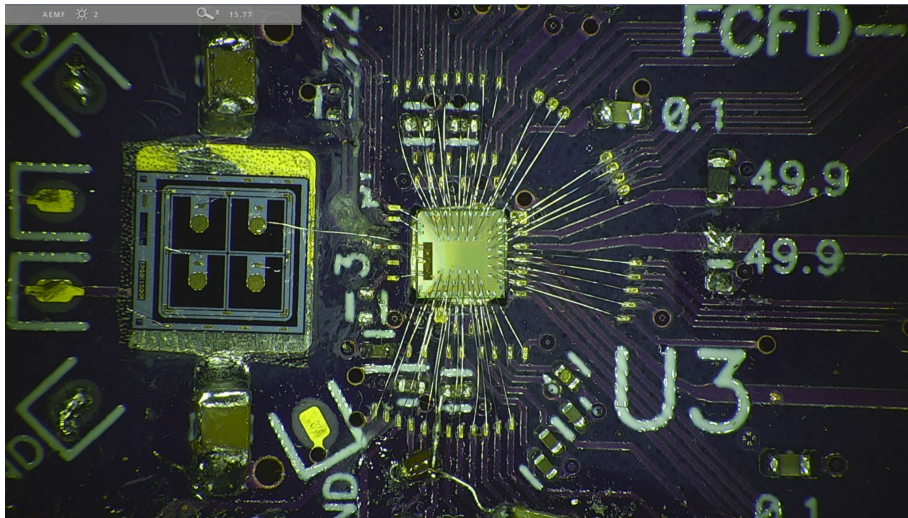
Pulse Generator Study



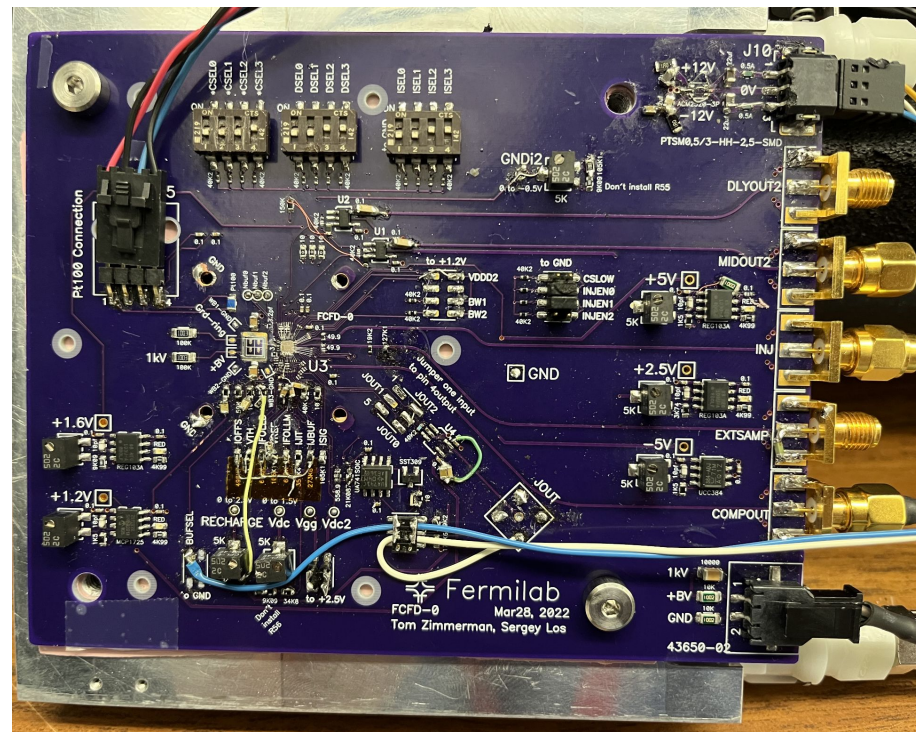
Charge Injection Study



Fermilab CFD ASIC & Test board

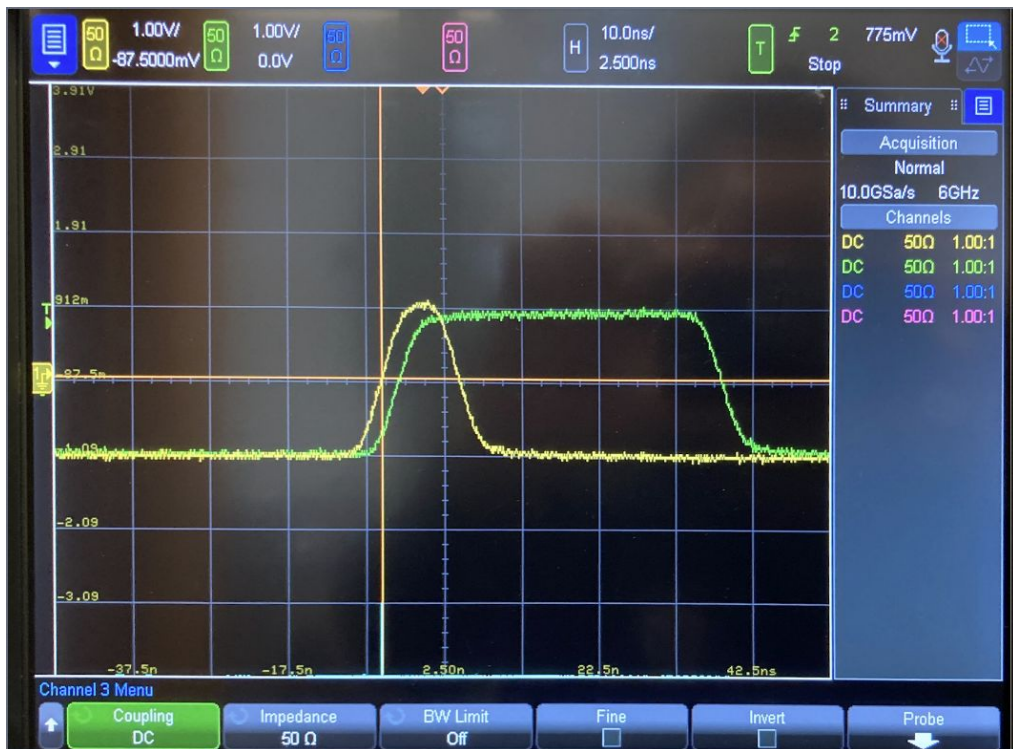


- See report from [CPAD23](#) & new report [here](#)

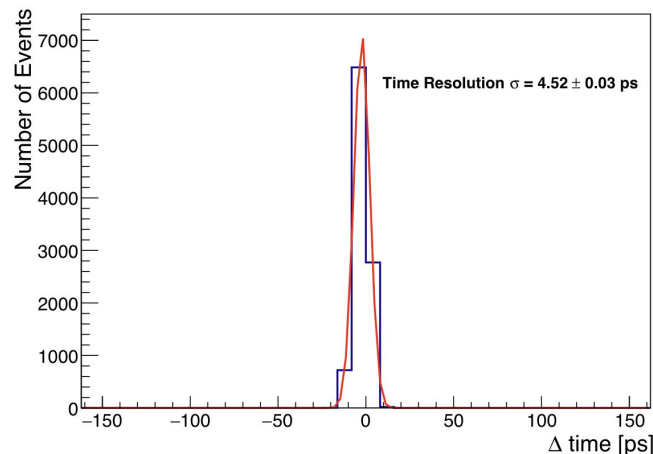


Pulse Generator Study

Start: Pulser CH1 (Yellow)
Stop: Pulser CH2 (Green)



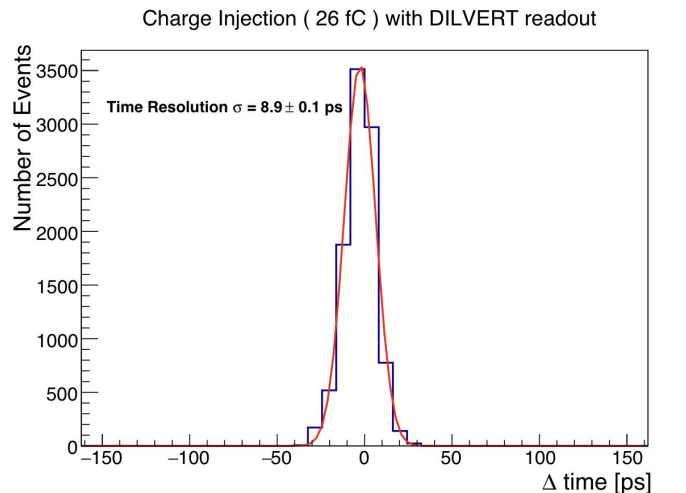
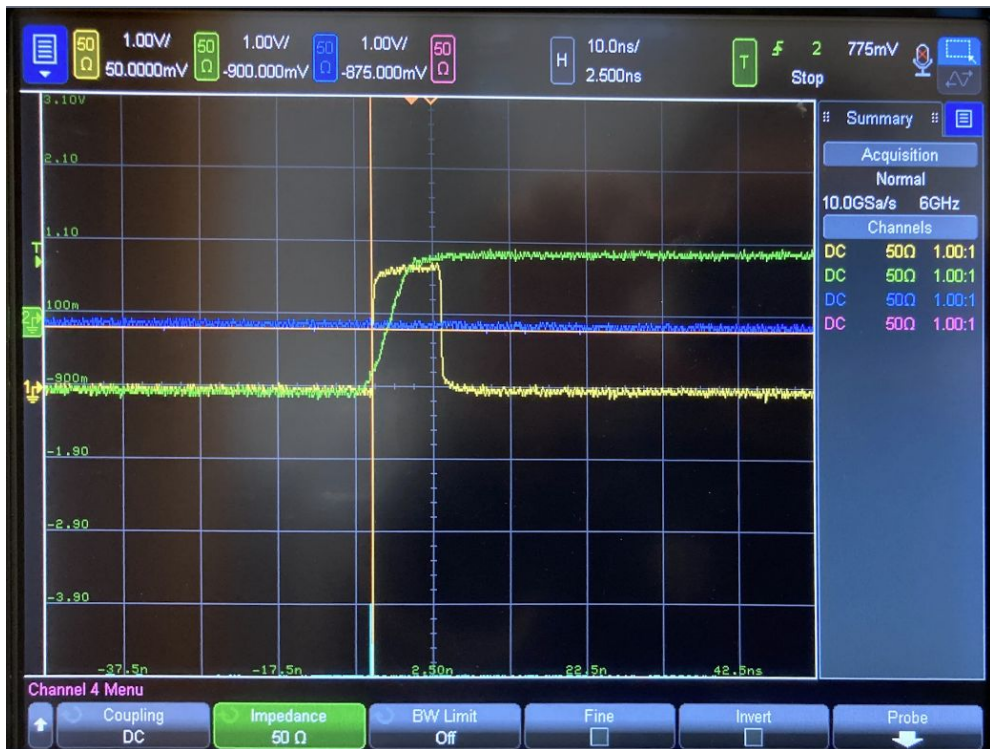
Pulse Generator Test Using DILVERT readout



Pulser jitter contributes 3.6ps

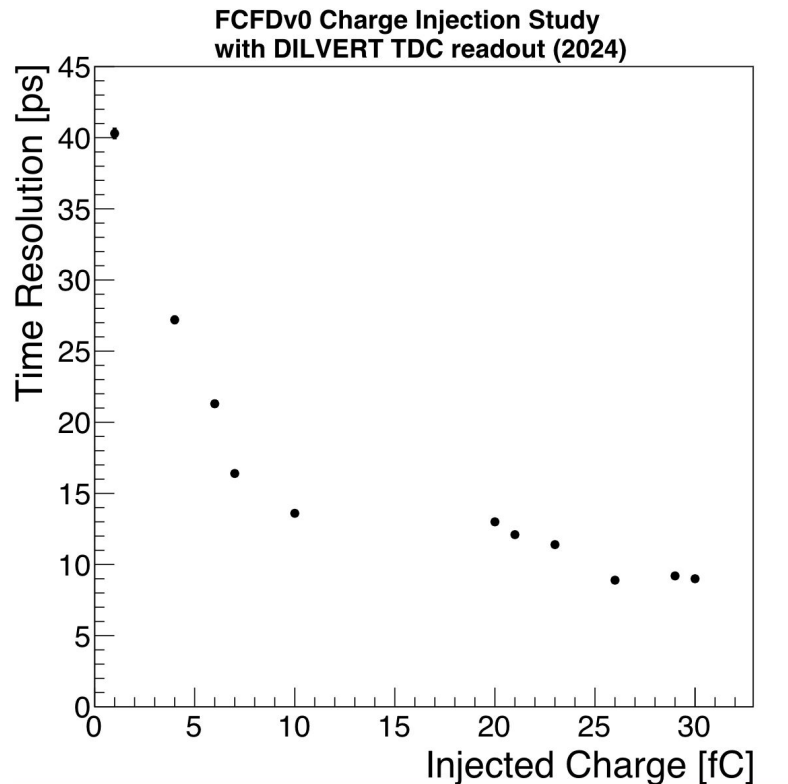
FCFD - Charge Injection Study

Start: FCFD output (Yellow)
Stop: Pulser (Green)



Accounting for FCFD jitter, DILVERT TDC contribution consistent with design spec of better than 4ps.

FCFD - Charge Injection Study

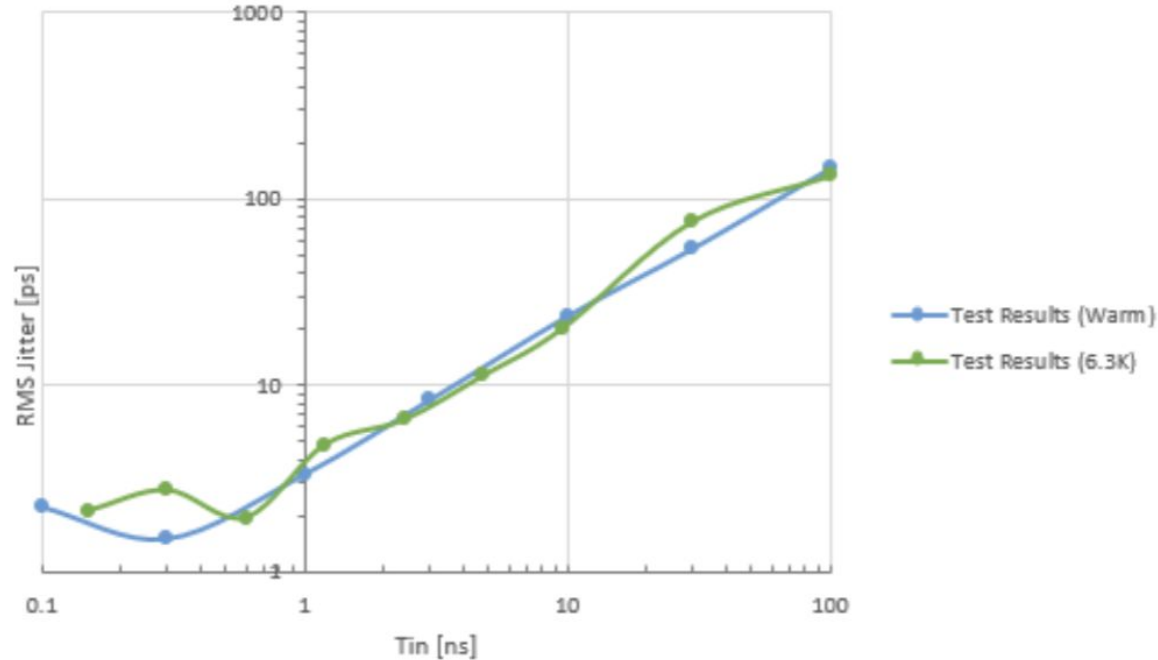


Time resolution as a function of injected charge consistent with previous FCFD study

Accounting for FCFD jitter, DILVERT TDC contribution consistent with design spec of better than 4ps.

Cryogenic Operations

- DILVERT was also calibrated and tested under cryogenic conditions (6K) and demonstrated performance consistent with room-temperature operation



Summary

- Presented characterization results of DILVERT - a cryogenic sub-5ps precision TDC ASIC in 22nm technology
 - Performance verified as designed, jitter maintained below 4 ps
 - Cryogenic operations validated
- Applicability for wide range of experiments including particle physics, quantum communication, precision metrology
- Future work includes implementation in more complex settings:
 - DILVERT design already implemented in more complex chips such as SUNROC for SNSPDs