



SParkDream: Low-Power, High-Bandwidth Photonic Communication for Readout Integrated Circuits

Adam Quinn, Davide Braga
Fermi National Accelerator Laboratory

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Agenda

- Silicon Photonics / tech
- SParkDream Demonstration
- Phase 0: Test Design

Silicon Photonics: A Critical Technology for Future Detectors

100x bandwidth, **100~1000x** lower heat load, **10~100x** channel density, EMI/cross-talk immunity.

Application Areas:

High-Bandwidth, Low-Power RT Readout

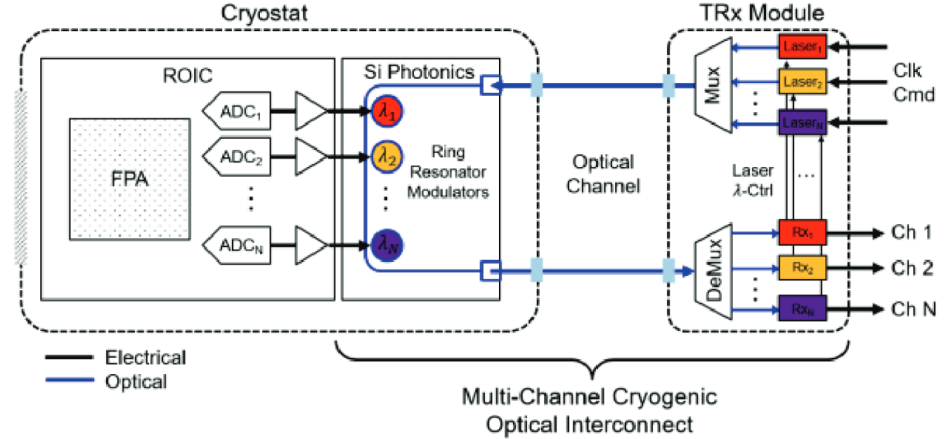
- FCC-ee, FCC-hh
- High-rate X-ray Imagers

Cryogenic (100K, 4K) Readout

- Dune Mod. 3/4
- SNSPDs
- Quantum / SC Readout

Radiation-Hard Readout

- LHC Phase 3



Quotes from ECFA Detector R&D Roadmap:

“Silicon photonics may be a **game-changing technology** in this context thanks to its good integration density and integration synergies with microelectronics.” [7.3.2.3]

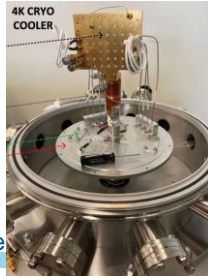
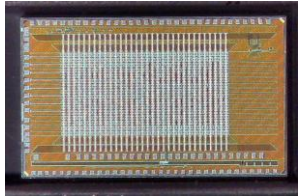
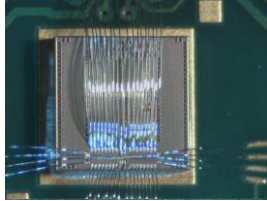
“Silicon photonics as the successor to actively modulated VCSEL-based links, facilitating **full-custom photonic integrated circuits (PICs) for HEP** (DRDT 7.4, DRDT 7.5)” [7.3.2.4]

The SParkDream Collaboration



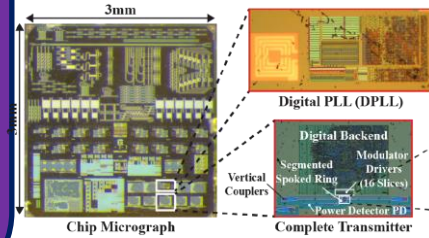
FNAL ASIC Division

- Expertise in analog/MS/digital ASIC design, test, and integration.
- Cryo + Rad-hard test facilities
- **Leverage existing ASIC IP**

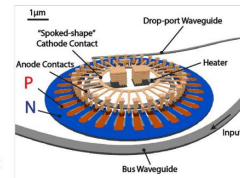
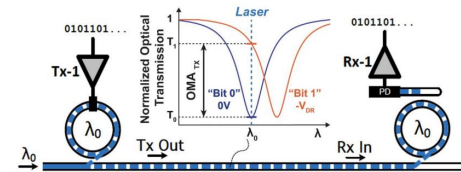


UW EMiT Lab

- Expertise in photonic design & integration.
- High-impact publications around photonic transmitters.
- Photonic test capabilities
- **Build on existing MRM characterization**

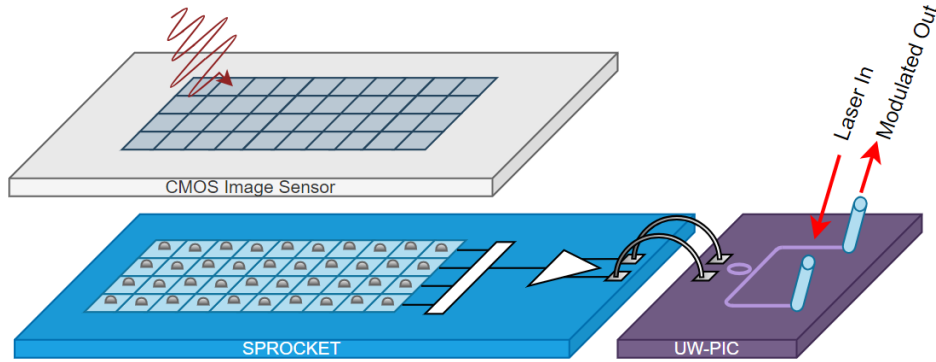


SparkDream

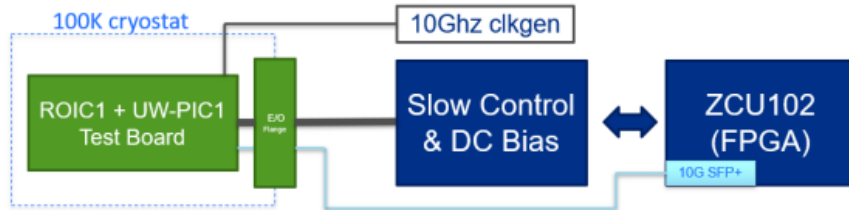


SParkDream (Silicon Photonics Demonstration at Fermilab)

Key Objective: Demonstrate the readout of a pixel detector ASIC using silicon photonics (10.24 Gb/s/chan) at both room and medium (100K) cryogenic temperature.



ROIC/PIC Integration (top)
Demonstration Block diagram (bottom)



We are here. →

Phase 0: Design test software and hardware.

Q1 2025

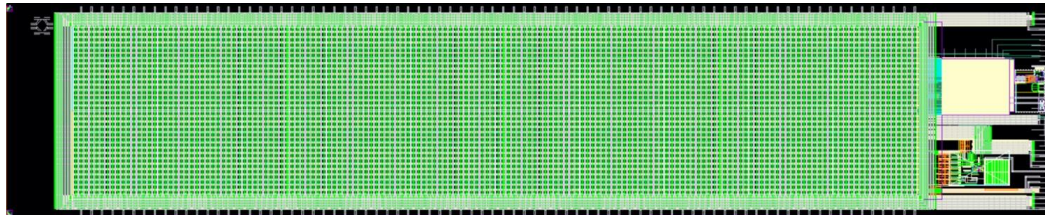
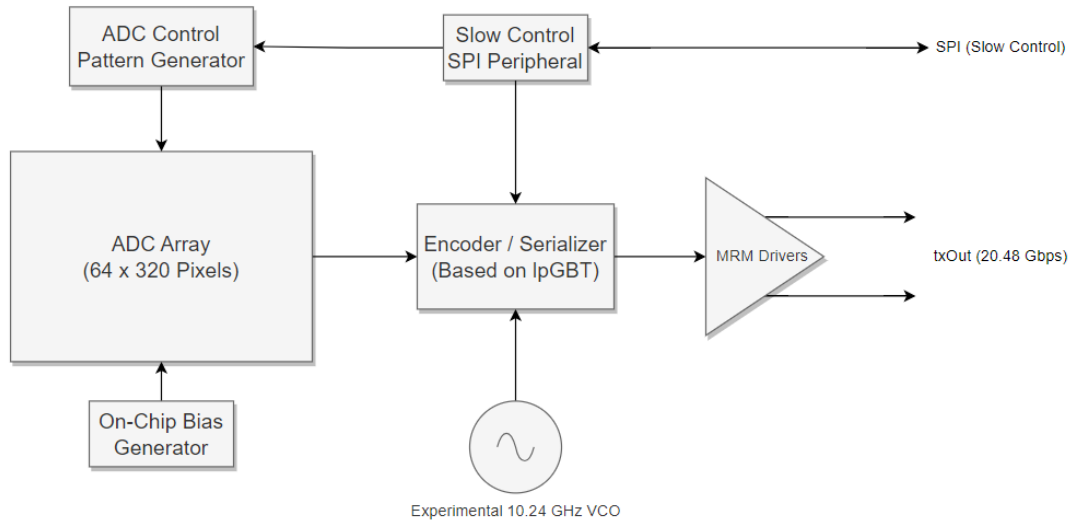
Phase 1: Demo Single-Channel Link @ RT + Cryo

Q3 2025

Phase 2: Demo Wavelength-Division Multiplexing (WDM)

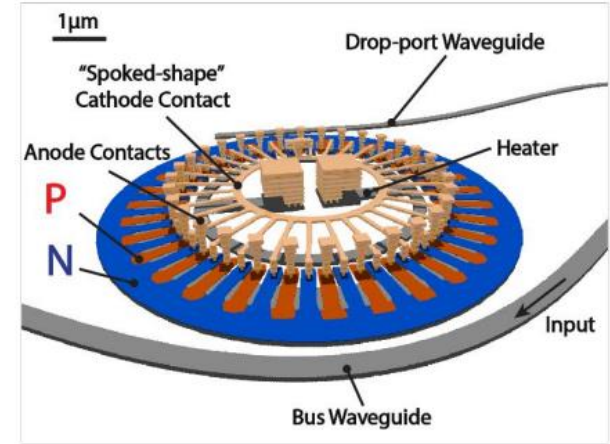
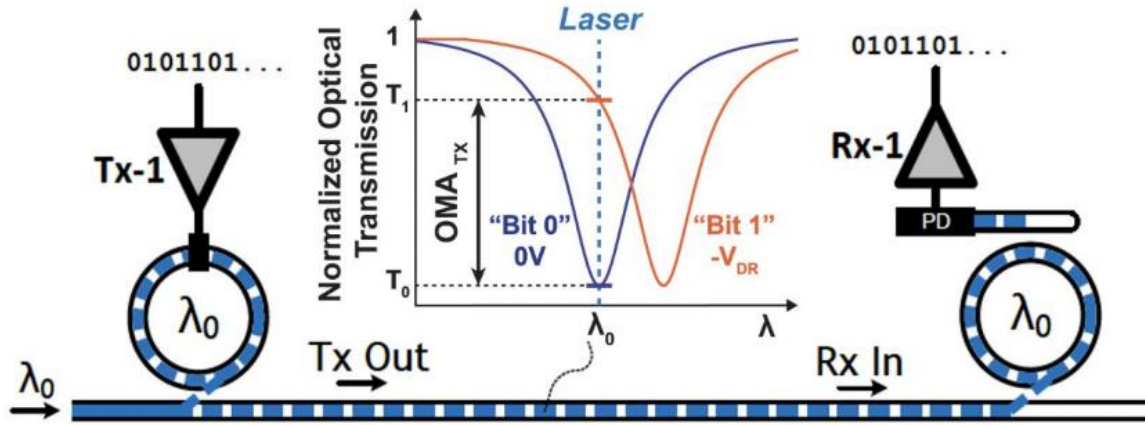
Future Work: Deep Cryo (4K), radiation hardness

SParkDream: The ROIC (SPROCKET3)



- Part of a family of pixel-detector ROICs for high-bandwidth Skipper-CCD readout.
- 20,000 pixels.
- Designed for hybrid integration with a reticle-scale CMOS image sensor.

SParkDream: The PIC (Micro-Ring Modulators)



The Potential:

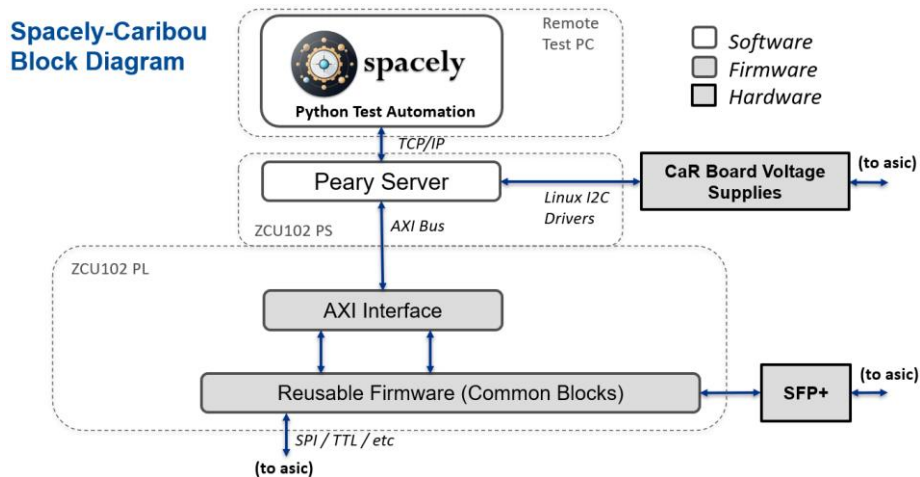
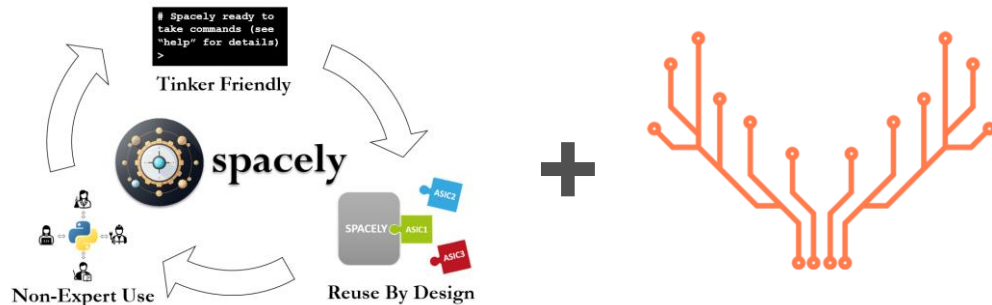
- Extremely high bandwidth through WDM
- Low power (signaling mirror analogy)

The Challenges:

- Improving cryogenic bandwidth
- Tuning cryogenic MRMs
- **Electronic/Photonic Co-design**

SParkDream: The Test Stand (Spacely-Caribou)

- **Spacely:** Open-source Python-based test automation framework for scientific ASICs, developed at Fermilab.
 - <https://github.com/SpacelyProject/spacely-docs>
- **Caribou:** Open-source data acquisition hardware with digital, analog channels, as well as 10.24 Gb/s SFP+ optical interface.
- **Together:** A flexible, open-source test platform for our SiPh demonstrator.



Phase 0: Optical Link Test Stand

Optical CDR and Scope
(Not Connected)

SFP+ Optical
Transmitter

SFP+ Optical
Receiver

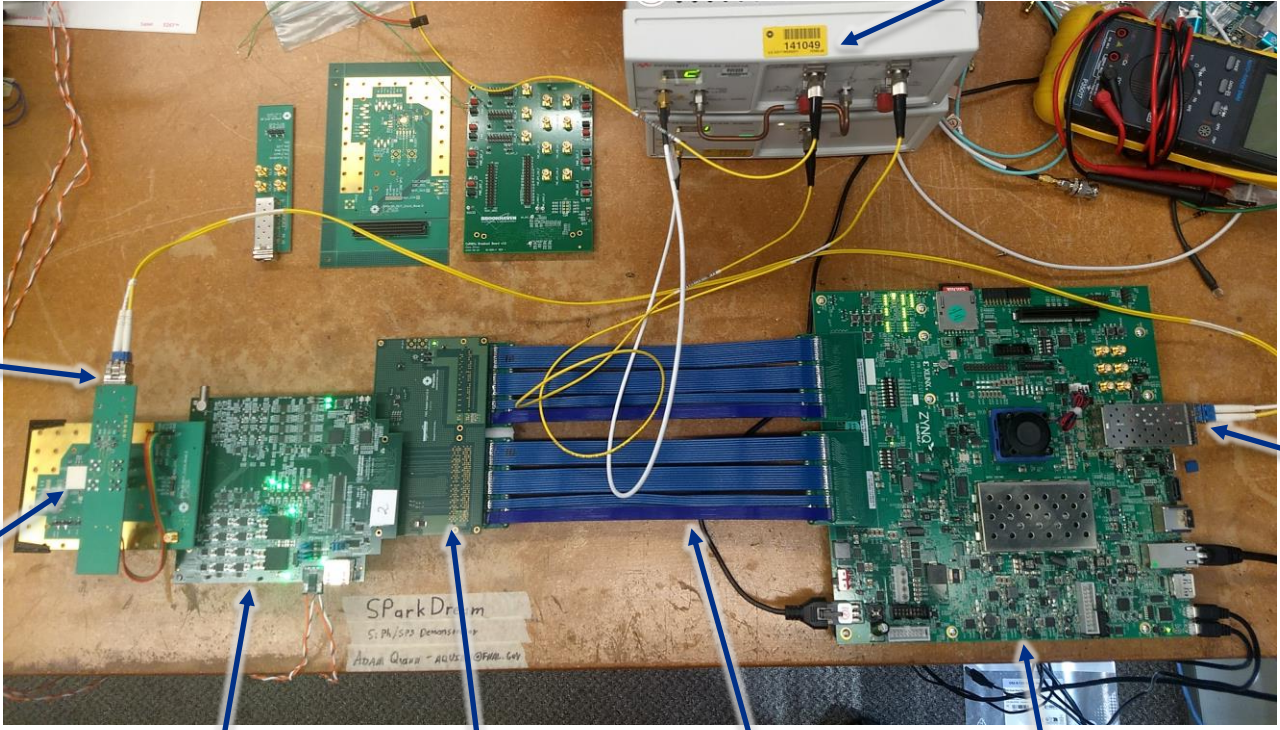
SPROCKET3A
ASIC

CaR Board

ZCU102 FMC
Mezzanine

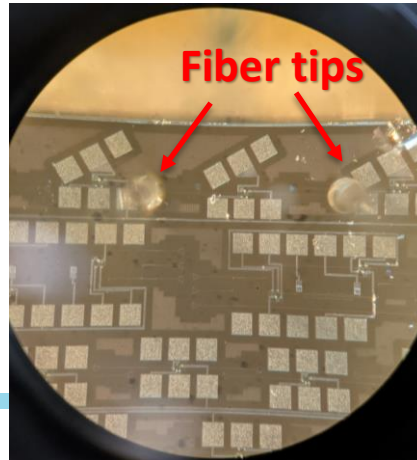
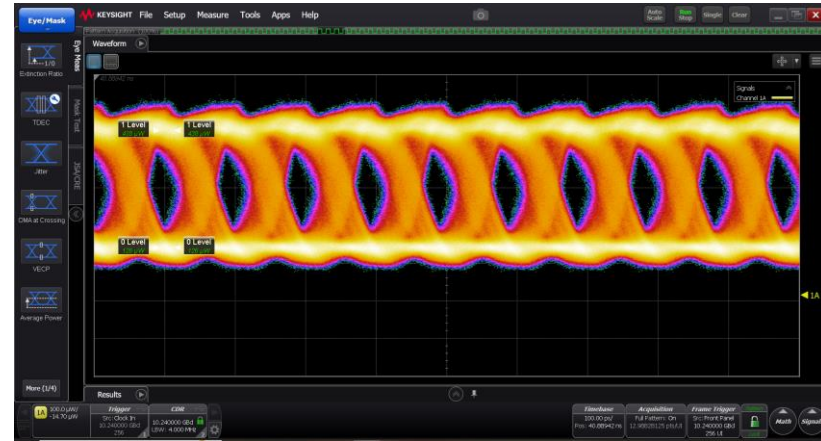
FMC Cables

ZCU102



SParkDream Initial Demonstrations in 2024

- Created a prototype link using a discrete optical transmitter with a driver based on the CERN IpGBT.
- Demonstrated a closed link and data transmission at 10.24 Gb/s. Measured BER < $3.2e-15$.
- Initial independent verification of ASIC and FPGA firmware.
- Prototyped micro-positioners and demonstrated successful alignment to photonic IC grating couplers.



Future Work

- Detailed planning underway for Phase 1 / 2 Tests in Spring 2025.
- Verifying complete test setup “Digital Twin” with Spacely.

Learn More About:

- Spacely:
<https://github.com/SpacelyProject/spacely-docs>
- SPROCKET:
<https://arxiv.org/abs/2406.15207>

