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A 10GHz Low-Jitter Cryogenic PLL For Quantum Applications in 22nm

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Quantum computing (QC) applications require the manipulation and readout of thousands or even millions of quantum bits (qubits) to execute quantum algorithms. Utility-scale quantum systems rely on classical control and readout cryo-electronics, which must be tightly integrated with the qubits in the same environment. This integration reduces the connections between the cryogenic plane and room temperature, lowering the latency of the control loop necessary for implementing error correction algorithms. A major challenge in developing large-scale, practical quantum computers is the complexity of interconnects between milli-kelvin qubits housed in dilution refrigerators and room-temperature (RT) controllers.

The ROADS project focuses on innovating qubit readout through multiplexing and data conversion. A popular readout scheme combines RF reflectometry with frequency domain multiplexing, where many qubits share a single RF transmission line, each tuned to a unique resonant frequency for parallel readout. However, ROADS is advancing toward direct-to-digital conversion, which requires wide bandwidth and high linearity. This involves generating and acquiring high-speed, high-accuracy, low-noise signals at cryogenic temperatures (CT), particularly the clock signals generated by a cryogenic phase-locked loop (PLL).

Designing a cryo-CMOS PLL for QC applications presents several challenges. First, low phase noise (PN) and low reference spurs (SREF) are essential to avoid limiting qubit control fidelity. Second, the PLL must function at CT, where transistor parameters differ significantly from RT, and no mature device models exist. For instance, the threshold voltage of transistors increases by ≈ 150 mV, and carrier mobility can double at CT. While ON-resistance of a transmission gate decreases when the input voltage is near the supply or ground level, it can increase by two orders of magnitude when the input is near the middle of the supply voltage, posing issues in sampling circuits. Additionally, transistors exhibit poorer matching at CT, degrading the linearity of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and current sources. Low power consumption (Pdc) is also crucial, given the limited cooling power of cryogenic refrigerators and the need to control more qubits.

This abstract presents a 10GHz low-jitter cryogenic PLL fabricated in GF 22nm FDX process, capable of operating at 4.2 K. To meet the challenges of cryogenic operation, an analog PLL architecture is employed to maintain high performance from 300 K to 4.2 K. A charge-pump type II PLL architecture was designed and implemented, comprising key sub-blocks such as the phase and frequency detector (PFD), charge pump, low-pass filter (LPF), LCVCO, and clock divider. The VCO frequency is integrated into a phase shift, which feeds back into the PFD. To compensate for temperature variations and reduce periodic disturbances, the PLL features programmable charge pump current and LPF bandwidth settings. A binary-controlled MOM capacitor array broadens the VCO tuning range, ensuring optimal loop parameters with good phase noise performance and loop stability. Phase noise and jitter measurements are currently underway and will be presented at the Workshop.

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