



A 10GHz Low-Jitter Cryogenic Phase-Locked Loop (PLL) For Quantum Applications

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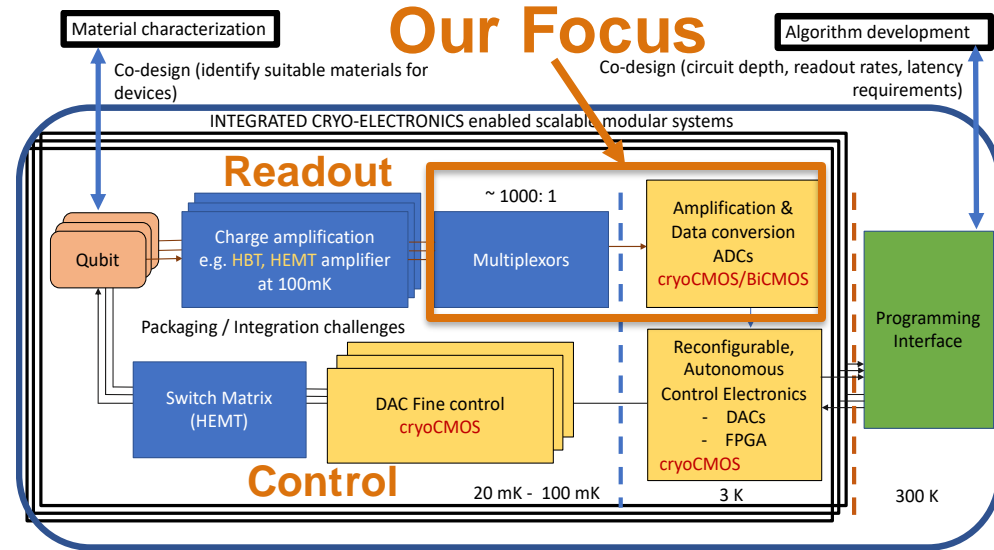
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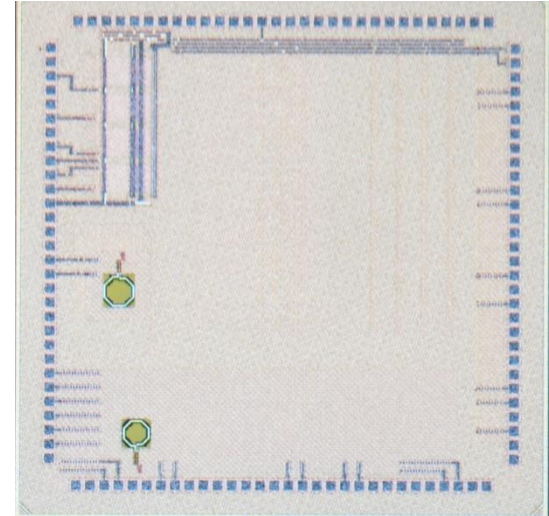
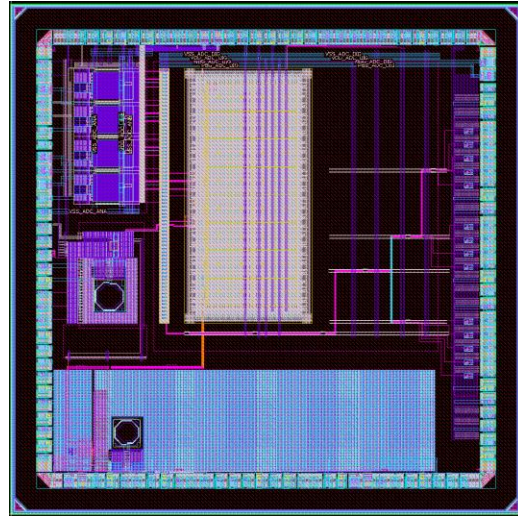
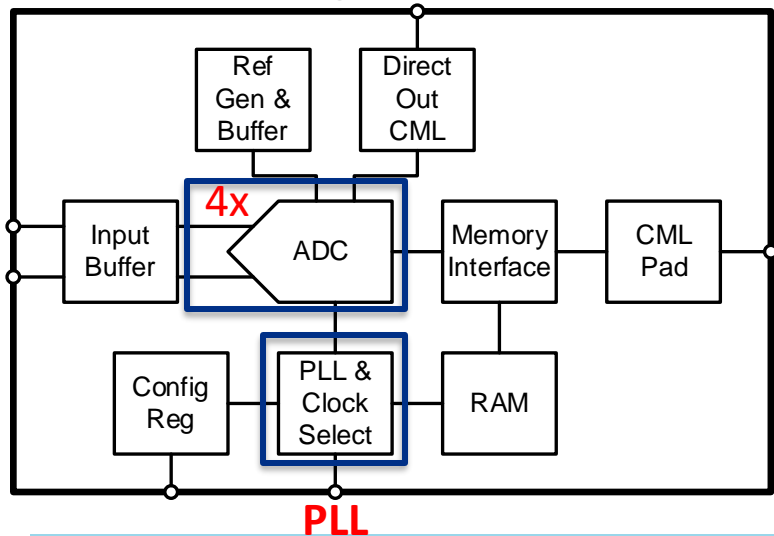
Cryo-electronics for Utility-Scale Quantum Systems

- Utility-scale quantum systems require classical control and readout cryo-electronics
- They must be tightly integrated with qubits in the same environment
 - Drastically reduces the connections between the cryogenic plane and room temperature
 - Lowers the latency of the control loop for implementing error correction algorithms
- A large-scale system is needed for high throughput testing qubit devices
 - Achieves parallel characterization to determining the best candidates for qubits arrays
 - Phase-Locked Loop to generate high-speed low-jitter clock signals for qubits readout

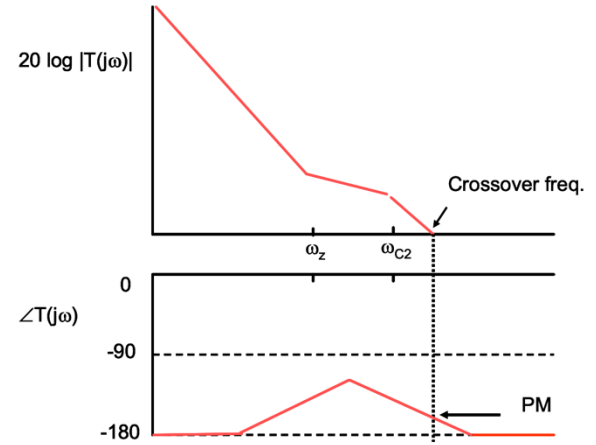
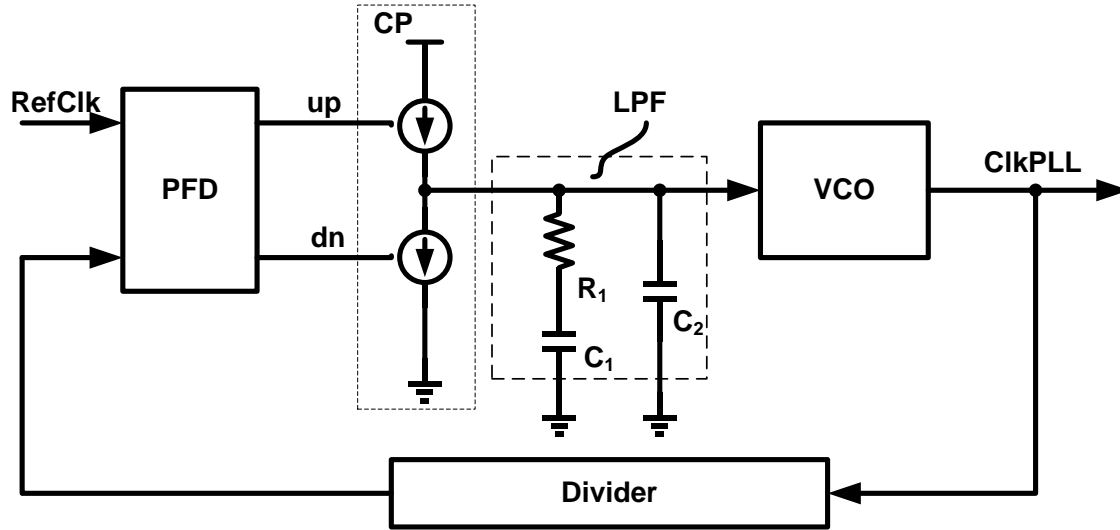


First Prototype

- This ASIC designed in GF22 FDX is the first milestone for the cryogenic Qubits readout effort
- Including four full sub-ADCs (588 Msps, Max 55dB SFDR), and a full-speed (10GHz) PLL
- Peripheral blocks: input buffering, reference generation, digital interface, and digital sample storage

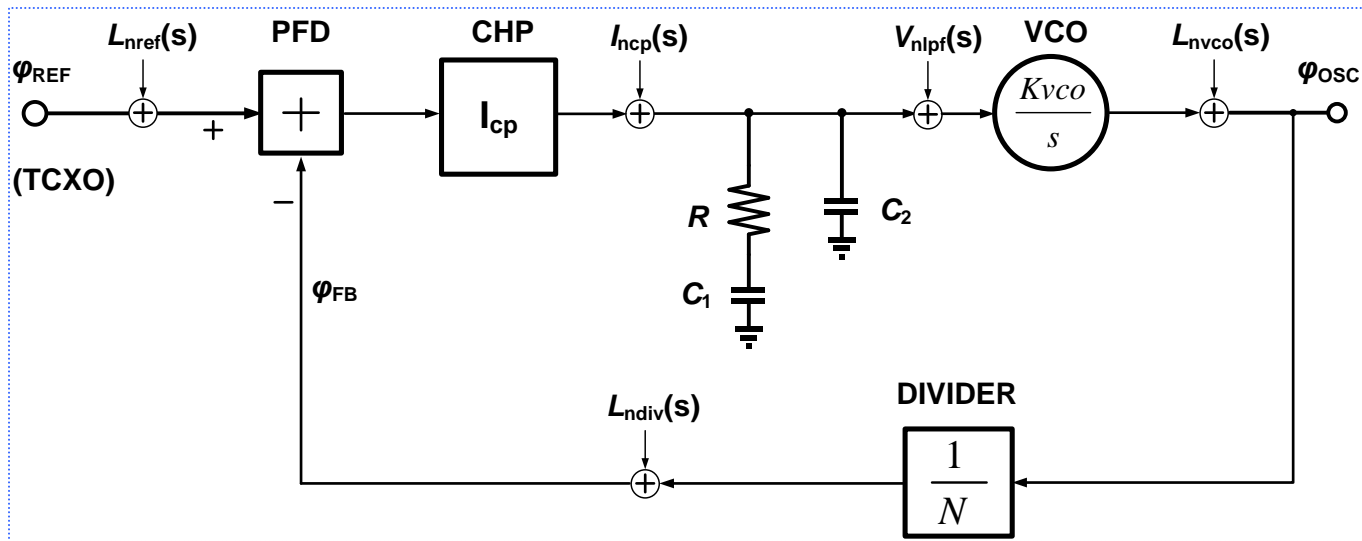


PLL Architecture



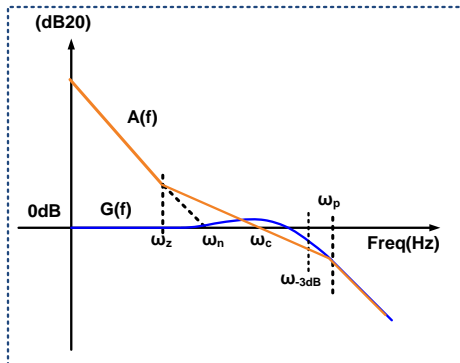
- Type II Charge-pump LC-PLL
- Analog 3rd order PLL with passive loop filter
- R_1 introduces a Zero to ensure the phase margin
- Reducing reference spurs and improving jitter by adding a second capacitor directly connected to VCO control voltage
- Programmable I_{cp} , R and C to cover PVT variations
- Binary-controlled Cap bank to widen the tuning range

Type II Charge Pump PLL Linear Model



- VCO (Voltage controlled oscillator)
- CHP (Charge pump)
- PFD (Phase and frequency detector)
- Frequency Divider N
- The loop filter comprises R , C_1 and C_2
- PFD and CP is modeled as constant gain
- VCO is modeled as voltage to frequency constant gain and frequency to phase integrator
- Frequency divider is modeled as constant loss

Type II Charge Pump PLL Linear Model



Open loop transfer function

$$A(s) = \frac{I_{CP}}{2\pi} \cdot \frac{1}{N} \cdot \frac{1+s/\omega_z}{(C_1+C_2) \cdot s \cdot (1+s/\omega_p)} \cdot \frac{K_{vco}}{s}$$

Zero frequency

$$\omega_z = \frac{1}{R \cdot C_1}$$

Pole frequency

$$\omega_p = \frac{1}{R \cdot C_1 C_2 / (C_1 + C_2)}$$

Cutoff Frequency

$$\omega_c = \frac{I_{cp} K_{vco} R}{N}$$

$$\omega_n = \omega_c / 2\zeta$$

Close loop transfer function

$$G(s) = \frac{A(s)}{1+A(s)}$$

Natural Frequency

$$\omega_n = \sqrt{\frac{I_{cp} K_{vco}}{(C_1 + C_2) \cdot N \cdot 2\pi}}$$

Damping Factor

$$\zeta = \frac{\omega_n}{2 \cdot \omega_z}$$

$$\omega_{-3dB} = 2 \omega_n \text{ for } \zeta = 0.707$$

$$\omega_{-3dB} = 2.5 \omega_n \text{ for } \zeta = 0.1$$

Close loop -3dB bandwidth

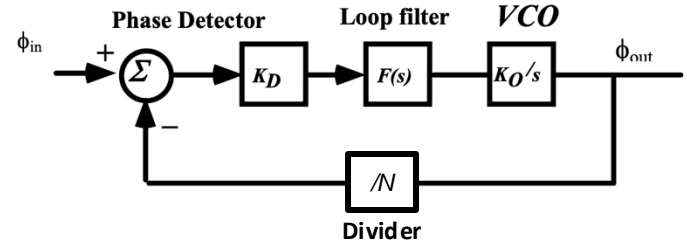
$$\omega_{-3dB} = \omega_n \cdot \sqrt{(2\zeta^2 + 1) + \sqrt{(2\zeta^2 + 1)^2 + 4}}$$

- Damping factor $\zeta > 0.707$. -- settling time (avoid overshooting, gain peaking and ringing)
- Closed-loop bandwidth $\omega_{-3dB} < \omega_{ref} \cdot 1/10$ -- stability
- Optimizing ω_{-3dB} -- phase noise and jitter performance

Reference Noise Transfer Function

Reference Noise:

$$\begin{aligned}\frac{\phi_{out}}{\phi_{ref}} &= \frac{\text{Forward Path}}{1 + T(s)} = \frac{K_V F(s) / s}{1 + K_V F(s) / Ns} \\ &= \frac{N(1 + s / \omega_2)}{Ns^2 / K_V + s / \omega_2 + 1}\end{aligned}$$

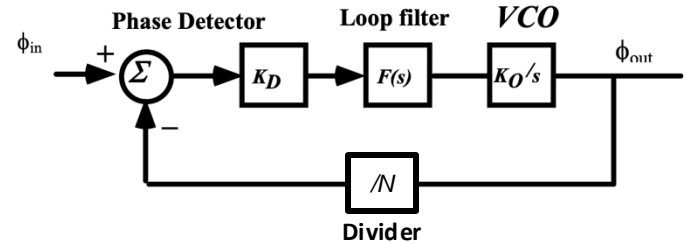


- Low pass transfer function
- Magnitude approaches N as “s” becomes small
- Reference phase noise is low pass filtered by the loop.
- Reference phase noise can be quite low when a crystal oscillator is used to generate the reference frequency.
- In-band reference phase noise gets multiplied by a factor of N for the integer N PLL.
 $\phi_{out} = N \phi_{ref}$ - **Small N Preferred**

VCO Noise Transfer Function

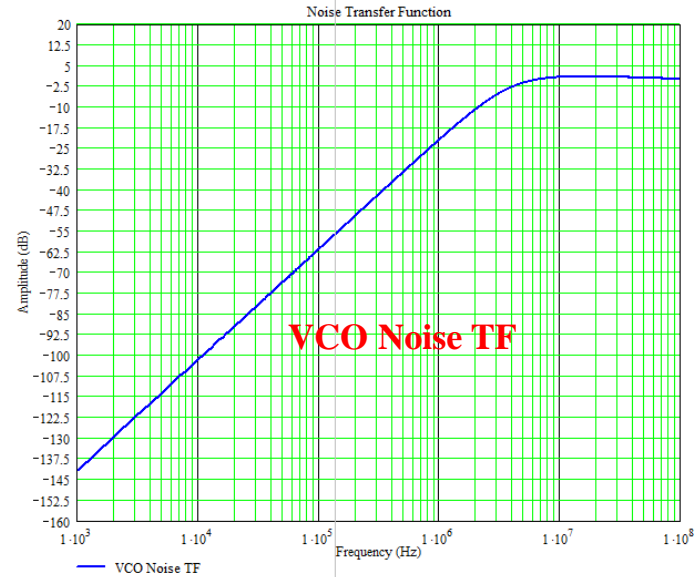
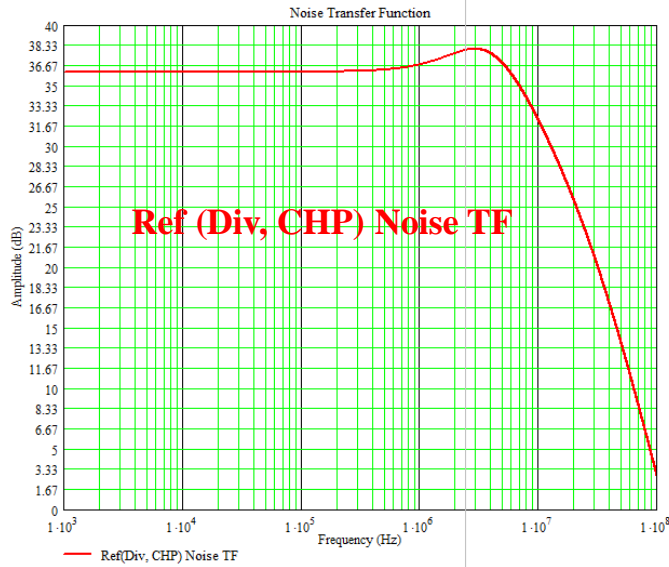
VCO Noise:

$$\begin{aligned}\frac{\phi_{out}}{\phi_{vco}} &= \frac{\text{Forward Path}}{1 + T(s)} = \frac{1}{1 + K_V F(s) / Ns} \\ &= \frac{Ns^2 / K_V}{Ns^2 / K_V + s / \omega_2 + 1}\end{aligned}$$



- High pass transfer function
- Approaches a magnitude of 1 as “s” becomes large
- The PLL can be used to clean up the VCO phase noise within the loop bandwidth. VCO phase noise is unattenuated at offset frequencies beyond the loop bandwidth.

Loop Bandwidth and Noise Transfer Function



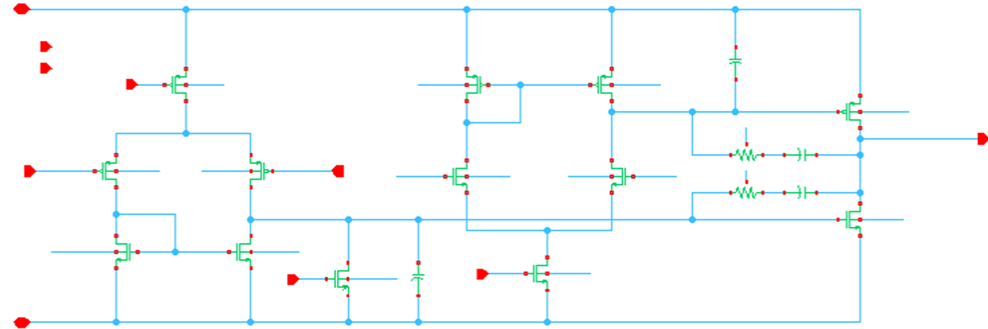
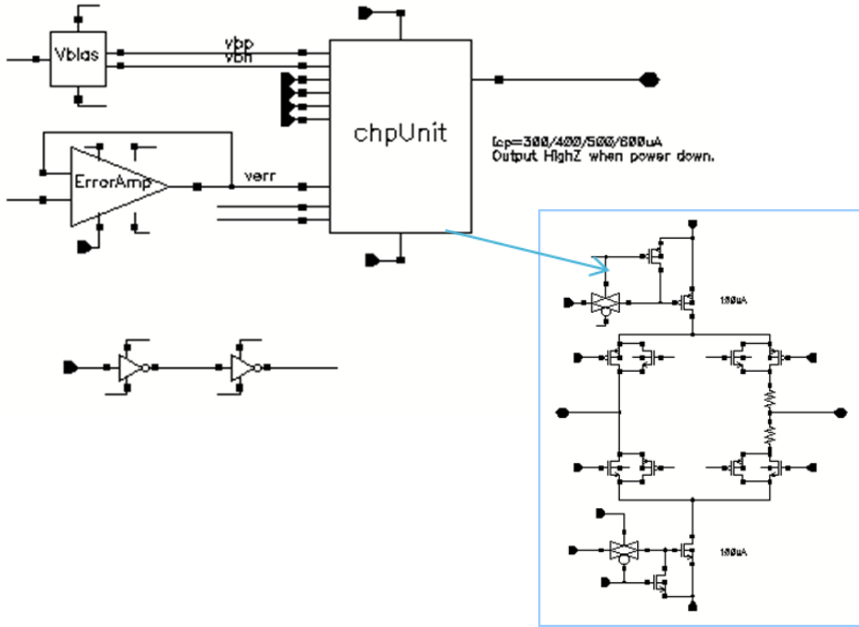
- ◆ Jitter optimization bandwidth
- ◆ NF of Ref., Div, CHP is low pass --- Low bandwidth is preferred
- ◆ NF of VCO is high pass --- High bandwidth is preferred

- ◆ Stability limits the maximum bandwidth
- ◆ $\omega_{3dB} \leq \omega_{ref}/10$
- ◆ VCO noise dominates, so low VCO PN is critical

$$\omega_{3dB} < \omega_{ref}/10$$

Higher ω_{ref} is desirable

PLL Charge Pump Design

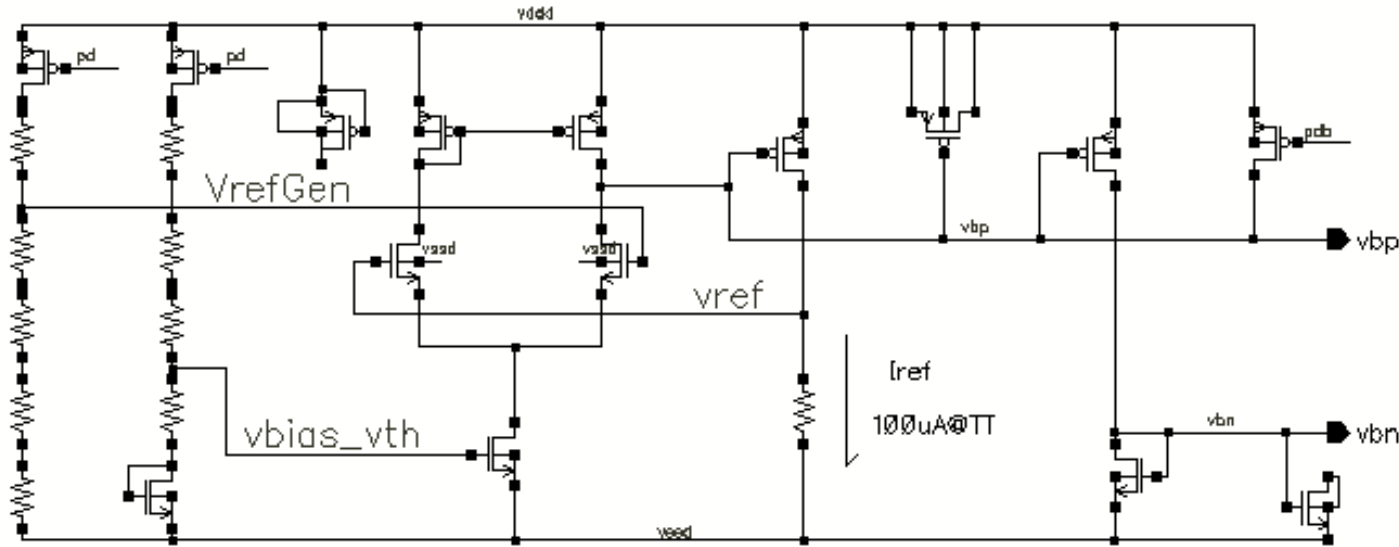


Error Amplifier for Charge Pump

- Drain switching charge pump
- One stage error amplifier to mitigate charge sharing
- Internal current reference and bias generator

- Two-pair inputs (N pair and P pair) – ideally rail-to-rail input common mode voltage
- Class AB output stage – ideally rail-to-rail output voltage range
- Minimum open loop gain: 20dB – assume 10% variation between voltages
- Minimum GBW 160MHz – reference frequency

Bias Generator for Charge Pump



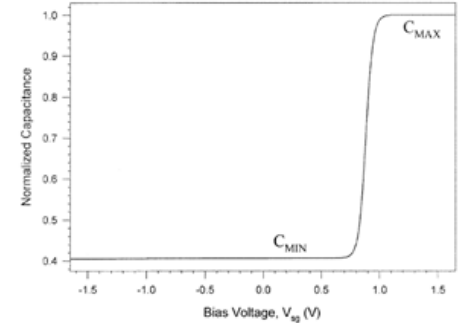
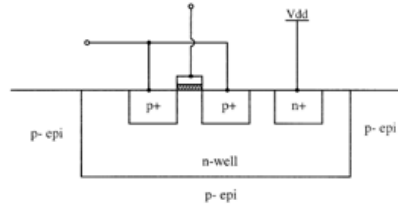
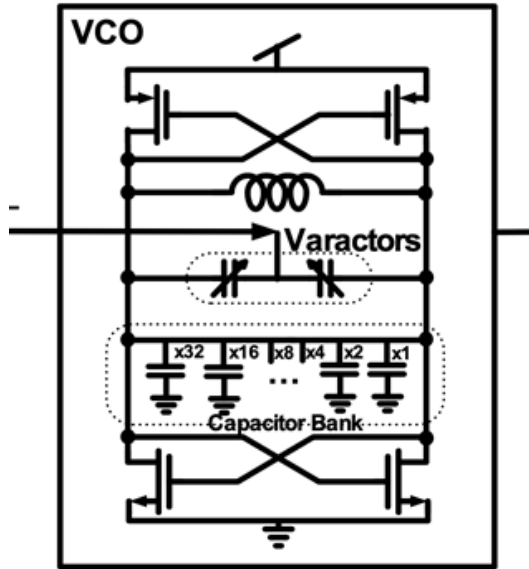
- R in the Bias Generator and the Rz in the LPF have the same temp variation.
- R/Rz should be stable.

- Minimizing the loop temperature variation
- Resistor divider voltage reference (VrefGen)
- Temperature depended bias (vbias_vth)
- Voltage over resistor 100uA current generator
- P and N voltage bias outputs

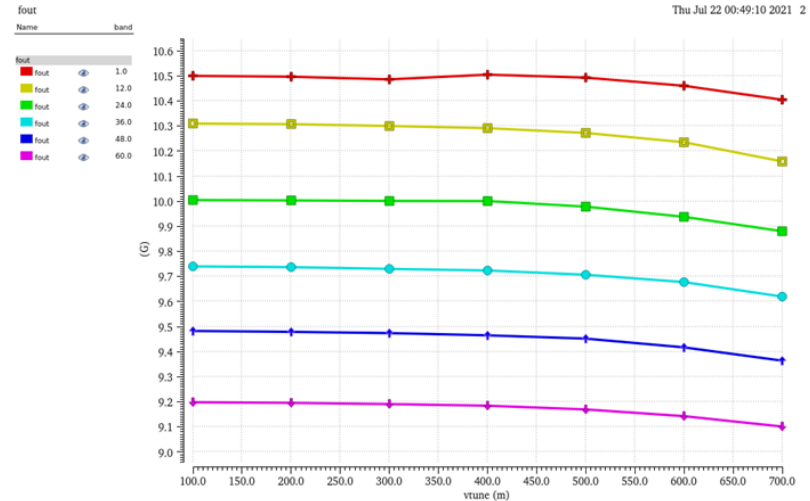
$$A(s) = \frac{I_{CP}}{2\pi} \cdot \frac{1}{N} \cdot \frac{1 + s/\omega_z}{(C_1 + C_2) \cdot s \cdot (1 + s/\omega_p)} \cdot \frac{K_{vco}}{s}$$

$$\omega_p = \frac{1}{R \cdot C_1 C_2 / (C_1 + C_2)}$$

PLL VCO Design

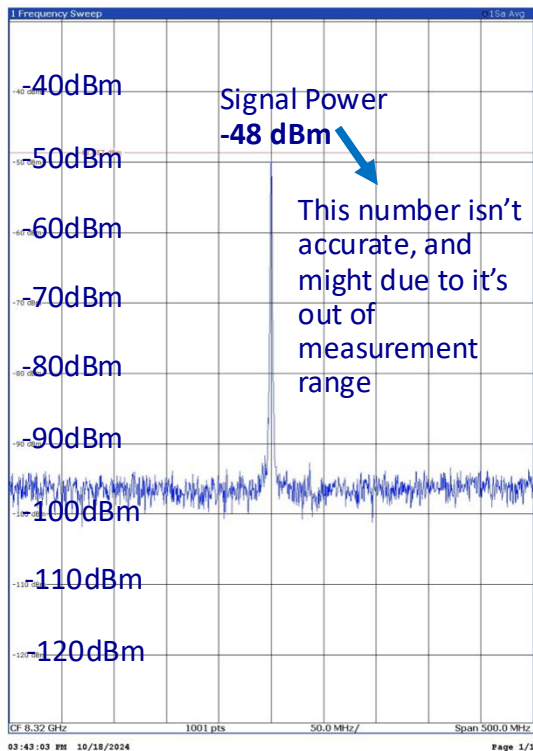
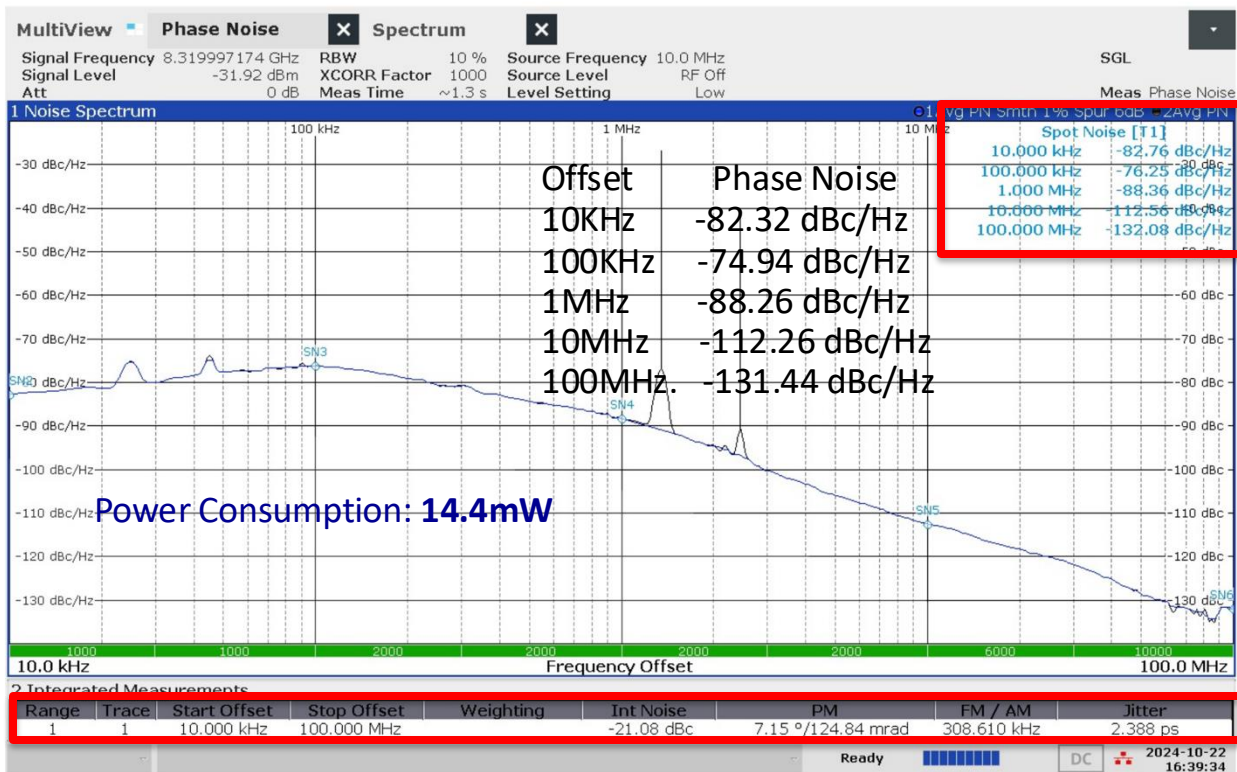


(c) PMOS Inversion-mode Varactor



- VCO is one of the critical blocks in the PLL
- Self-biased cross-coupled architecture – eliminate the flicker noise from tail current transistor
- Varactors provide single-band fine tuning
- Capacitor banks widen the coarse tuning range

Measurement Results – Room Temperature 300K

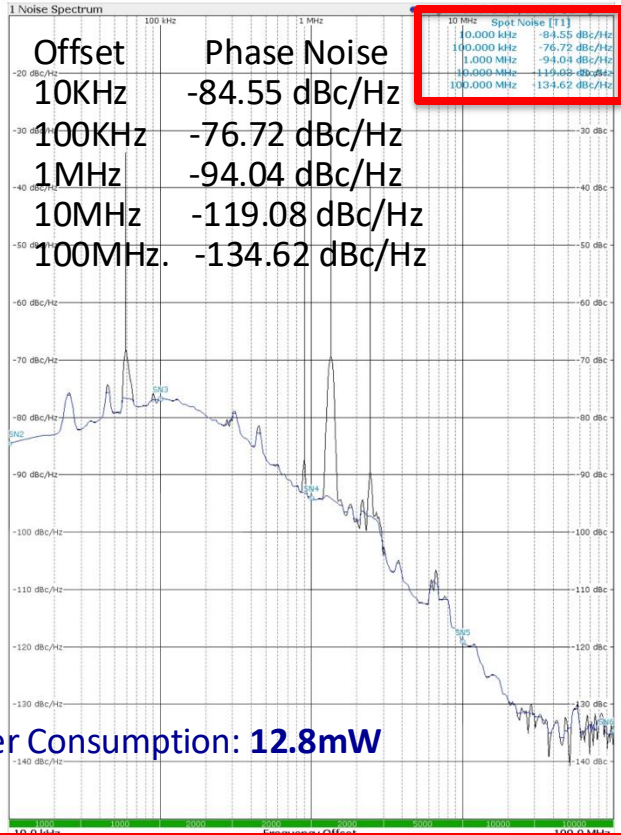


Phase Noise

RMS Jitter= 2.388ps

Spectrum

Measurement Results – Cryogenic Temperature 7K

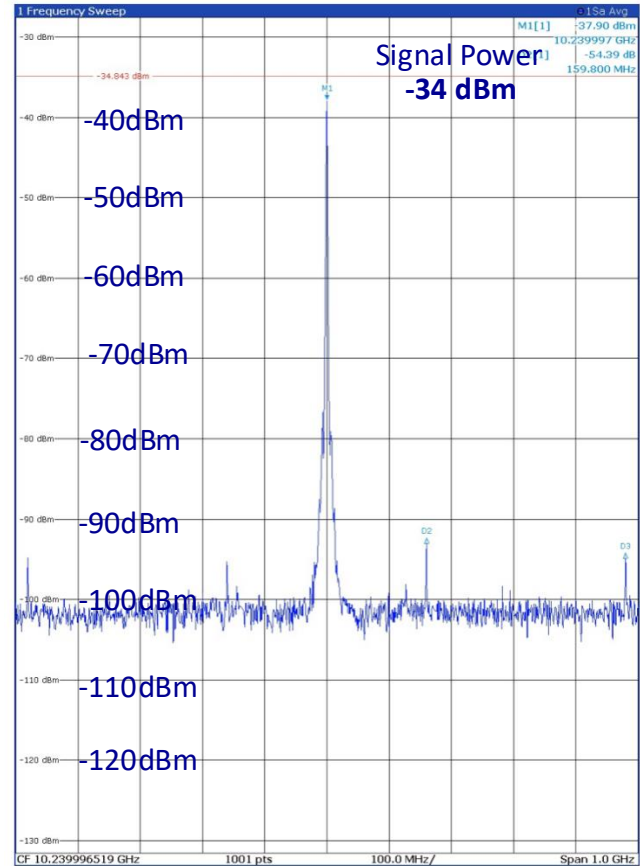


Phase Noise

RMS Jitter
=1.86ps

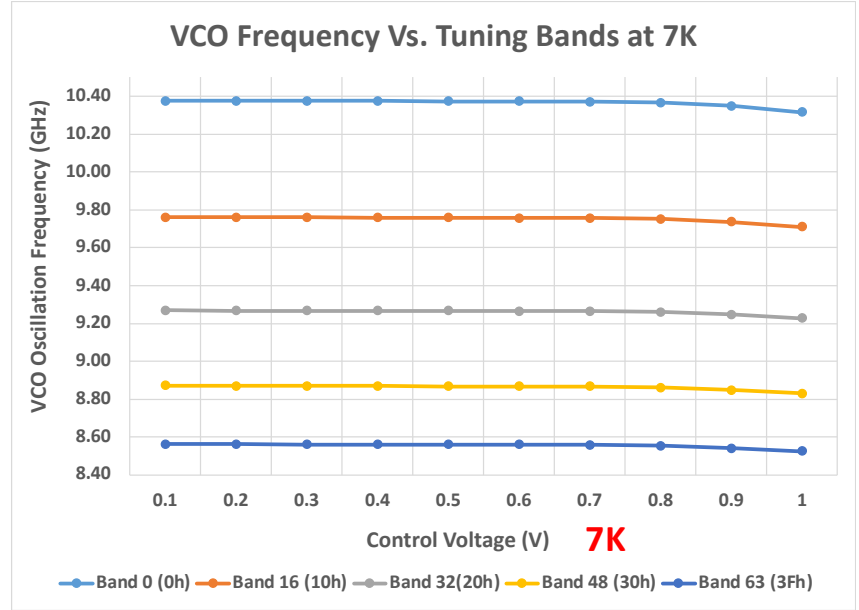
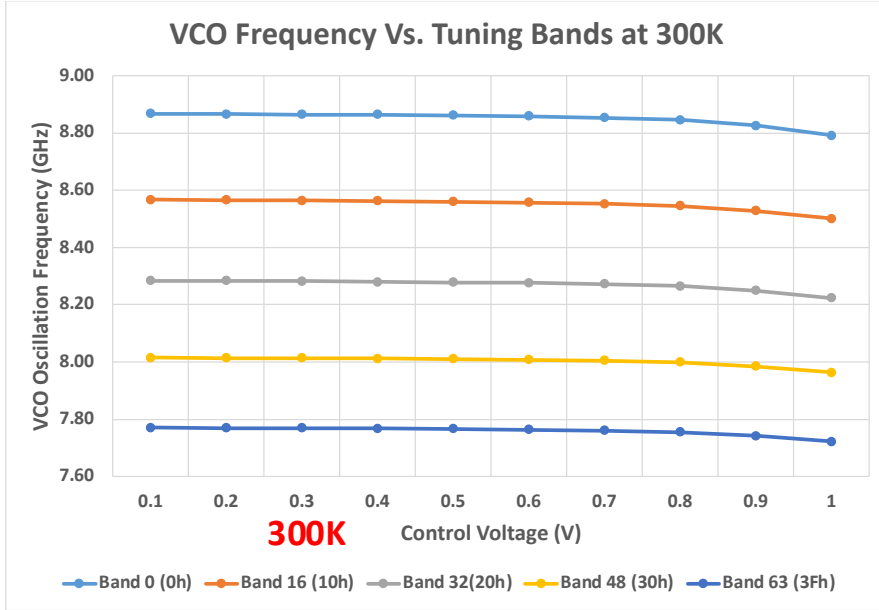
Power Consumption: 12.8mW

2 Integrated Measurements										
Range	Trace	Start	Offset	Stop	Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	10.000 kHz	100.000	-22.31 dBc	6.21 °/108.43 mrad	194.321	1.860 ps



Spectrum

Measurement Results – VCO Tuning Range and Kvco



10%-16% Frequency Variation – useful information ensuring tuning range at cryogenic covers target frequency

Temperature 300K	Band 0	Band 16	Band 32	Band 48	Band 63
Kvco (MHz/V)	84.62	73.96	66.13	57.60	54.76

Temperature 7K	Band 0	Band 16	Band 32	Band 48	Band 63
Kvco (MHz/V)	66.13	56.18	46.22	46.22	40.53

20%-30% Kvco Variation - useful information ensuring loop bandwidth is optimal at cryogenic temperature

Conclusions

- A 10 GHz cryogenic PLL designed in GF 22nm FDX is fully functional
- 11% power saving at cryo (14.4mW@300K vs. 12.8mW@7K)
- 21.8% RMS jitter reduction at cryo (2.38ps@300K vs. 1.86ps@7K)
- 10%-16% Frequency Variation between 7K and 300K
20%-30% Kvco Variation between 7K and 300K
- Higher signal power is obtained at cryogenic temperature – due to higher mobility
- A new sampling-based PLL has been development for a target of 10's fs RMS jitter

Thank You