

2024 Coordinating Panel for Advanced Detectors (CPAD) Workshop

Nov. 18-22, 2024 | University of Tennessee, Knoxville

RDC4 | Readout and ASICs

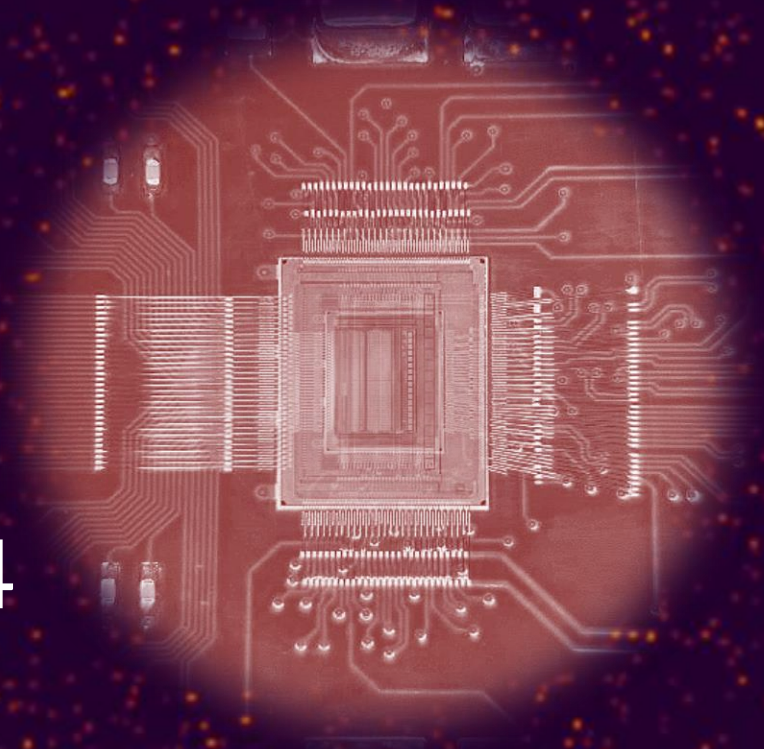
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Cryogenic CMOS Amplifiers for Enhanced Sensitivity in the CMB-S4 Experiment

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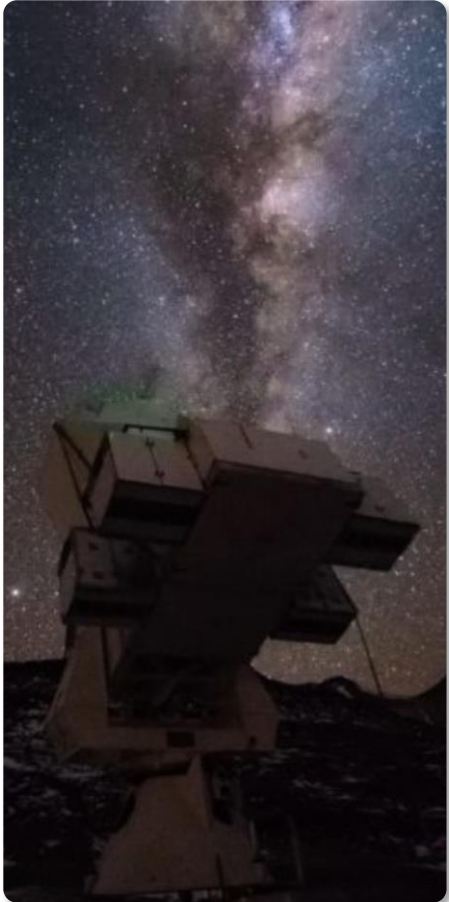
Agenda

1. Motivation
2. SQUID readout
3. Amplifier specs and architecture
4. Simulation results
5. System interface

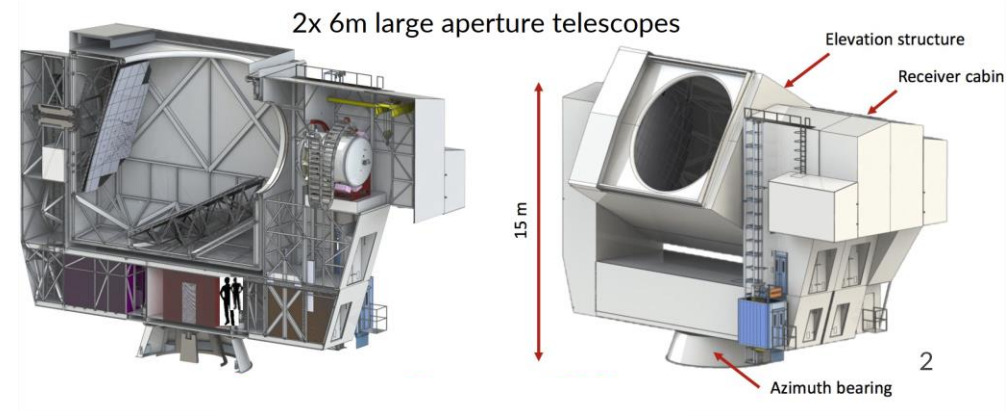
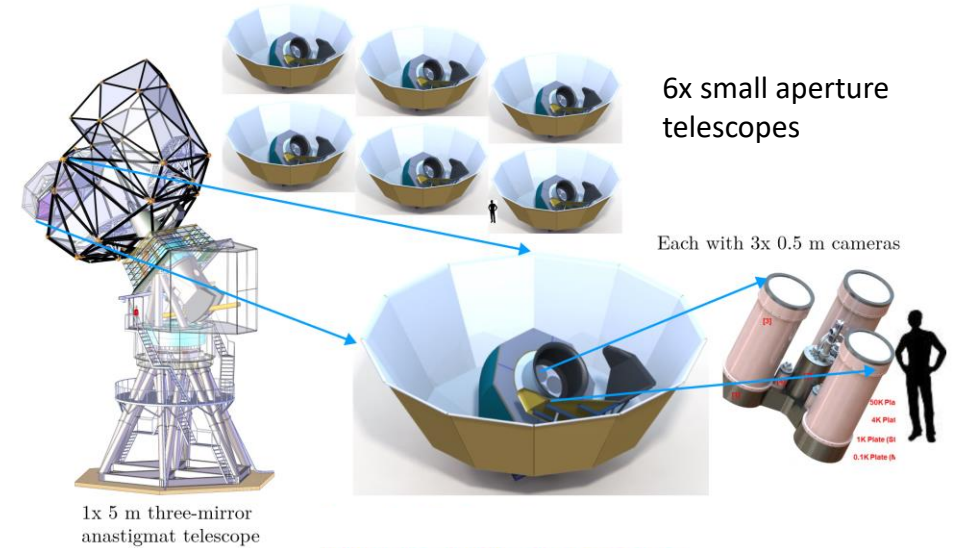
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Motivation

CMB-S4



- **CMB-S4: Cosmic Microwave Background Stage 4**
<https://cmb-s4.org/>
- 12 telescopes (> 500, 000 superconducting sensors) surveying the sky over 20 – 270 GHz
 - Order of magnitude more sensors on sky than all existing efforts combined!
- **Transformative discoveries [1, 2, 3] in:**
 - Fundamental physics
 - Cosmology
 - Astrophysics
 - Astronomy



Current challenges and proposed solution

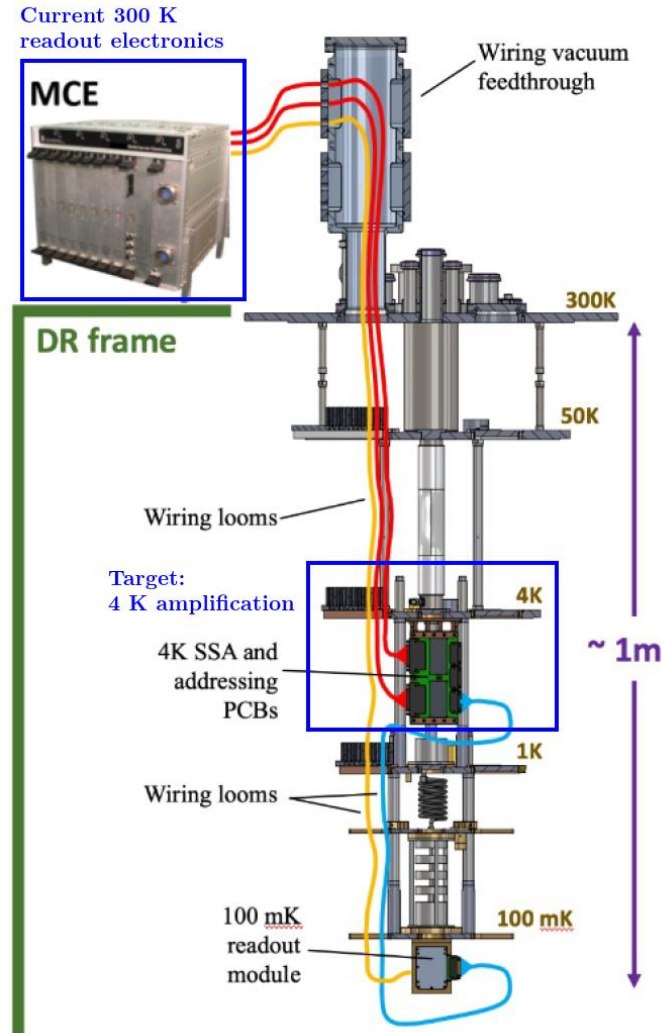
Challenges

- SQUID* signals are very weak ($< 100 \mu\text{V}$)
→ Ultra-low-noise amplifier is needed
- Cabling from Cryo to 300 K is susceptible to crosstalk

Pros of a cryogenic amplifier

- Reduce system complexity
- Higher robustness against crosstalk
- Better SNR and performance
- Enable channel multiplexing → no longer limited by the $R_{\text{SQUID}} C_{\text{cable}}$ time constant

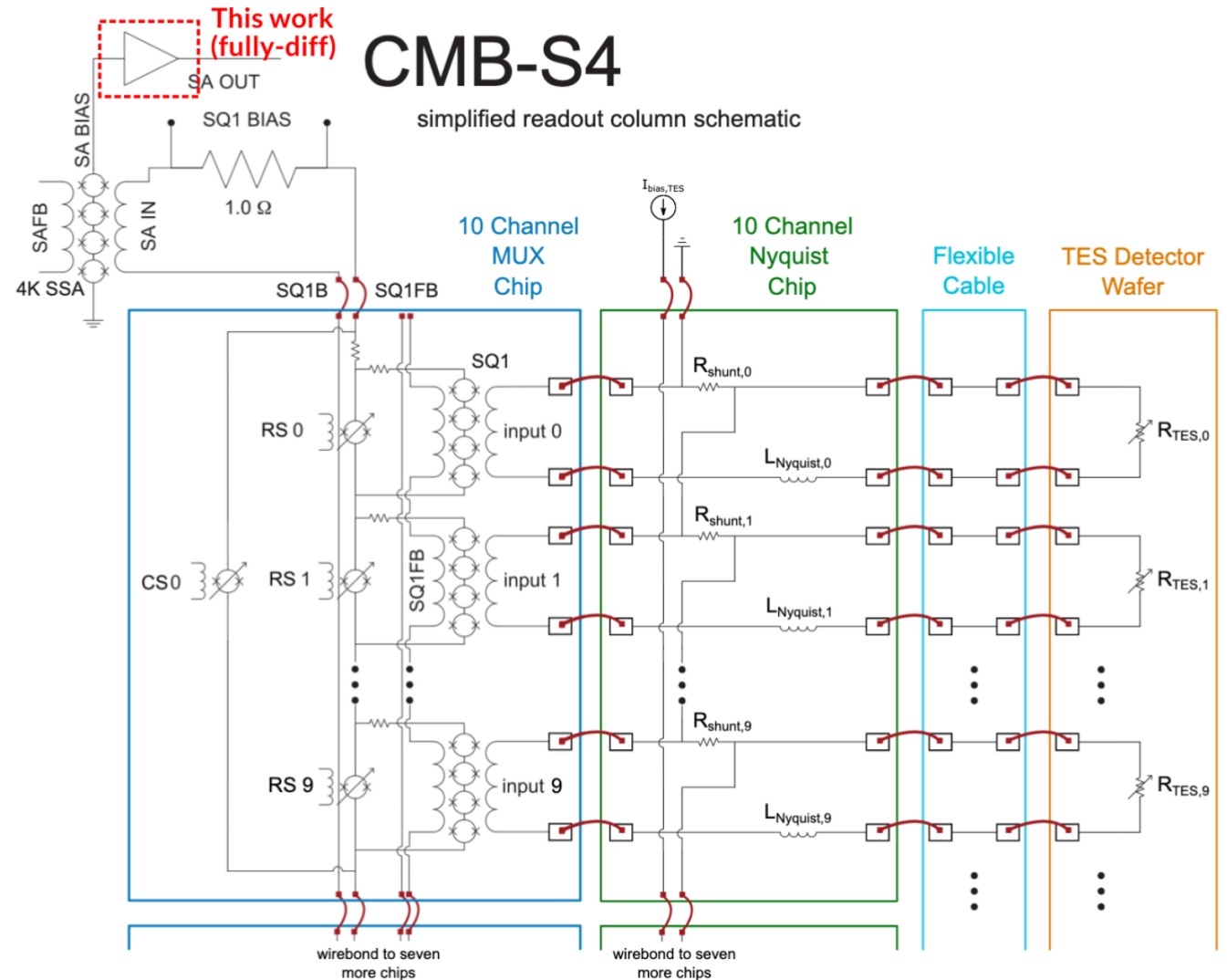
* SQUID - Superconducting Quantum Interference Device is an ultra-sensitive device that detects tiny magnetic fields using superconducting principles



System overview

- Multiple signals, with components of interest in the 0.1 – 100 Hz range, are multiplexed to the SSA*
- Amplification is needed given their low amplitude ($< 100 \mu\text{V}$)
- $\text{BW} \propto$ number of signals that can be multiplexed
- Power consumption sets how many Cryo amplifiers can coexist

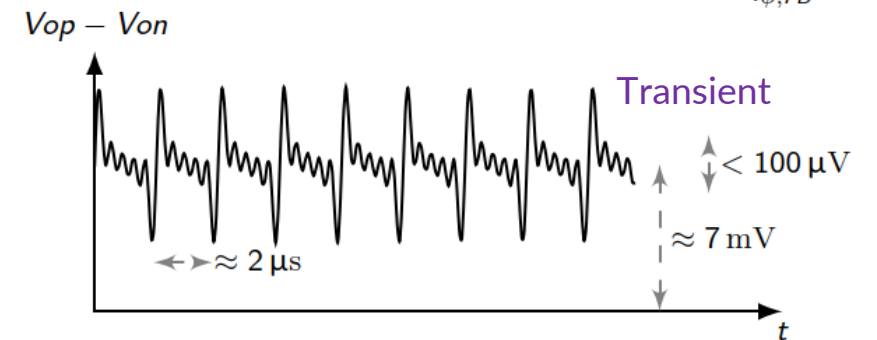
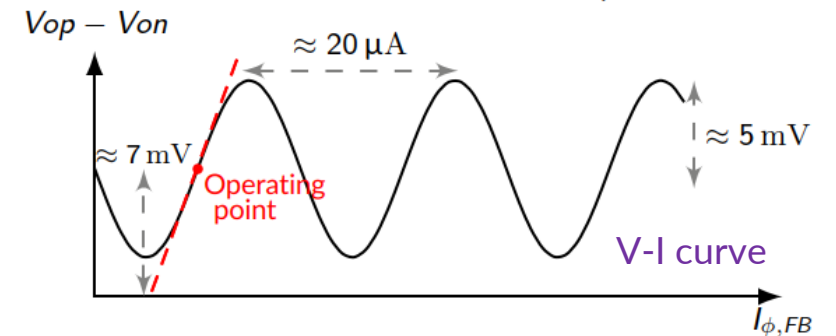
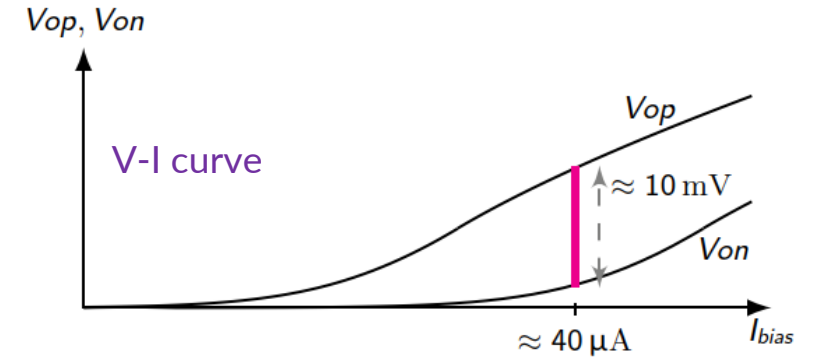
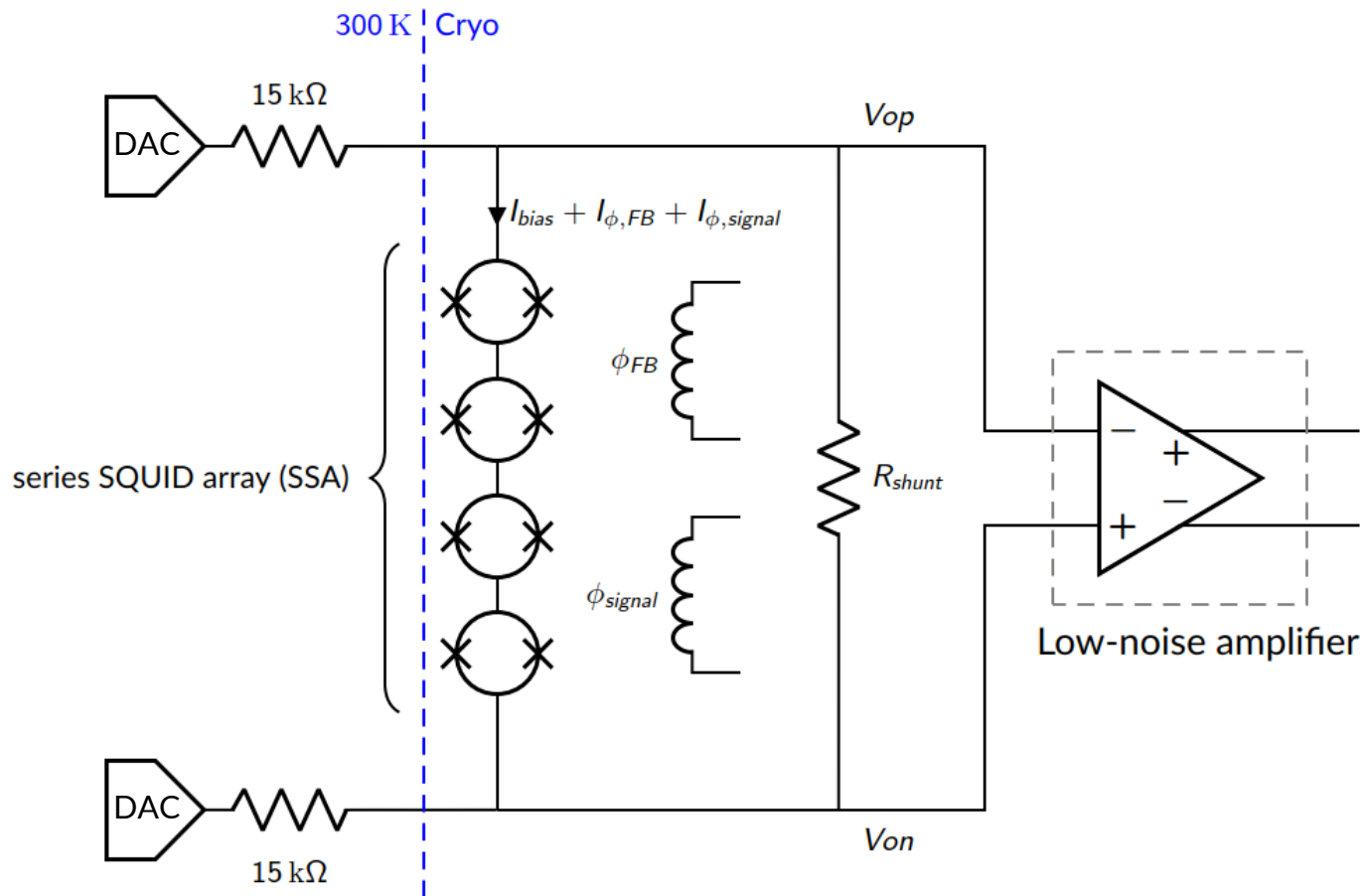
* SSA - Series SQUID Array



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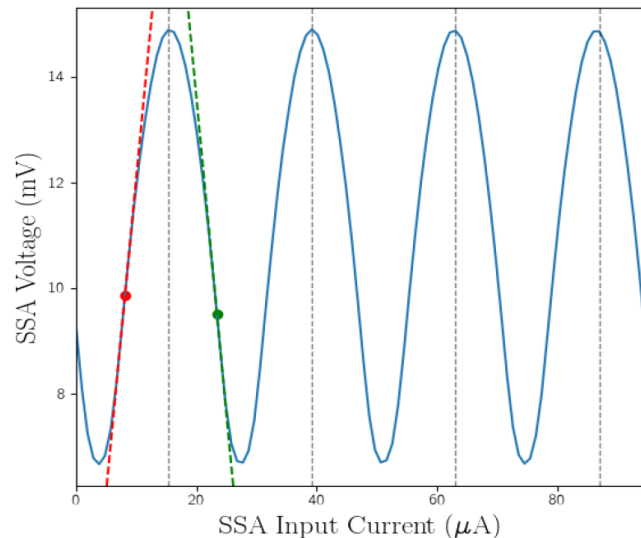
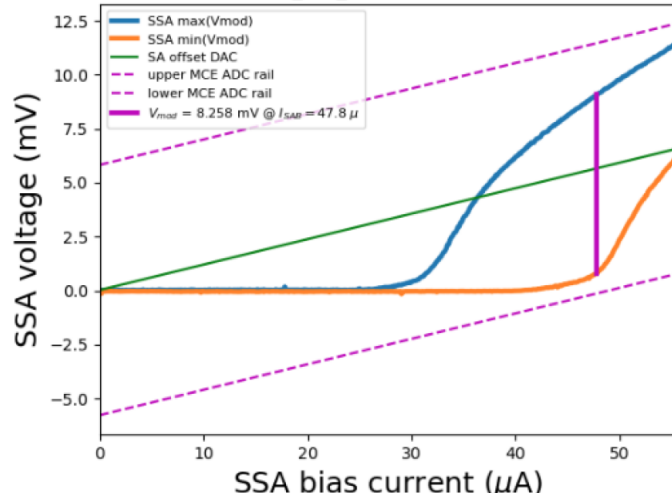
SQUID readout

SQUID readout: calibration phase



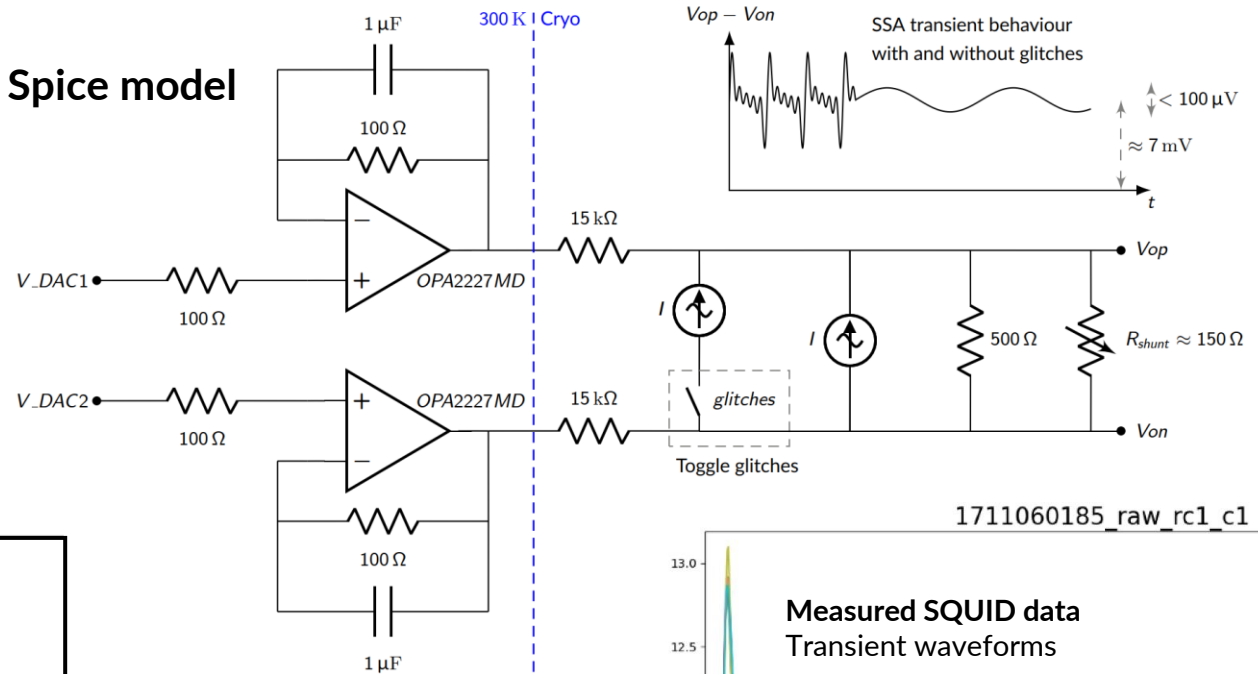
SQUID readout: measured data and spice model

03/18/24 : SLAC DR cooldown #39 SSA c0 voltage vs bias
vs_sab_1710800261.log

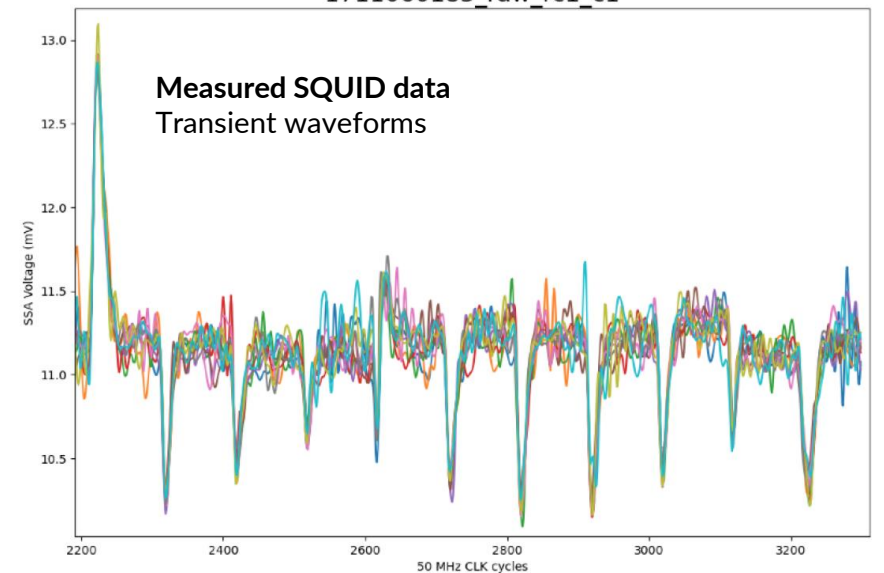


Column 0	
<u>Measured</u>	
I_{SSA}^{bias}	$= 47.7 \mu A$
V_{mod}^{SSA}	$= 8.225 mV$
Φ_0^{SSAFB}	$= 35.8 \mu A$
M_{FB}^{SSA}	$= 57.7 pH$
$dV_{ADU}^{SSA} / dFB_{DAC}^{SSA}$	$\downarrow = -8.11$
$dV_{nV}^{SSA} / dFB_{\mu\Phi_0}^{SSA}$	$\downarrow = -28.69$
$ dI_{n,pA}^{SSA} / dV_{nV}^{SSA} $	$\downarrow = 0.83$
$dV_{ADU}^{SSA} / dFB_{DAC}^{SSA}$	$\uparrow = 8.02$
$dV_{nV}^{SSA} / dFB_{\mu\Phi_0}^{SSA}$	$\uparrow = 28.36$
$ dI_{n,pA}^{SSA} / dV_{nV}^{SSA} $	$\uparrow = 0.84$
<u>Assumed</u>	
nV/ADU	$= 707.5$
M_{nV}^{SSA}	$= 86.5 pH$
$SSAFB nA/DAC$	$= 7.166$
R_{cable}^{cryo}	$= 123.6 \Omega$
$R_{roundtrip}$	

Spice model



1711060185_raw_rc1_c1

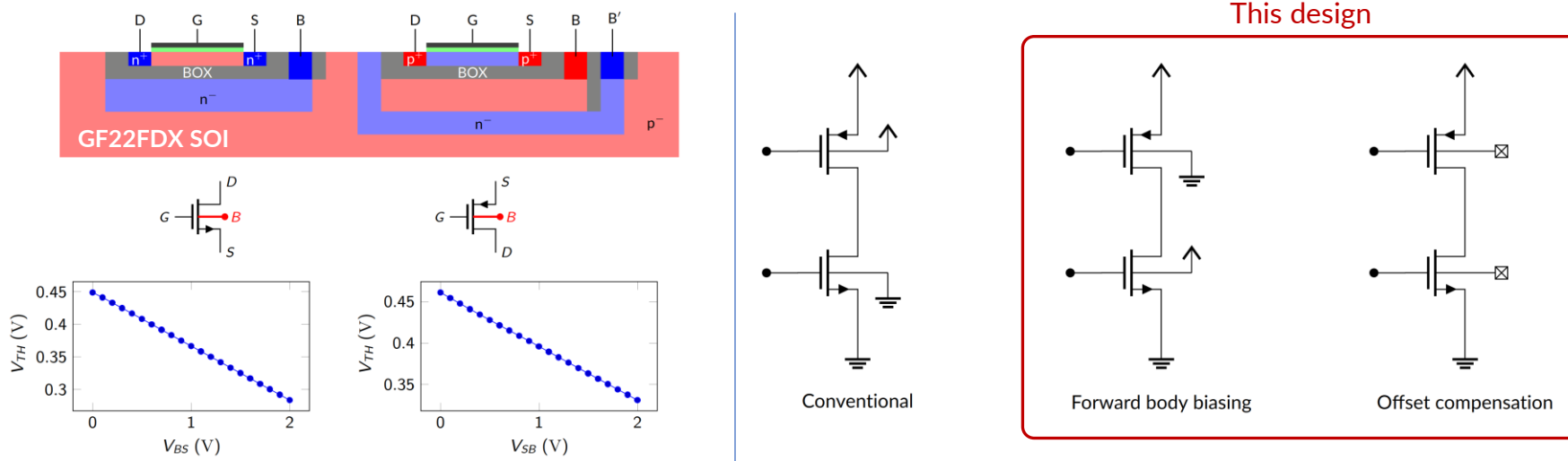


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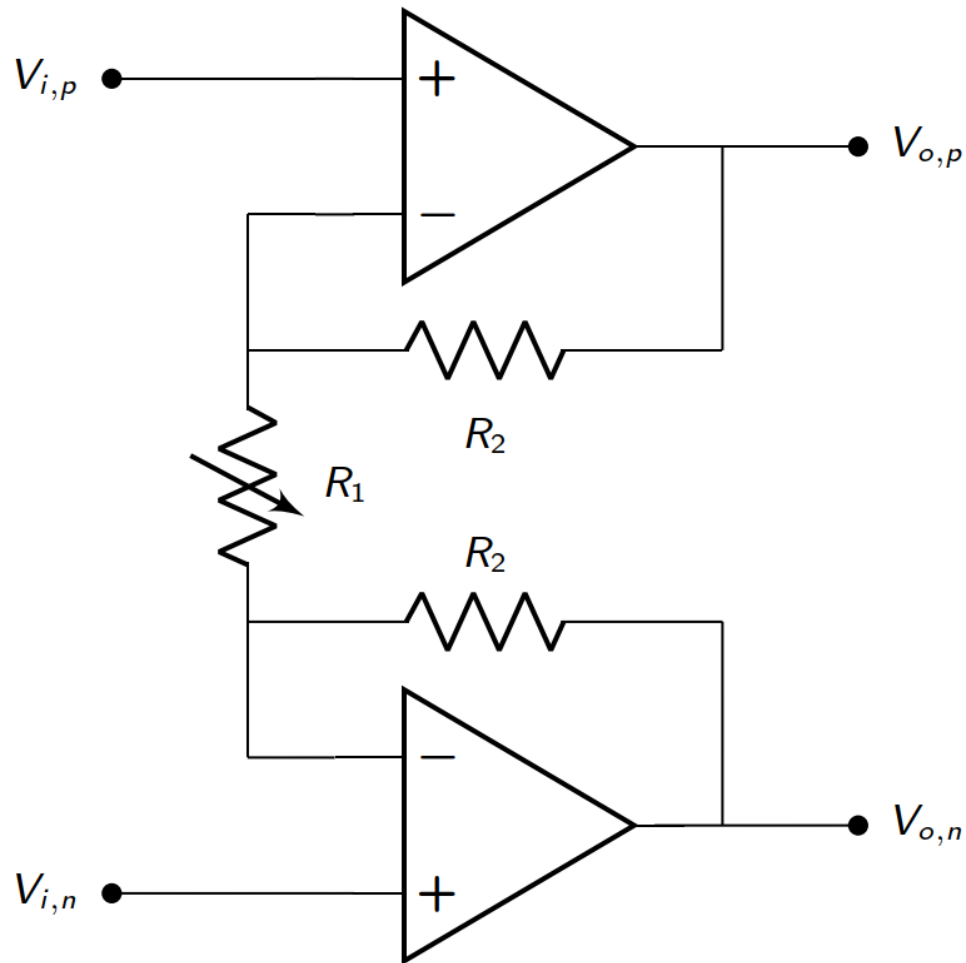
Amplifier specs and architecture

Key specifications

Metric	Target	Comment
Technology	GF22FDX FDSOI	GlobalFoundries 22 nm
Temperature	4 K	300 K operation should be achieved too
Supply voltage	0.8 V	Nominal GF22FDX voltage
Power consumption	< 1 mW	Cryocooler power budget at 4 K \approx 1 W, this is R&D
Bandwidth	> 1 MHz	Sets the number of multiplexed sensors, can be relaxed
Amplification	[20, 600]	{20, 50, 100, 150, 200, 300, 600}
Noise	< 0.3 nV Hz ^{-0.5}	Key metric
Input signal	\approx 7 mV (DC) \pm 100 μ V (AC)	AC component < 100 μ V



Architecture: instrumentation amplifier (INA)



Why an INA?

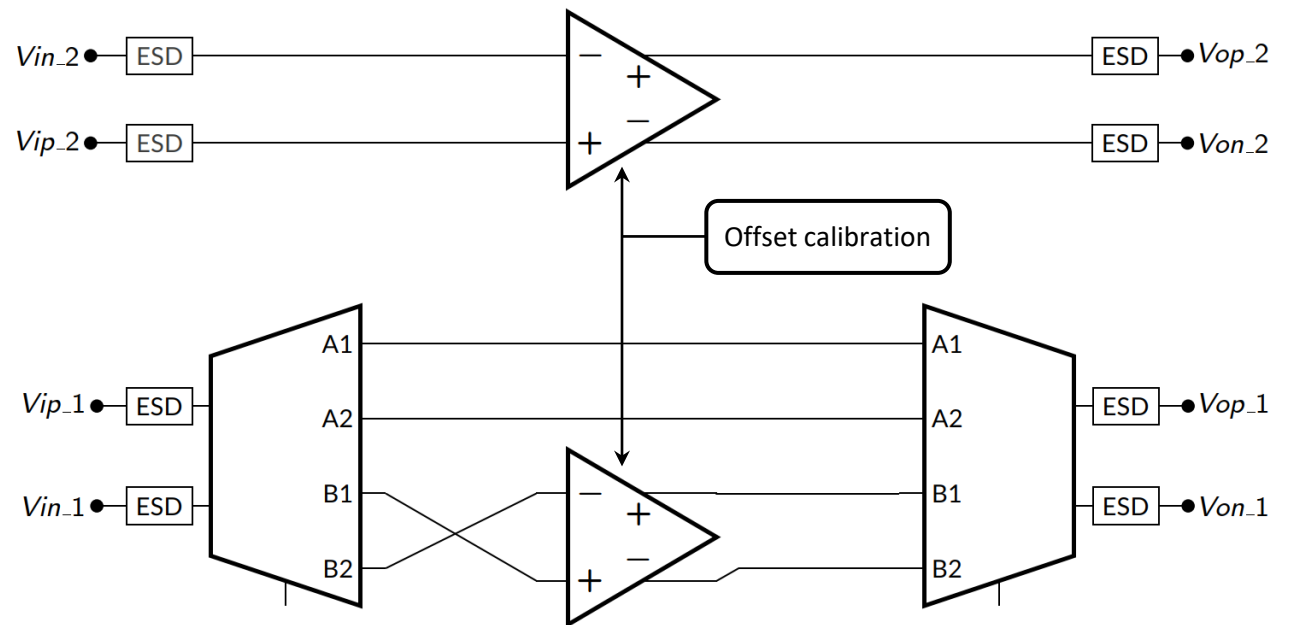
- High input-impedance → negligible effect on the SQUID operating point
- Programmable gain
 - $A_v \approx 1 + R_2 / R_1 \rightarrow$ robustness and tunability
- Fully-differential
- No common-mode feedback (CMFB)
- Relatively low-power

Key considerations at 4 K

- Aim for a simple circuit implementation
- Programmability and design for risk mitigation
- Design for a wide temperature range

Architecture: channel configuration

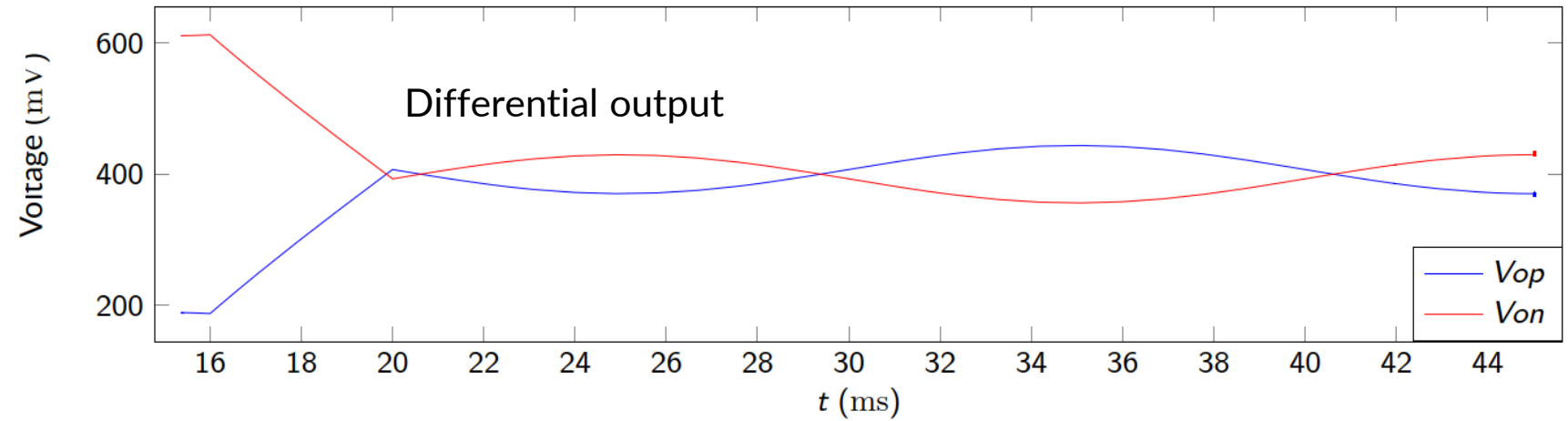
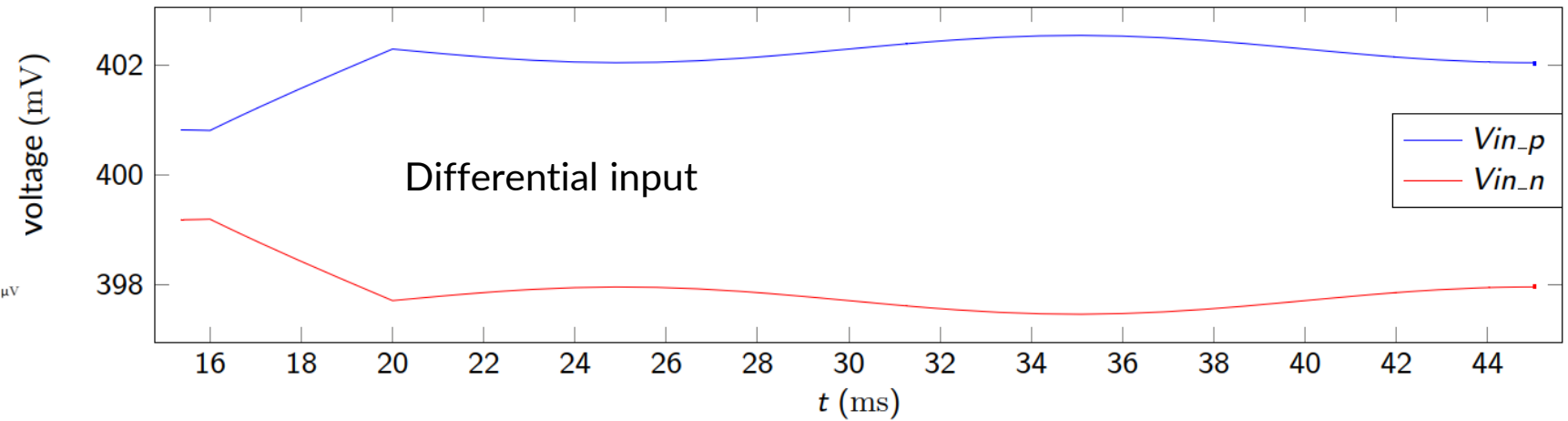
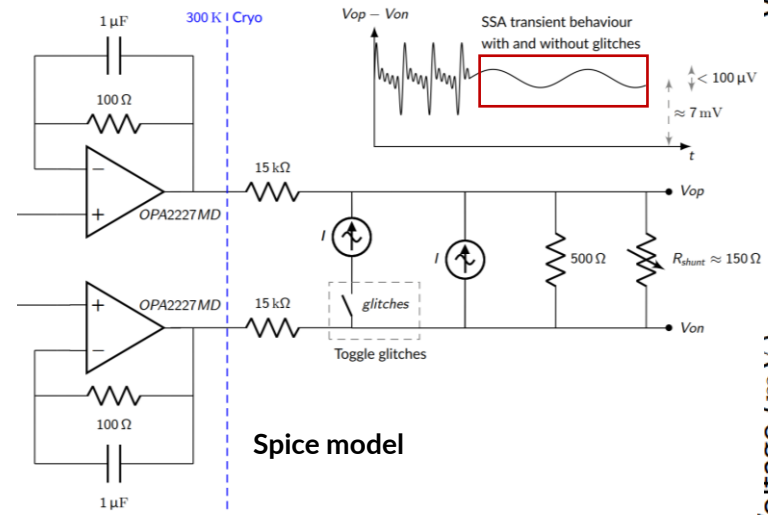
- Dual-channel preamplification stage for SQUID readout:
 - 1 INA is always attached for continuous operation
 - 1 INA that can be bypassed, enabling calibration of the SSA with room-temperature electronics
- On-chip multiplexing can eventually support multiple SSA channels
- Input/output ESD protection
- On-chip offset calibration



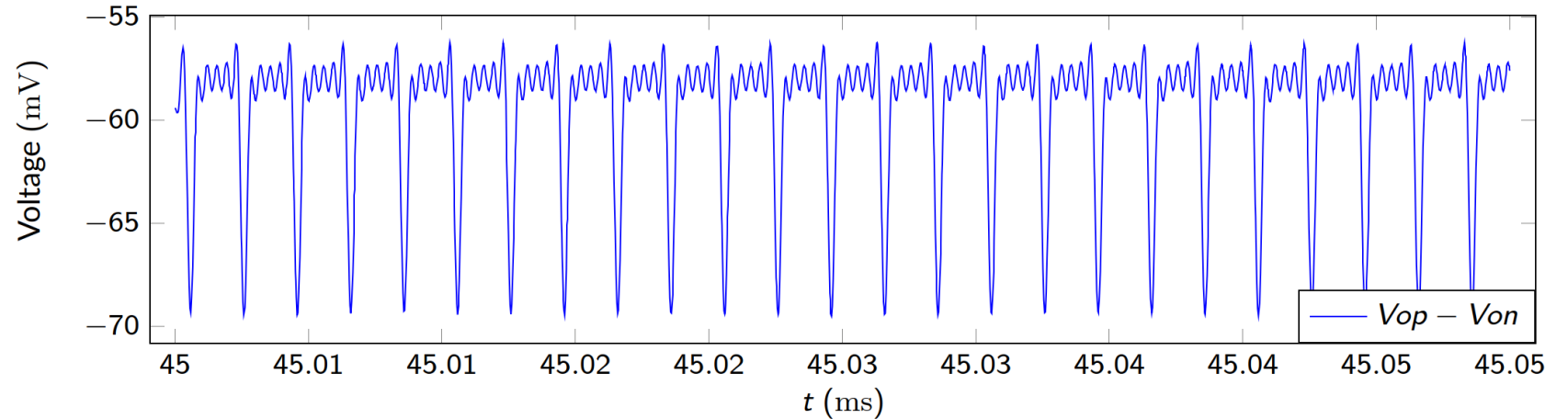
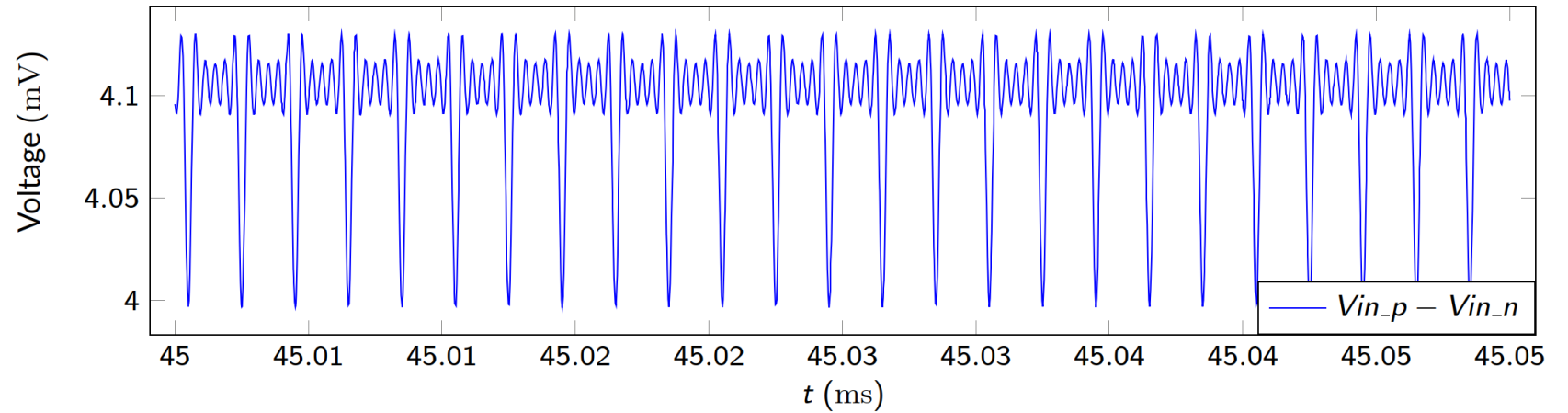
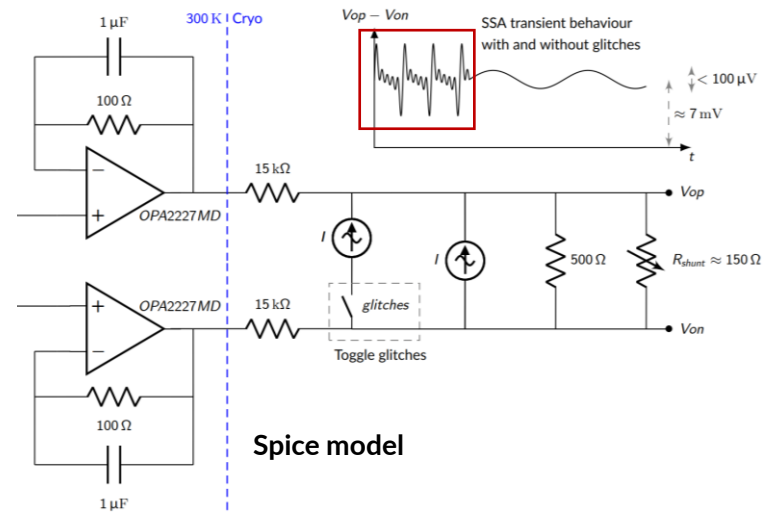
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Simulation results

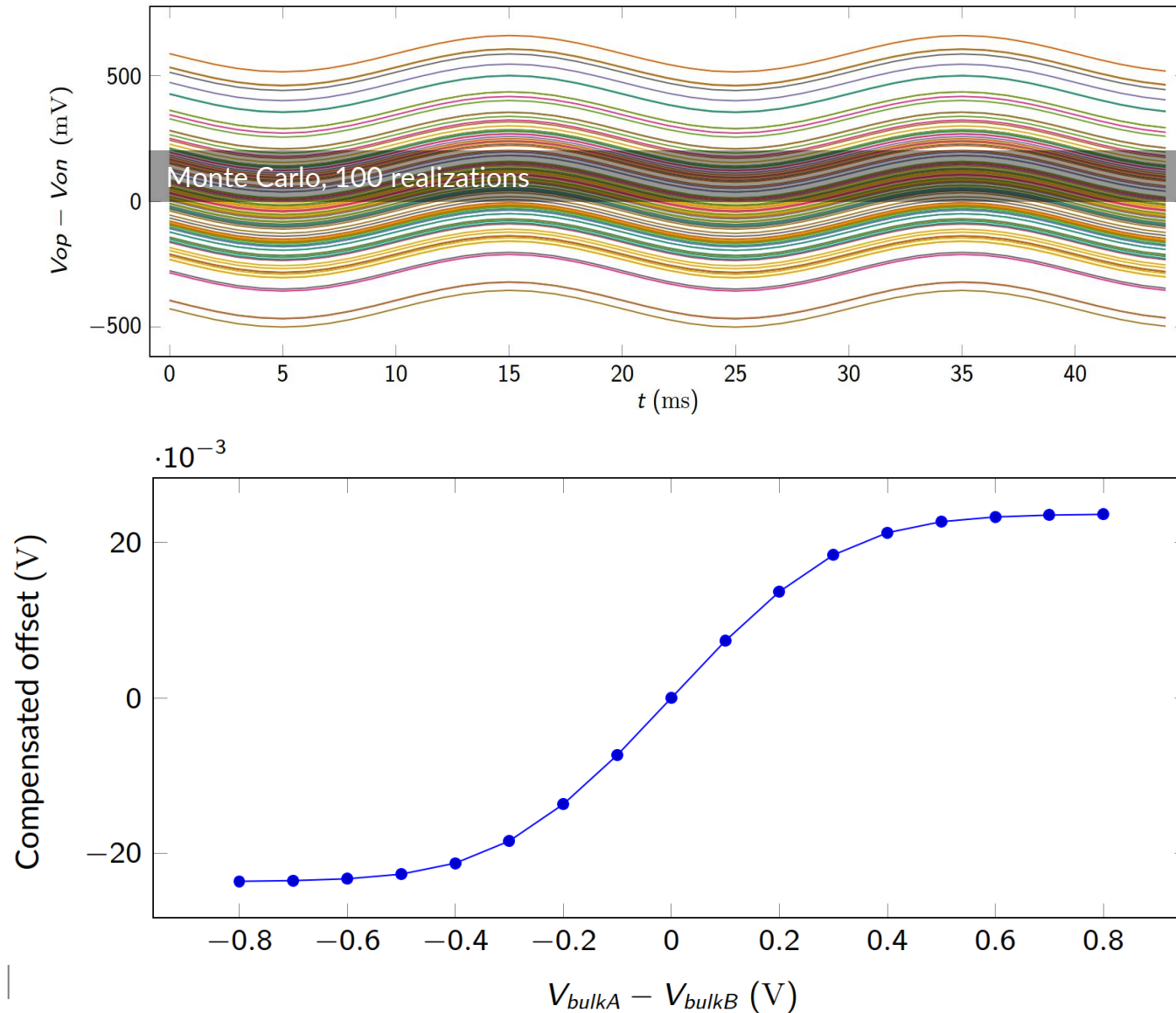
Simulation results: amplification & offset calibration (70K)



Simulation results: glitches amplification (70 K)



Simulation results: $\pm 23.57\text{mV}$ offset calibration (70 K)



Simulation results

SS, SF, TT, FS, FF corners, default settings, 0.8 V supply, 70 K + noise extrapolation:

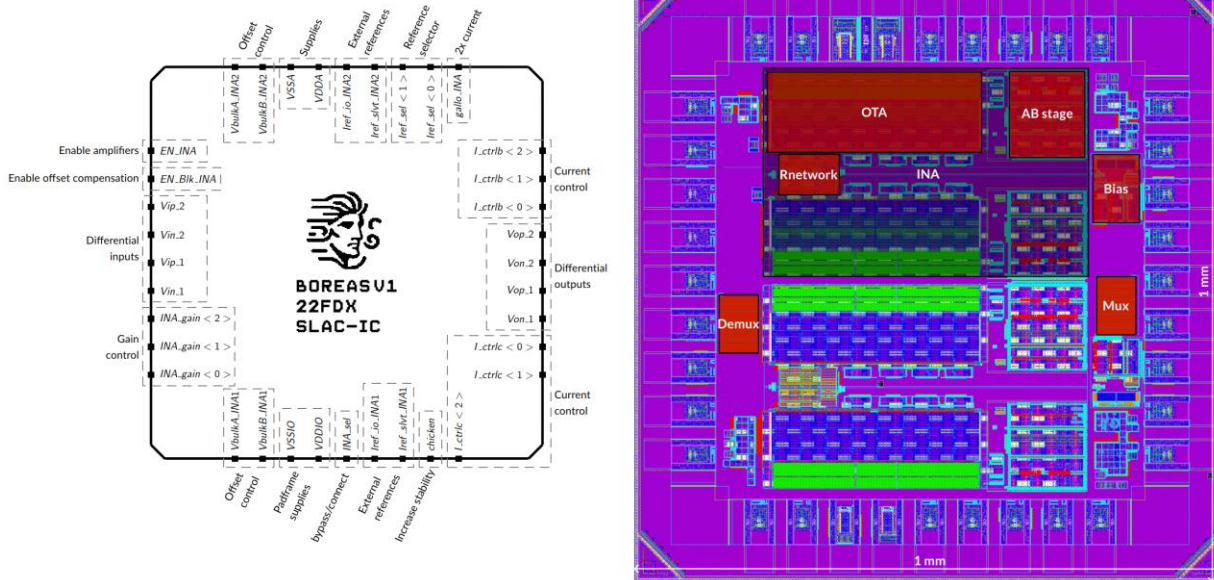
Metric	Target	min	TT	max
Power consumption	< 1 mW	1.22 mW	2.19 mW	3.46 mW
Bandwidth (BW)	> 1 MHz	1.24 MHz	1.36 MHz	1.42 MHz
Noise ($S_{n,in}$) [†]	< 0.3 nV Hz ^{-0.5}	0.359 nV Hz ^{-0.5}	0.367 nV Hz ^{-0.5}	0.377 nV Hz ^{-0.5}
Amplification	150	147.5	147.5	147.9
Differential PM	> 60 deg	83.36 deg	86.24 deg	88.36 deg
Offset compensation		±23.49 mV	±23.57 mV	±23.65 mV

[†] removed noise contribution from SQUID model and R_{shunt} .

miniASICs: Boreas and Vesper

Boreas

Dual Channel Amplifier in GF22FDX SOI

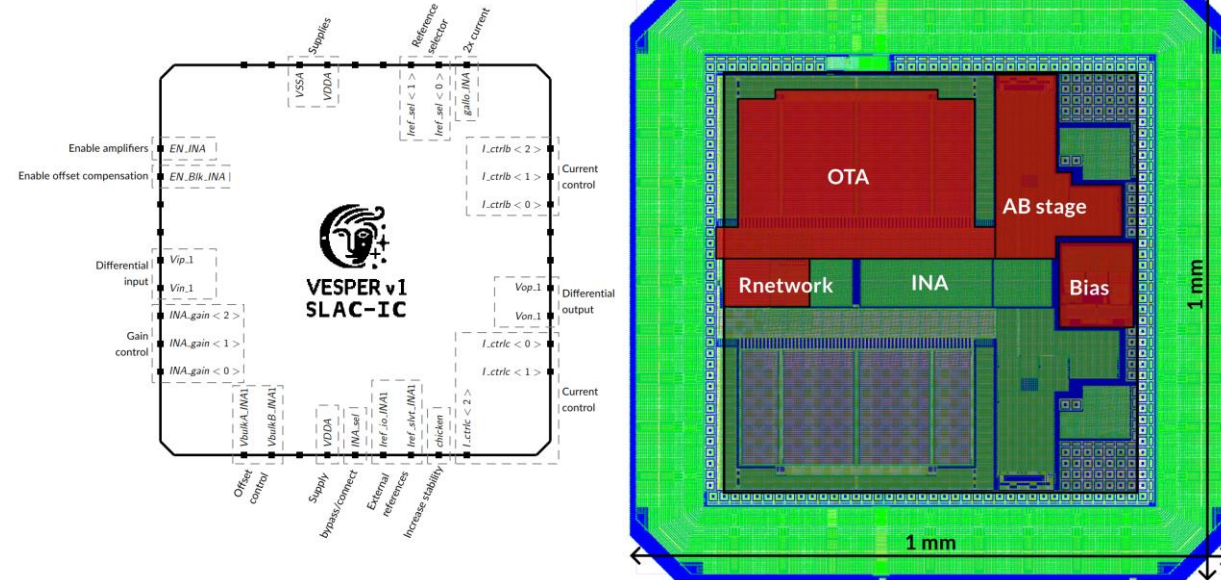


BOREAS is the **God of the Violent North Wind** in Greek mythology

- B** - **Broadband** (MHz bandwidth operation)
- O** - **Outstanding** (Amplification by a factor of 100 or more)
- R** - **Refrigerated** (Operates at 4 Kelvin, cryogenic temperature)
- E** - **Efficient** (Consumes very low power)
- A** - **Amplifier** (Small noise amplifier for SQUID signals)
- S** - **SQUID-compatible** (Fits into the CMB-S4 project)

Vesper

Single Channel Amplifier in 28nm (backup solution)



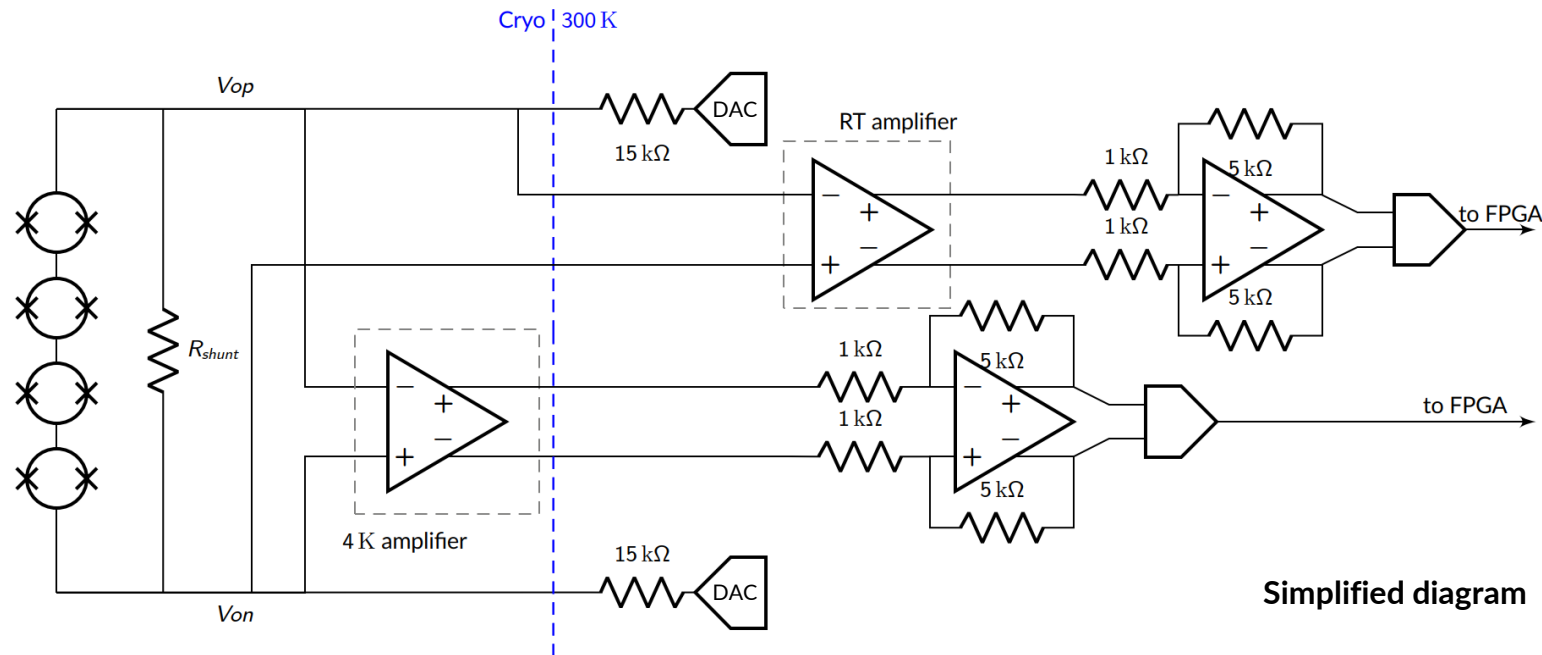
VESPER is the **God of the Evening Star** in Greek mythology and **brother of Boreas**

- V** - **Very-low-noise** (300pV/sqrt(HZ))
- E** - **Efficient** (Amplification by a factor of 100 or more)
- S** - **SQUID**
- P** - **Precision** (Tunable gain level, feedback stability)
- E** - **Enhanced** (Boosting modes)
- R** - **Read-out Amplifier** (SQUID read-out)

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System interface

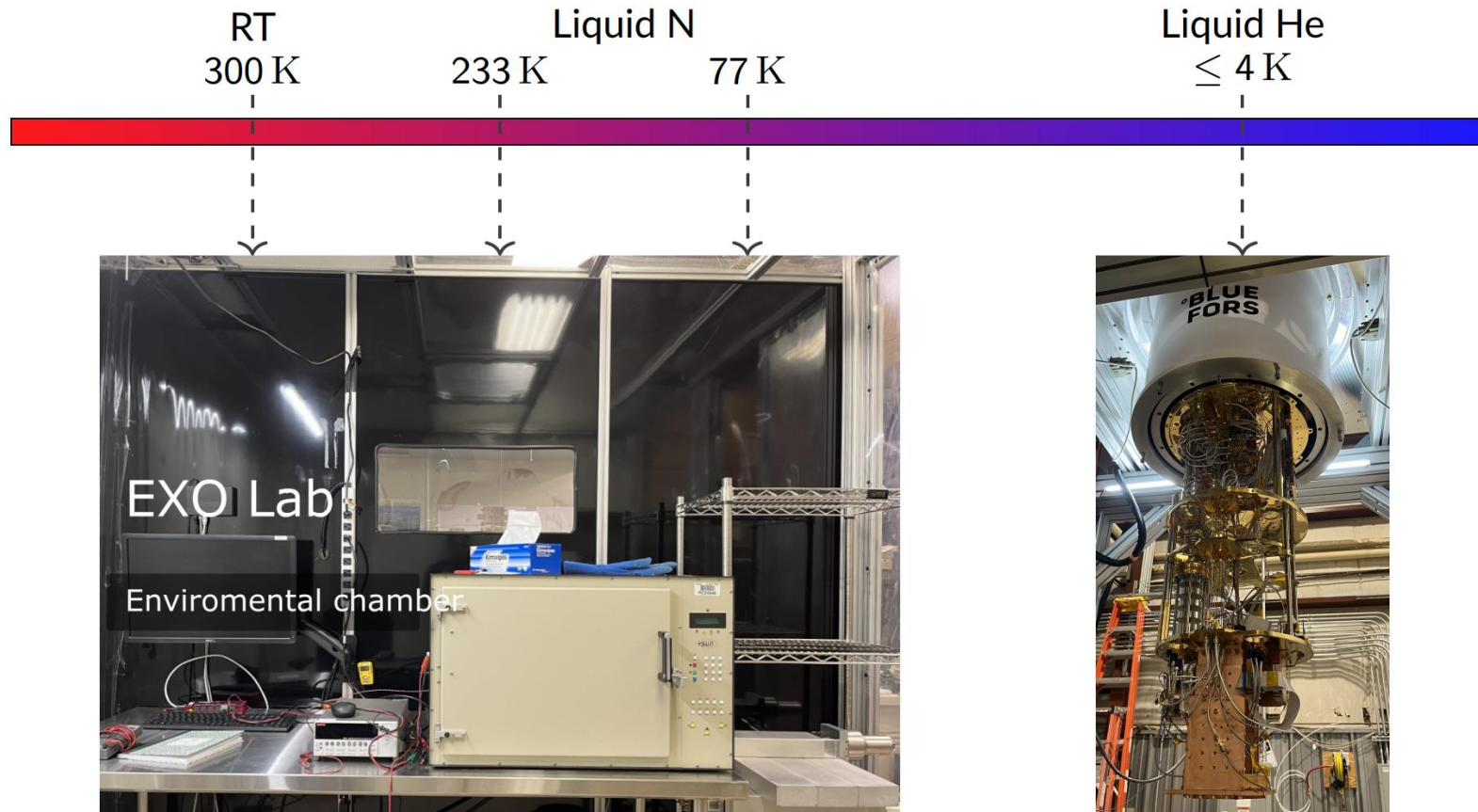
System interface



- The 4 K amplifier requires a differential signal from the SSA configuration
- Proper biasing via external DACs set the common-mode input voltage
- The 4 K amplifier outputs interface with an external ADC driver
- Parallel operation with the warm electronics is anticipated for comparison purposes

Timeline and upcoming testing

- MiniASICs estimated arrival: early to mid-December 2024
- Projected start of testing: early 2025



Thanks!!

References

- [1] Kevork N. Abazajian et al. *CMB-S4 Science Book, First Edition*. 2016. arXiv: 1610.02743 [astro-ph.CO]. URL: <https://arxiv.org/abs/1610.02743>.
- [2] D. R. Barron et al. *Conceptual Design of the Modular Detector and Readout System for the CMB-S4 survey experiment*. 2022. arXiv: 2208.02284 [astro-ph.IM]. URL: <https://arxiv.org/abs/2208.02284>.
- [3] Lawrence Berkeley National Laboratory. *Lead Lab Selected for Next-Generation Cosmic Microwave Background Experiment*. Accessed: 2024-08-19. 2020. URL: <https://www.interactions.org/press-release/lead-lab-selected-next-generation-cosmic-microwave>.

Backup Material

Challenges & design strategy (I)

- **4 K operation and no cryogenic models:**
 - Design for a wide temperature range and run simulations across corners
 - Include control bits
 - Extrapolate noise to compare against spec
- **Very low noise:**
 - Size large OTA (first stage) transistors
 - Add decoupling capacitors at critical nets both on-chip and off-chip
- **Input offset:**
 - Design an offset compensation mechanism.
 - Risk mitigation: control bit to toggle offset compensation ON/OFF.
- **Stability:**
 - Implement a compensation technique that leverages the Miller effect.
 - Implement a chicken bit to increase phase margin (PM) at the cost of bandwidth (BW).

Challenges & design strategy (II)

- **Robustness:**
 - Pursue a simple design
 - Include programmability to achieve a reliable operation, high performance and low power
- **SQUID readout:**
 - Review the literature (sensor behavior, application, specifications)
 - Implement a model with a reasonable transient behavior
 - Design an amplifying stage with a high-input impedance
- **System-level integration:**
 - Characterize the 4 K-300 K cable
 - Review the existing room-temperature electronics and check the 4 K amplifier can be biased properly
 - Influence the ADC driver configuration so that the ASIC can drive it

Boreas pinout

