

Characterization of the MetaRock fast timing analog front end for future HEP experiments

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Z. Zhang, K. Caisley

CPAD 2024, Knoxville TN

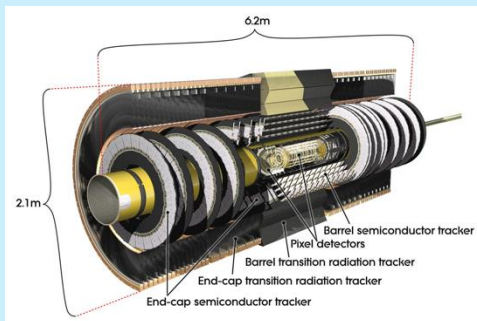
20 November 2024



4D Tracking

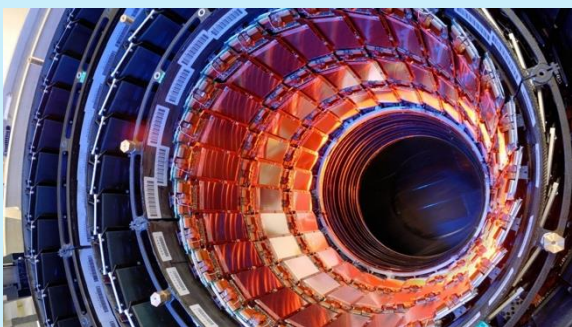
- High granularity and fast timing detectors exist, 4D Tracking refers to the merger of high granularity and fast timing.

Spatial Resolution



**ATLAS Inner
Detector**

**CMS
Silicon
Tracker**



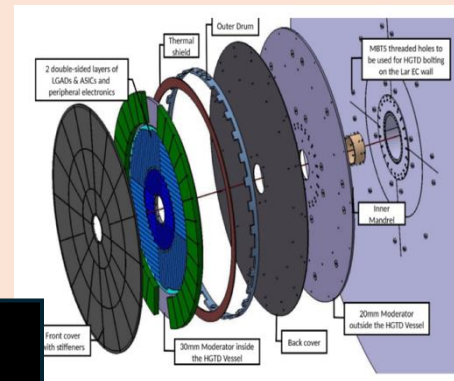
4D Tracking



HiLumi
HL-LHC PROJECT

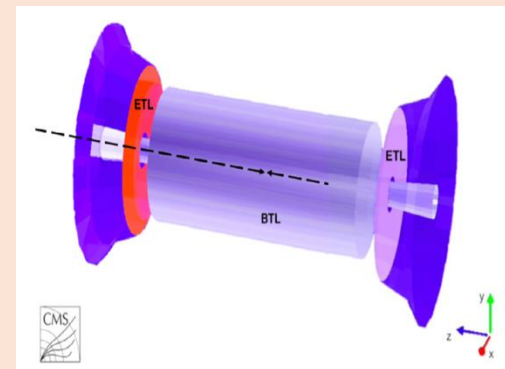


Timing Resolution



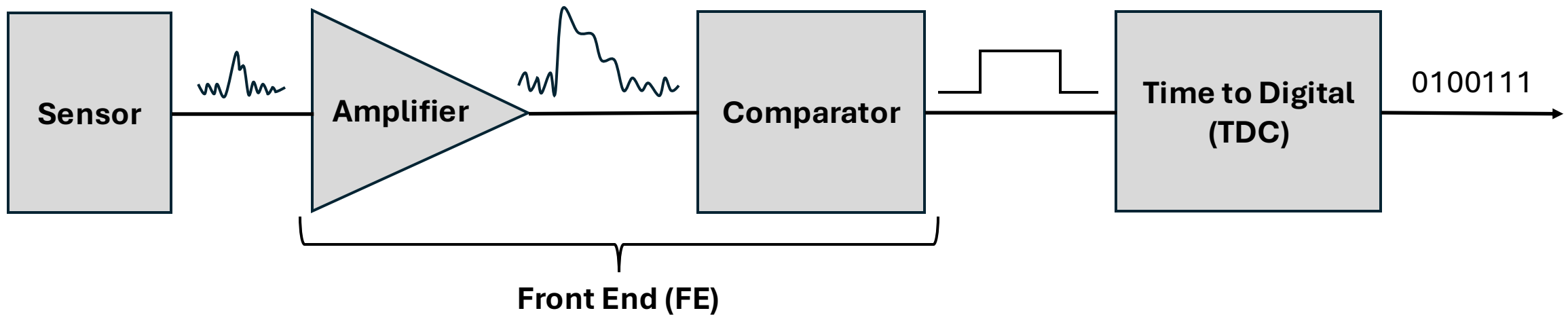
ATLAS - HGTD
30-50 ps / track

CMS - ETL
30-40 ps / track



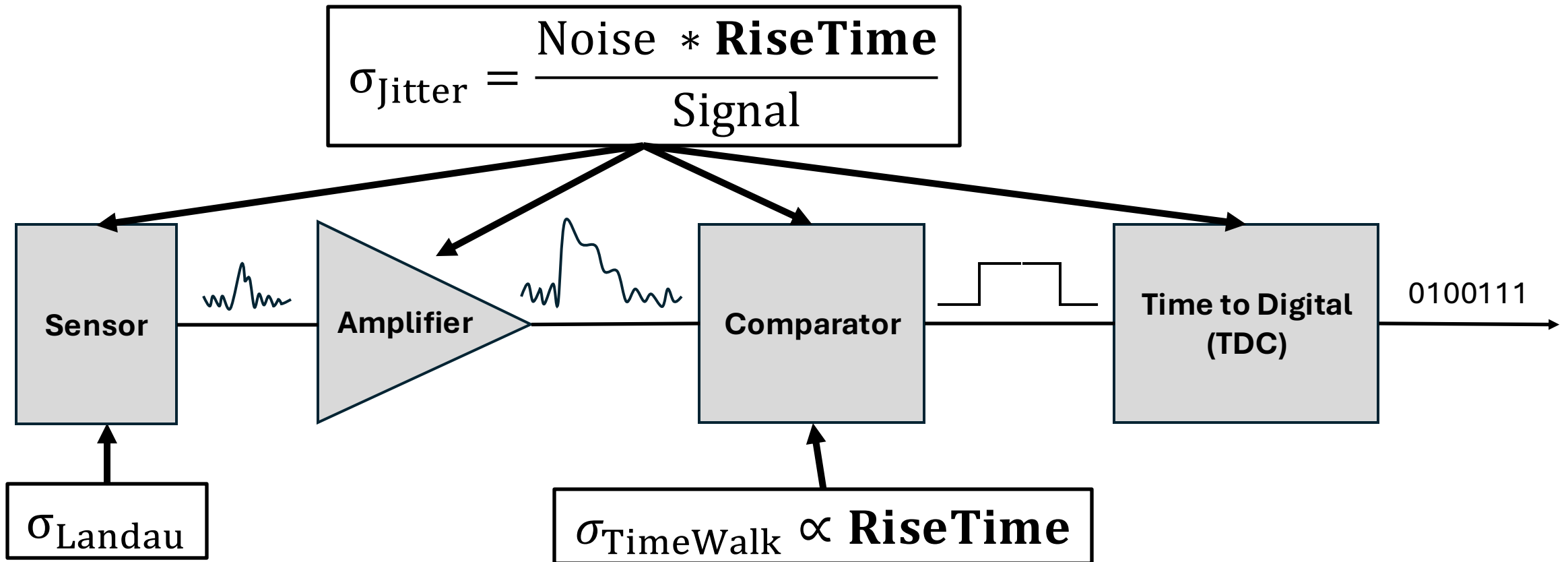
Prototyping Stages

- 4D Tracking is in the prototyping stages. There are many open questions:
 - Sensor Material – [T. Yang on SiC LGADs](#)
 - Sensor Structure – [H. Farook on LGADs](#) and [A. Gentry on Small Pith 3D Sensors](#)
 - Front End Design – [This Talk](#)
 - Time to digital converter (TDC) design – [B. Markovic on 28 nm TDC](#) and This Talk



Timing Resolution

- The sensor timing resolution has many contributions: jitter, Landau fluctuations, time walk...



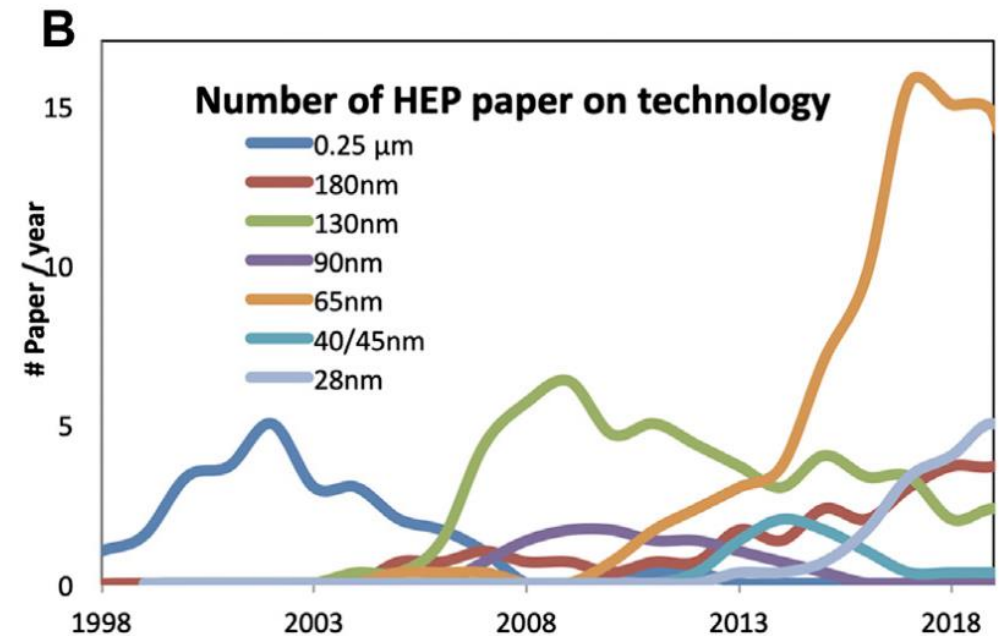
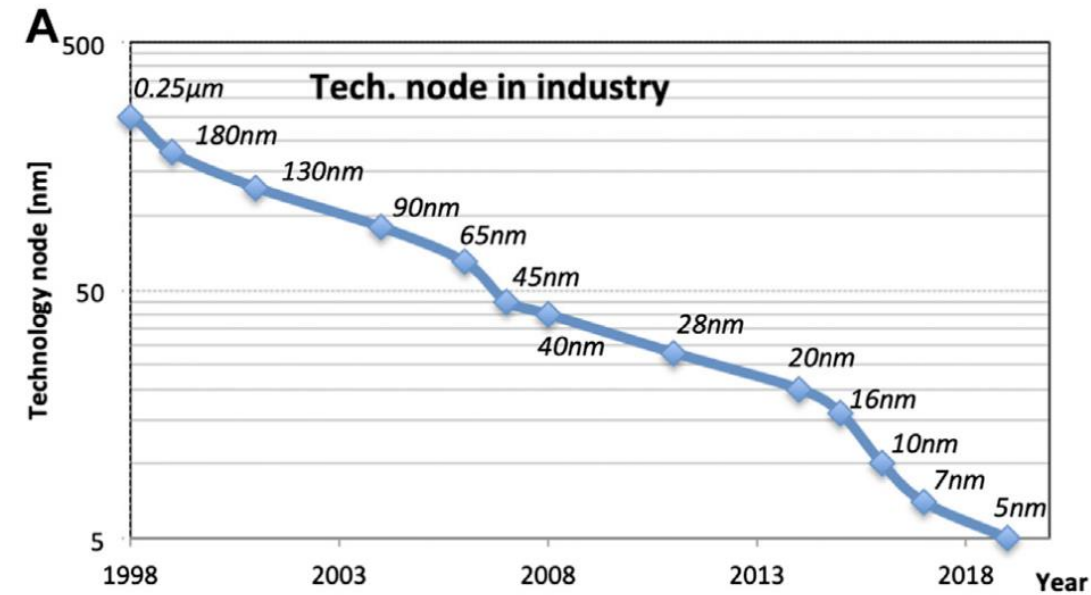
Constraints

- Collider experiments come with limitations that must be balanced with the timing resolution:
 - **Low Mass** – the mass in a detector increases back scattering and effects particle trajectories. Sensors, electronics, and infrastructure need to have as small of mass as possible
 - **Low Power** – power generates heat which must be removed from the detector volume to stay within operational temperatures. Lower power sensors means less heat generated, and therefore less mass needed for cooling.
 - **Small Area** – the sensor pitch must be small for good spatial resolution
 - **Hit Rate** – the sensor must be reset before the next particle arrives.

Variable	Target	Note
Time Resolution	$< 50 \text{ ps}$	at 3 ke^-
Analog Area	$35 \mu\text{m} \times 35\mu\text{m}$	Split with TDC analog component
Analog Power	$5 \mu\text{W}$	Split with TDC analog component
Threshold	1000 e^-	$100 \text{ e}^- \text{ ENC}$

28 nm CMOS

- Active LHC readout electronics are fabricated with the 65 nm CMOS technology. This study is on readout electronics fabricated in the 28 nm CMOS node.
- Migrating to a smaller node in the CMOS size provides several advantages:
 - Smaller propagation delays
 - Lower power
 - More logic per area
- Future collider experiments will demand more on chip processing, which makes having more logic per area a very attractive advantage of moving to smaller nodes.
- However, there are challenges with smaller nodes in HEP:
 - More contributions of parasitic capacitance
 - Unknown performance in high radiation environments



LBNL Front End Electronics Activities

- LBNL produced the **BigRock** and **Pebbles** ([Pebbles, CPAD2023](#)) chips in 28 nm.
 - charge injection circuit $100 e^-$ to $20 ke^-$
 - 16 channels with different input capacitances (0, 25, 50, 100 fF)
 - High-power TDC for characterization (20 ps)

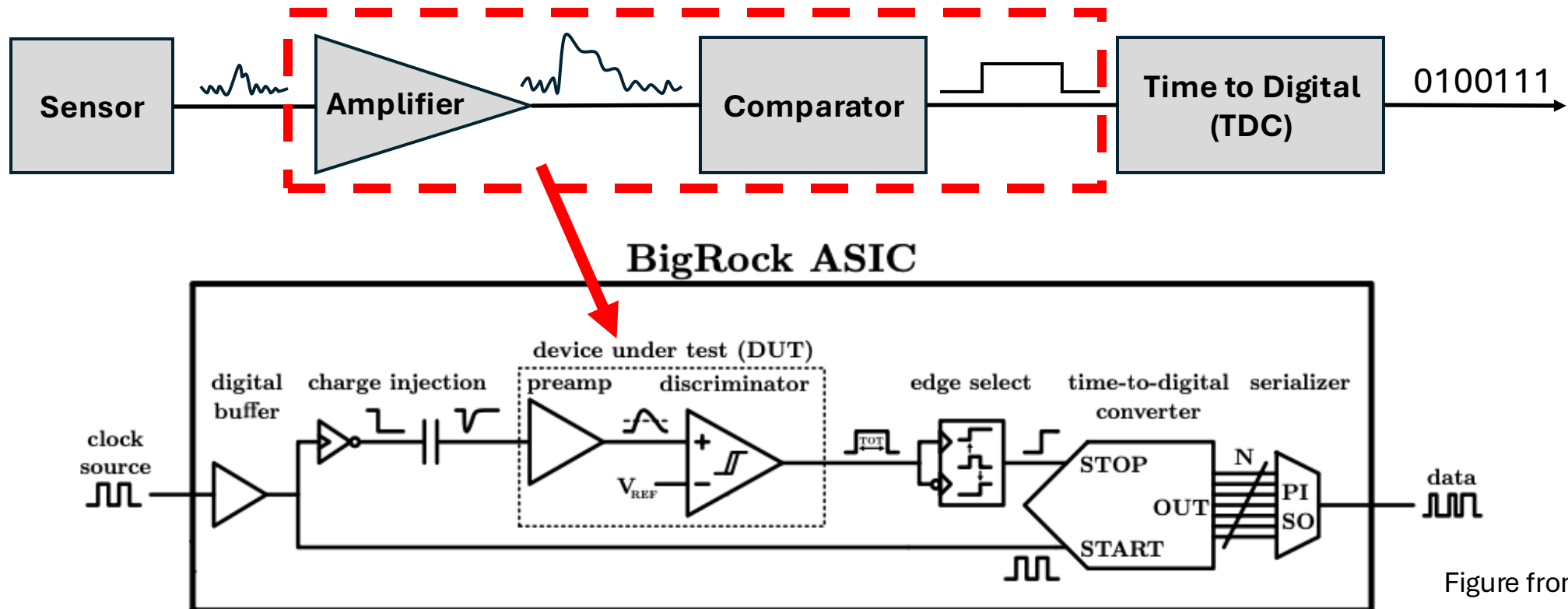


Figure from K. Caisley

LBNL Front End Electronics Activities

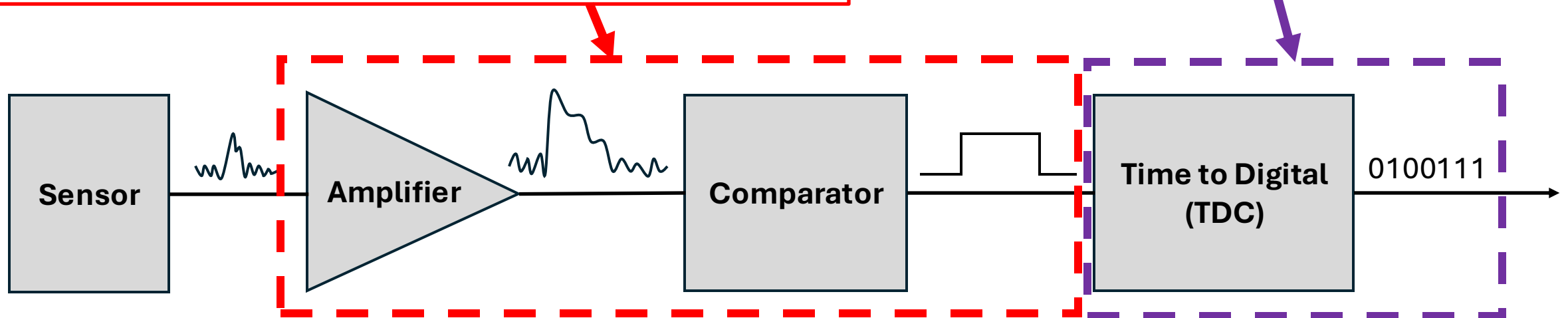
- **Meta Rock** is the successor of Pebbles

reduction of the **front end** parasitic capacitance by

- further minimizing some routing paths
- resizing the feedback FET smaller

Simulations suggest that this will improve the FE timing resolution from ~ 75 ps to ~ 55 ps for a 50fF channel

A prototype **low-power TDC** based on a time stretching technique



MetaRock Low-Power TDC

- The low-power TDC design is based on a 40 MHz clock.
- Two stages of time stretching are used to
- Time stretching costs signal conversion time, which should not exceed $\sim 2\mu\text{s}$, but it is low power and uses few components (small Area)

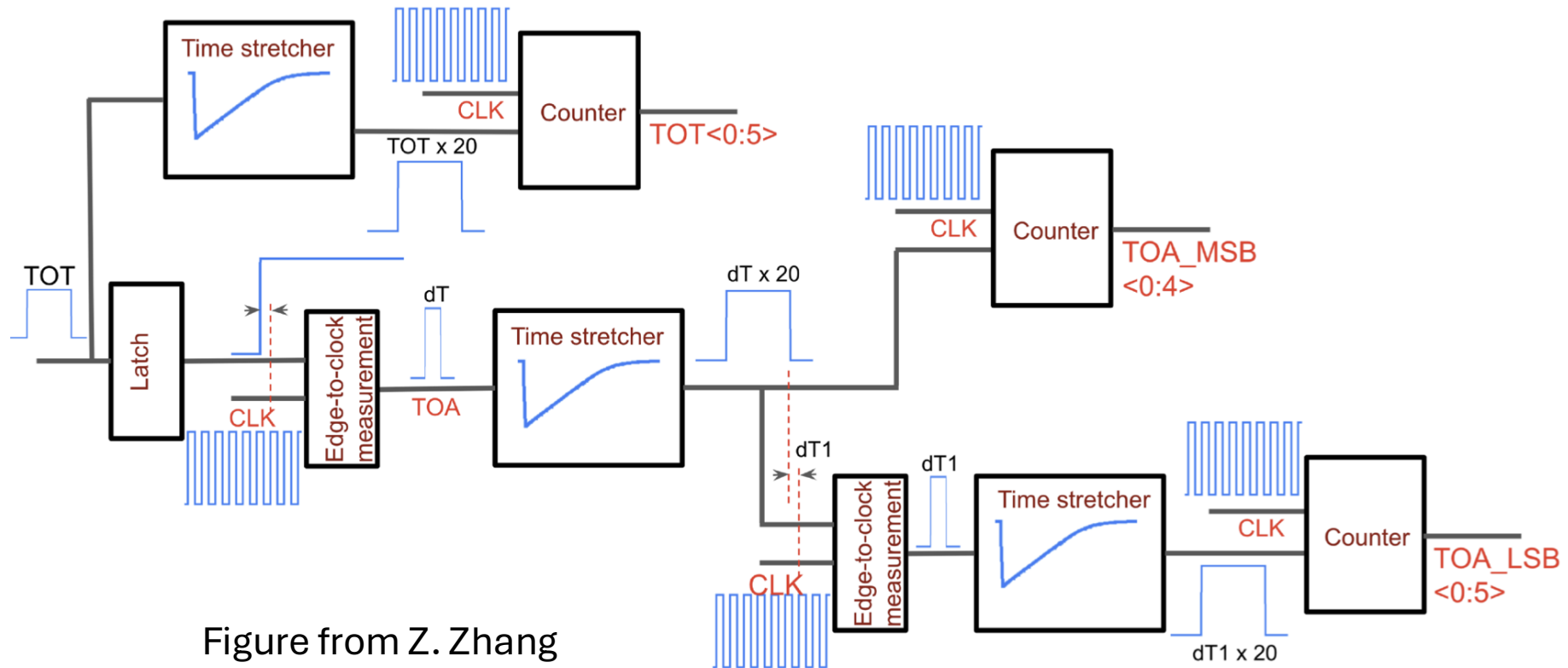
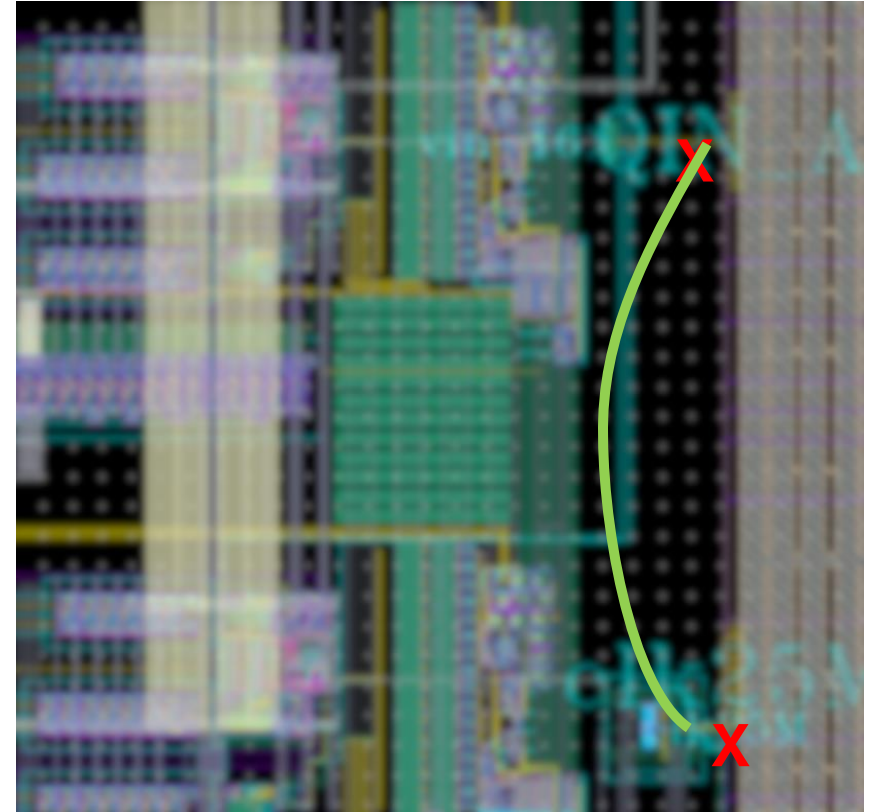


Figure from Z. Zhang

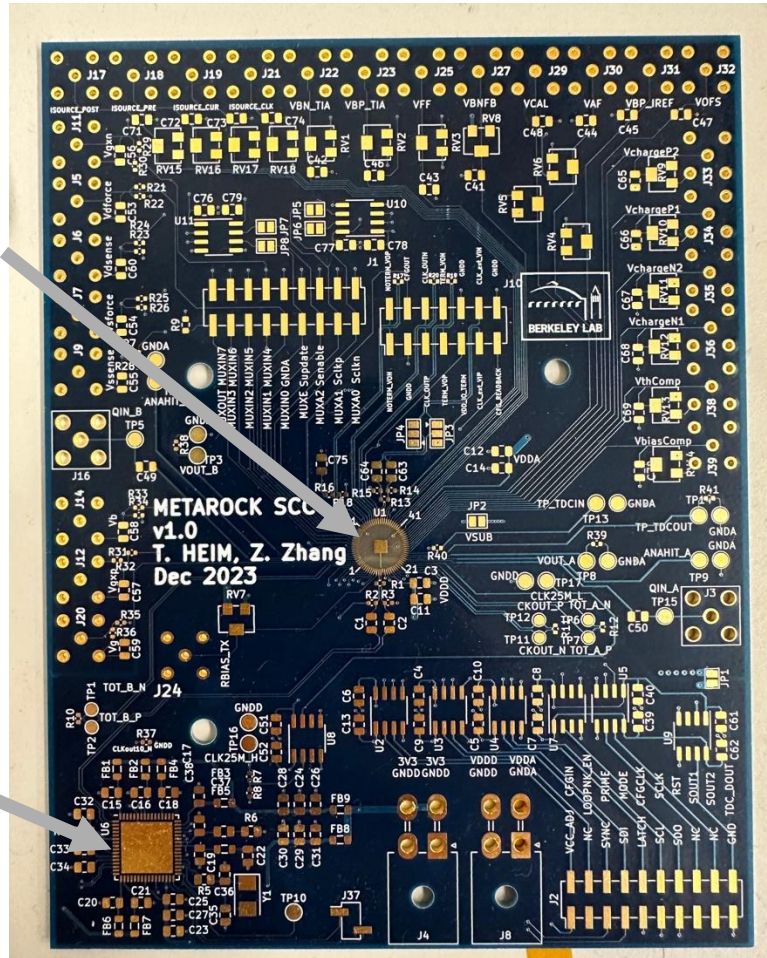
Problem with Low-Power TDC

- There is a short in the MetaRock chip between the 40 MHz clock (required for the low-power TDC) and VDDD (chip power).
 - An incorrect IO cell placement was not found with LVS as we did not have access to backend views at the time.
- Several chips underwent a Focused-Ion-Beam (FIB) technique to isolate the shorted pad and reroute the 40 MHz input to a different pad.
- The 40 MHz clock pad is rerouted to a pad used for external charge injection.



Test Setup

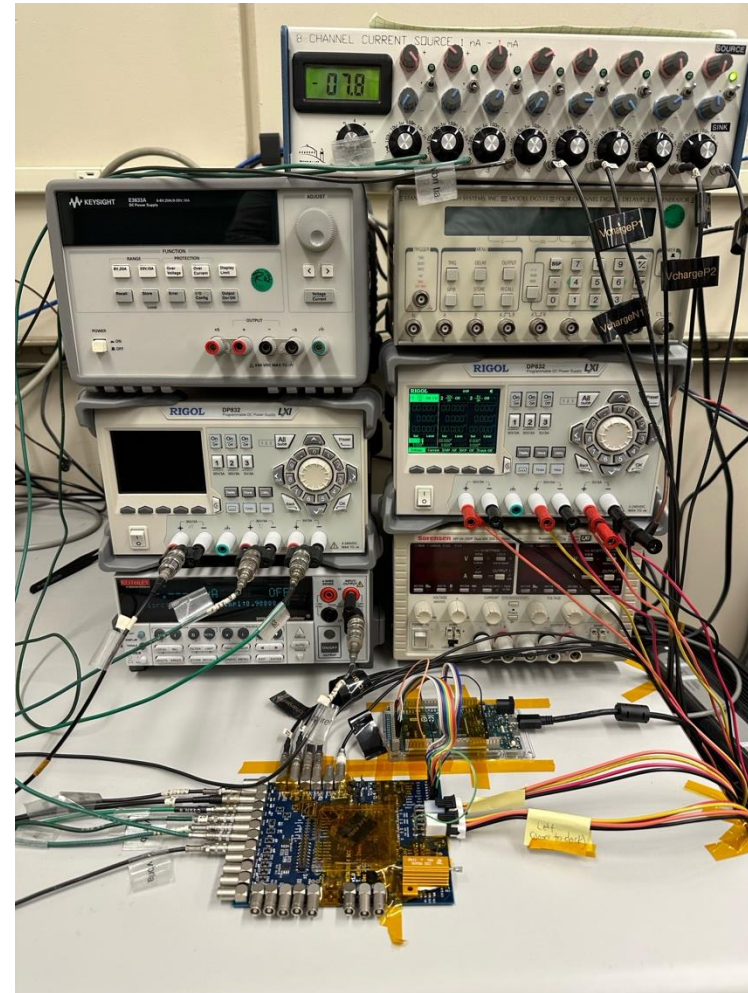
MetaRock PCB



MetaRock
Chip

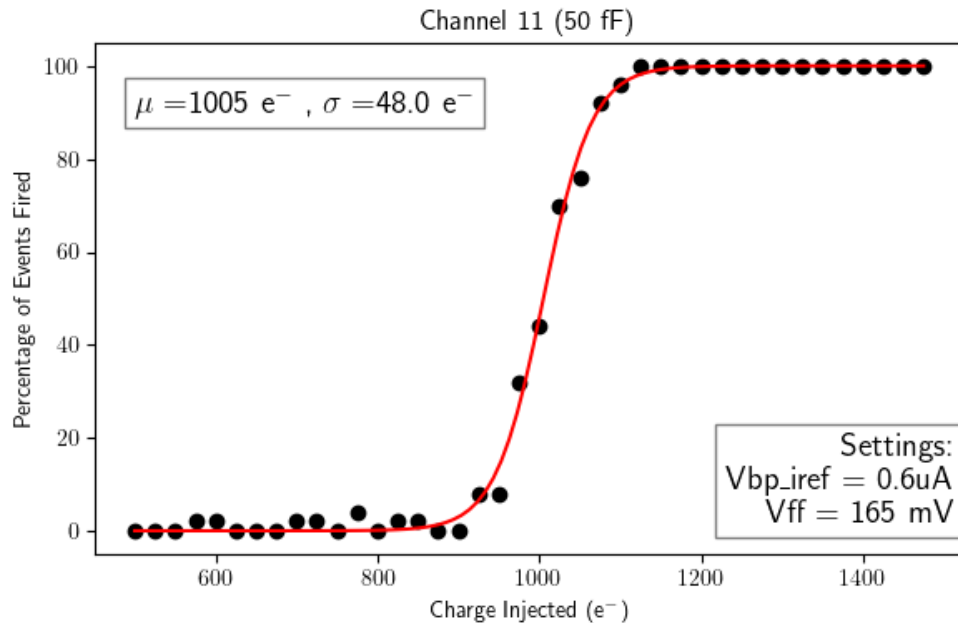
Low-jitter
clock

LBNL Test Setup



Noise Scans

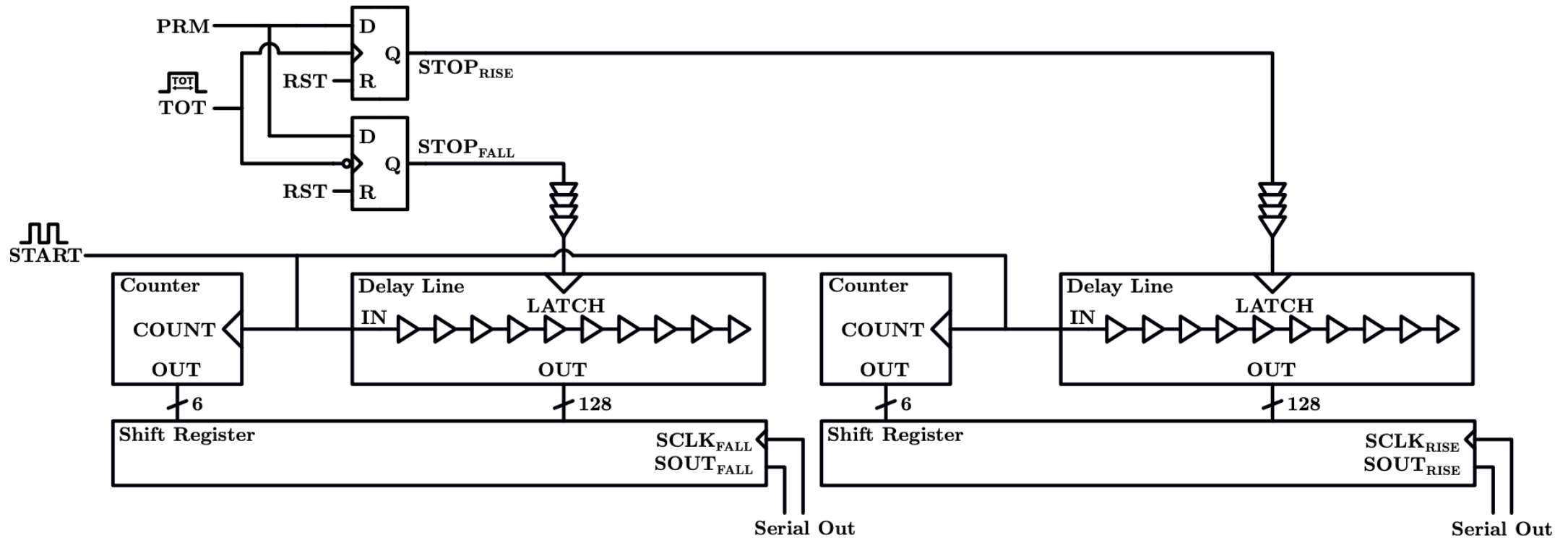
- The threshold is set to 1000 e⁻ and charge injection is scanned from 500 to 1500 e⁻.
- 100 injections are done at each charge, and the number of injections triggering preamplifier circuit are recorded.
- A fit to $F(Q) = 1/(1 + e^{-k(Q-\mu)})$ with $k = 4/\sqrt{2\pi * ENC}$ where ENC is the equivalent noise charge.
- This is repeated for each channel, and the results are tabulated below.



Channel	Capacitance [fF]	ENC [e ⁻]
3	0	63.1
4	0	60.5
5	25	72.2
9	25	73.5
10	50	59.1
11	50	60.0
12	50	69.7
13	50	48.0
14	100	92.6

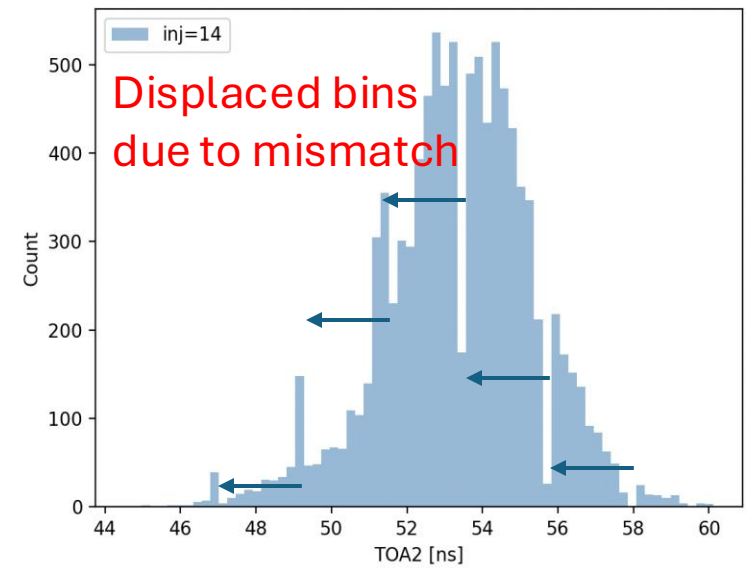
High Power TDC

- The high-power TDC uses a 1 GHz clock that ripples through a coarse counter and delay line in parallel.
- A coarse counter counts the incoming clock rising edges and the delay line propagates the clocks rising edge in 20 ps increments.
- The penetration of the clock rising-edge into the delay line is used for a fine count.

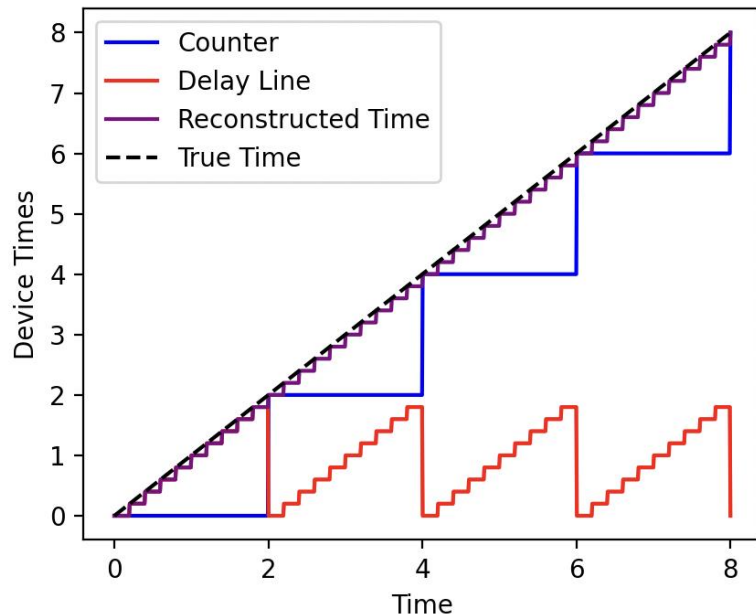


Mismatch in High Power TDC

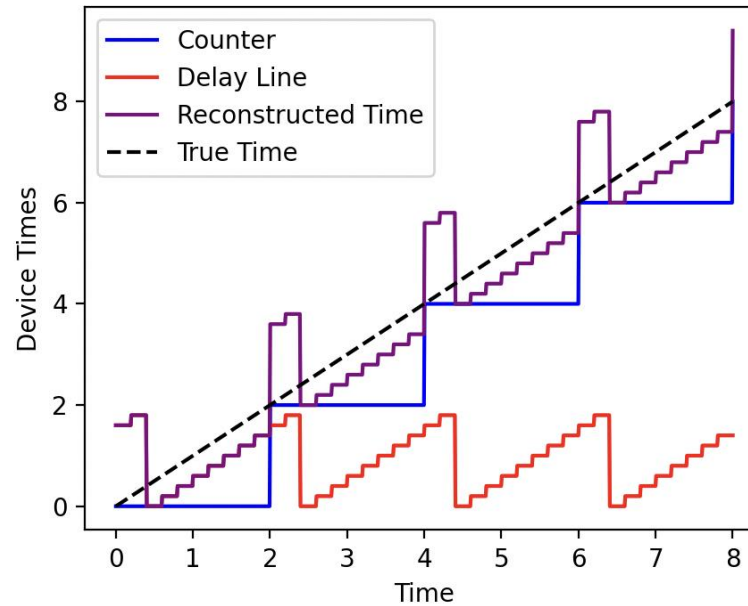
- There is a propagation delay between the clock reaching the coarse counter and the delay line.
- The propagation delay causes discrete jumps in the measured TOA.
- This propagation delay is constant in a single measurement (TPV dependent) and is corrected in each measurement.



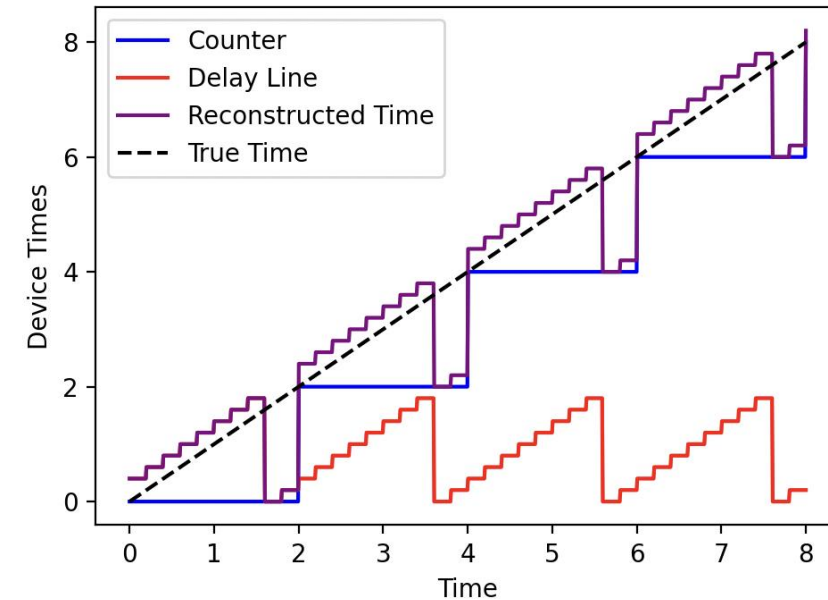
No Propagation Delay



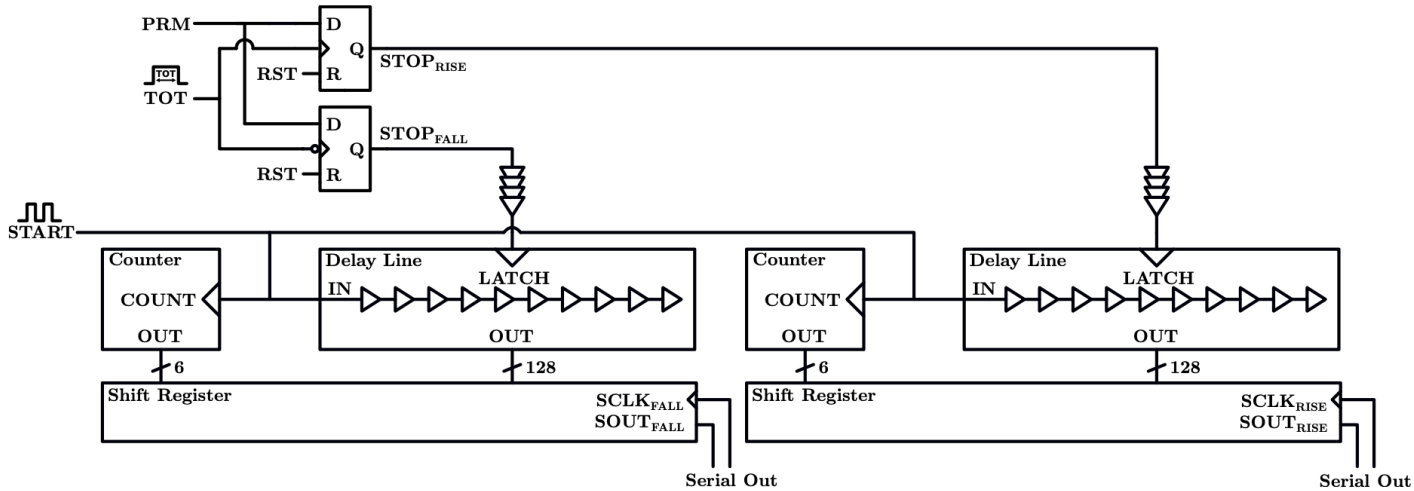
Delay Line Behind



Delay Line Ahead

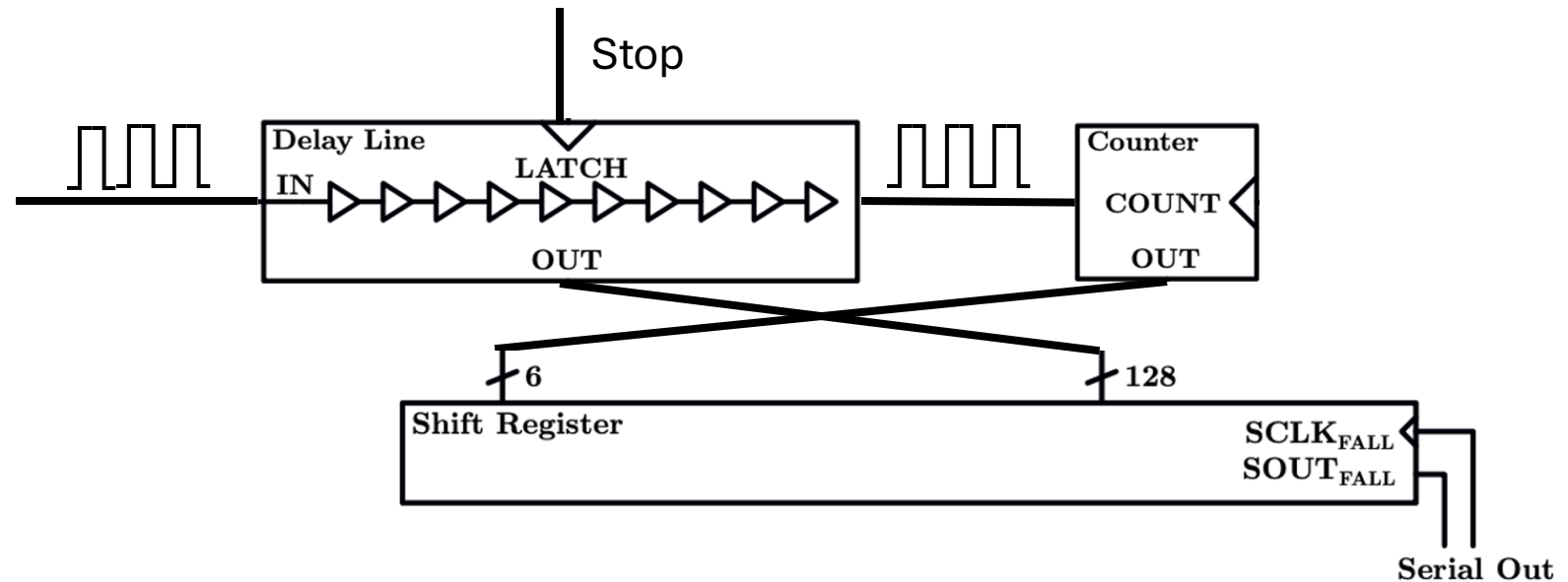


TDC Improvements



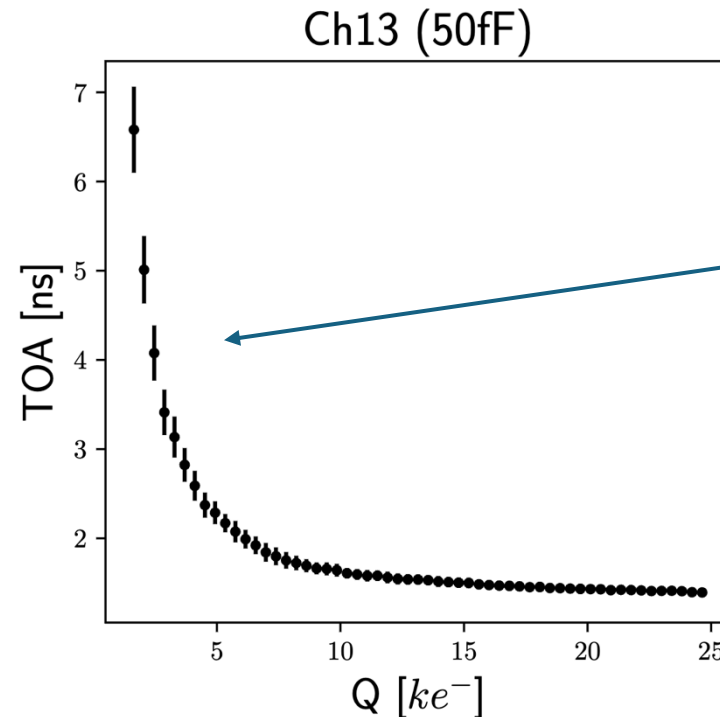
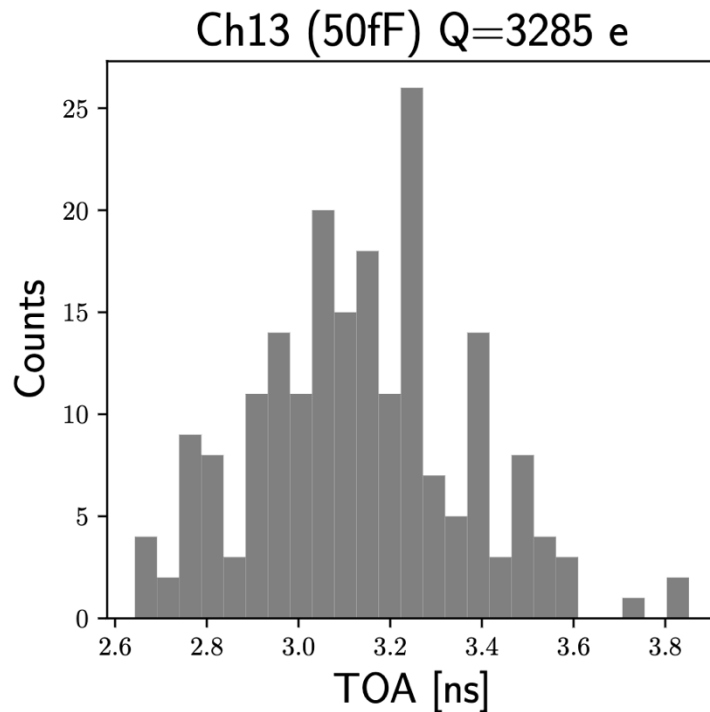
- The mismatch is possible because the counter and delay line are in parallel.

- Putting the delay line and counter in series would resolve this problem.



Preamplifier and Discriminator Performance

- After correcting for the high-power TDC mismatch, the TOA distribution is gaussian.
- The charge injection circuit has a jitter of ~ 2 ps (from simulation), *and we assume negligible jitter from the high-power TDC.**

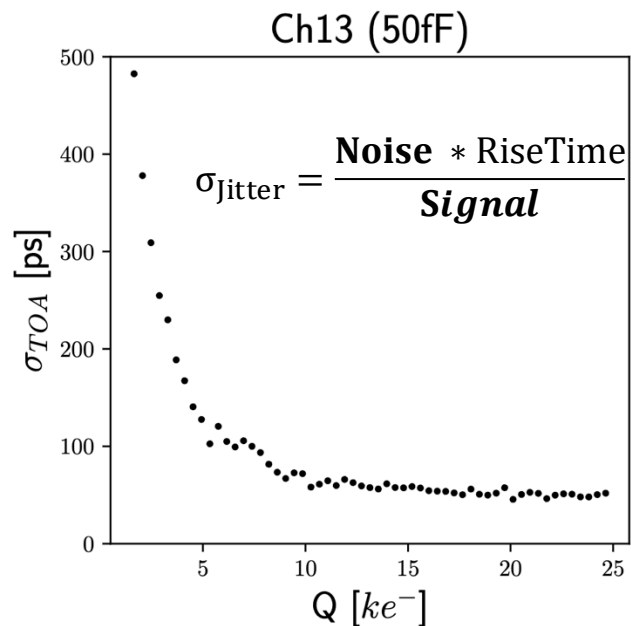


Later TOA from smaller injections because of time-walk

**not verified, testing with an external TDC*

Preamplifier and Discriminator Performance

- The standard deviation of the TOA distribution is plotted below versus charge.
- At low charge injections, the S/N ratio is less, which increases jitter.

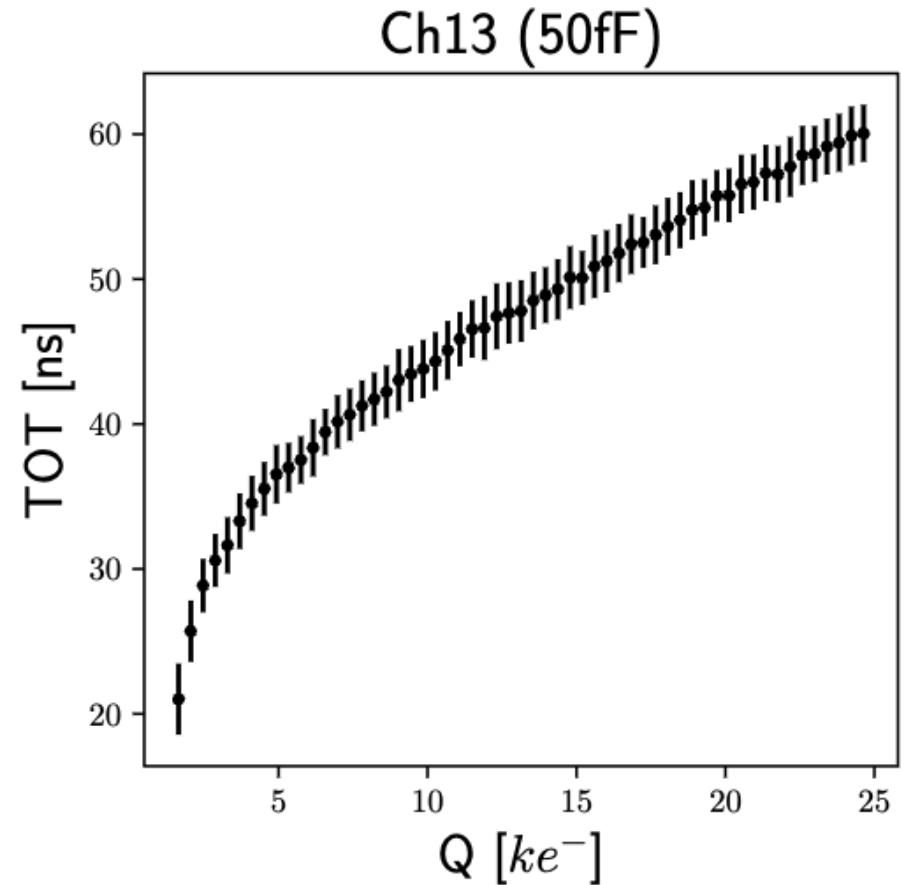
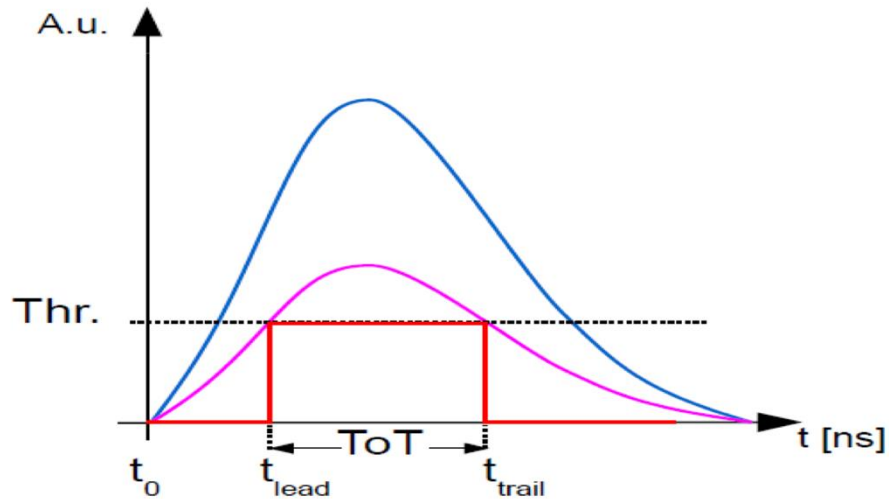


Channel	Capacitance [fF]	$\sigma_{TOA}(3ke^-)$	$\sigma_{TOA}(10ke^-)$
3	0	91	71
4	0	105	74
5	25	105	78
9	25	190	79
10	50	229	71
11	50	218	77
12	50	211	77
13	50	230	58
14	100	471	149

- **Compared to Pebbles, this is not significantly better jitter performance.** We are investigating why.
 - Optimization and validation of the setup?
 - Non-negligible contribution to jitter from the high-power characterization TDC?

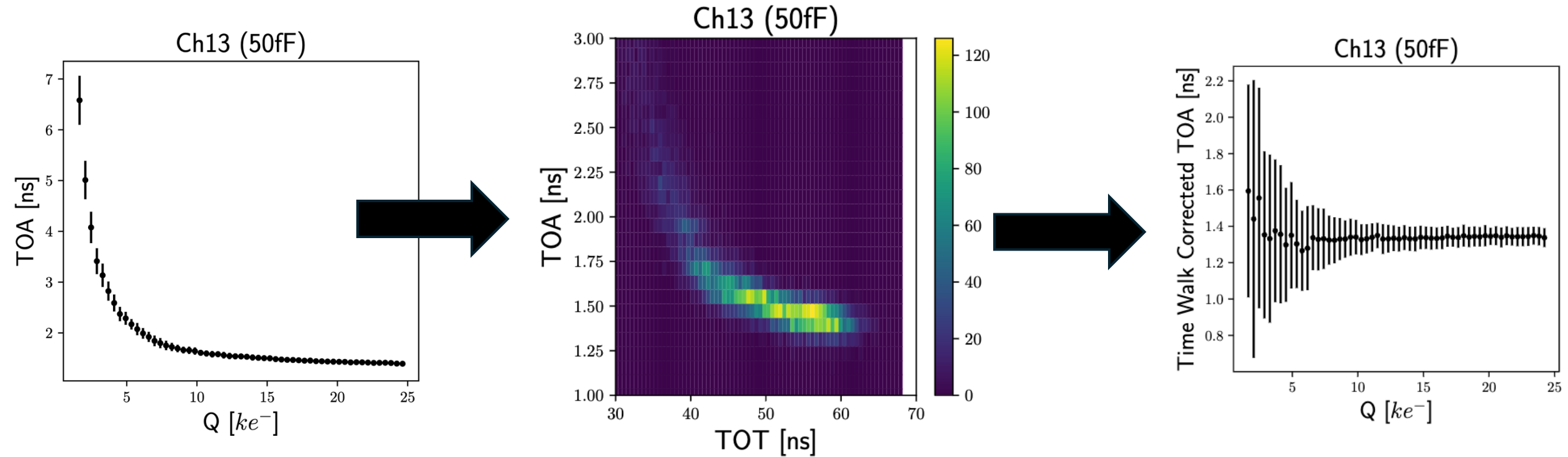
Time Walk Correction

- **Time walk** is an effect on TOA measurements due to smaller amplitude signals reaching threshold later than high amplitude signals.
- The TOT's relationship with the charge injection can be used to correct time walk.
- The TOT is calculated at each step in the charge injection.



Time Walk Correction

- A look up table is made based on the combined TOA and TOT measurement.
- After the time-walk-correction, the TOA measurement is consistent for different charge injection levels. This does not affect the uncertainty in the time resolution caused by the front-end jitter.



- This correction assumed TOT with same resolution as the TOA. Real systems will have coarse TOT measurements, which will effect the time-walk corrections performance.

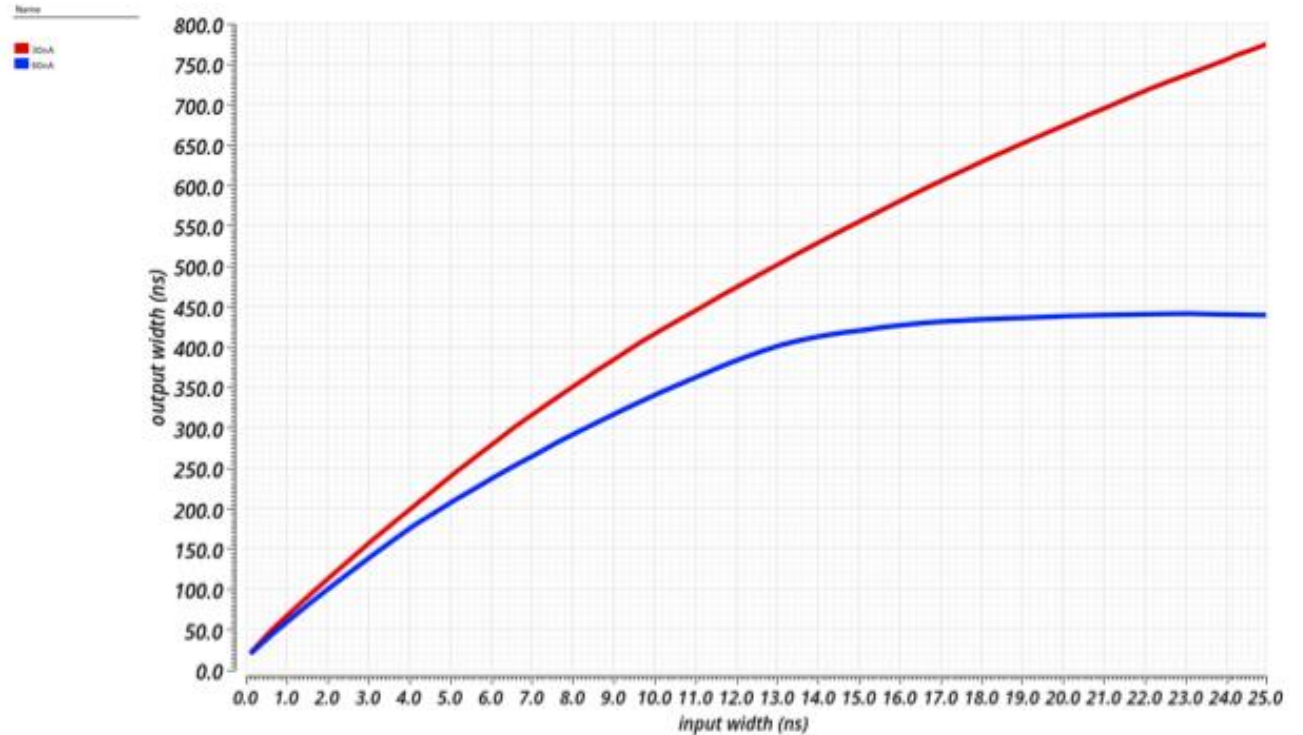
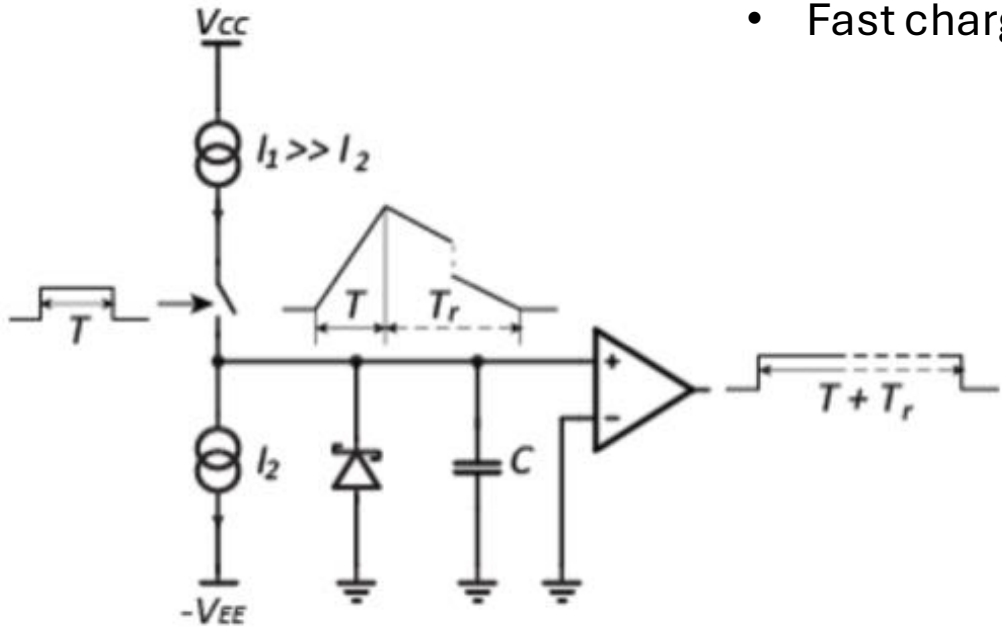
Conclusion

- **MetaRock** is the latest edition of LBNL's prototype front-end fabricated in **the 28 nm CMOS node**.
 - Front end optimized for parasitic capacitance
 - Prototype low-power TDC, which has not been tested
- Measurements of MetaRock's **ENC**, **TOA**, σ_{TOA} and **TOT** have been made. These measurements have been used for a **time walk correction**.
 - Setup validation still required!
- Upcoming measurements include testing the low-power TDC on the FIB altered MetaRock chips and studying the performance of the device under X-ray irradiations.

Backup Slides

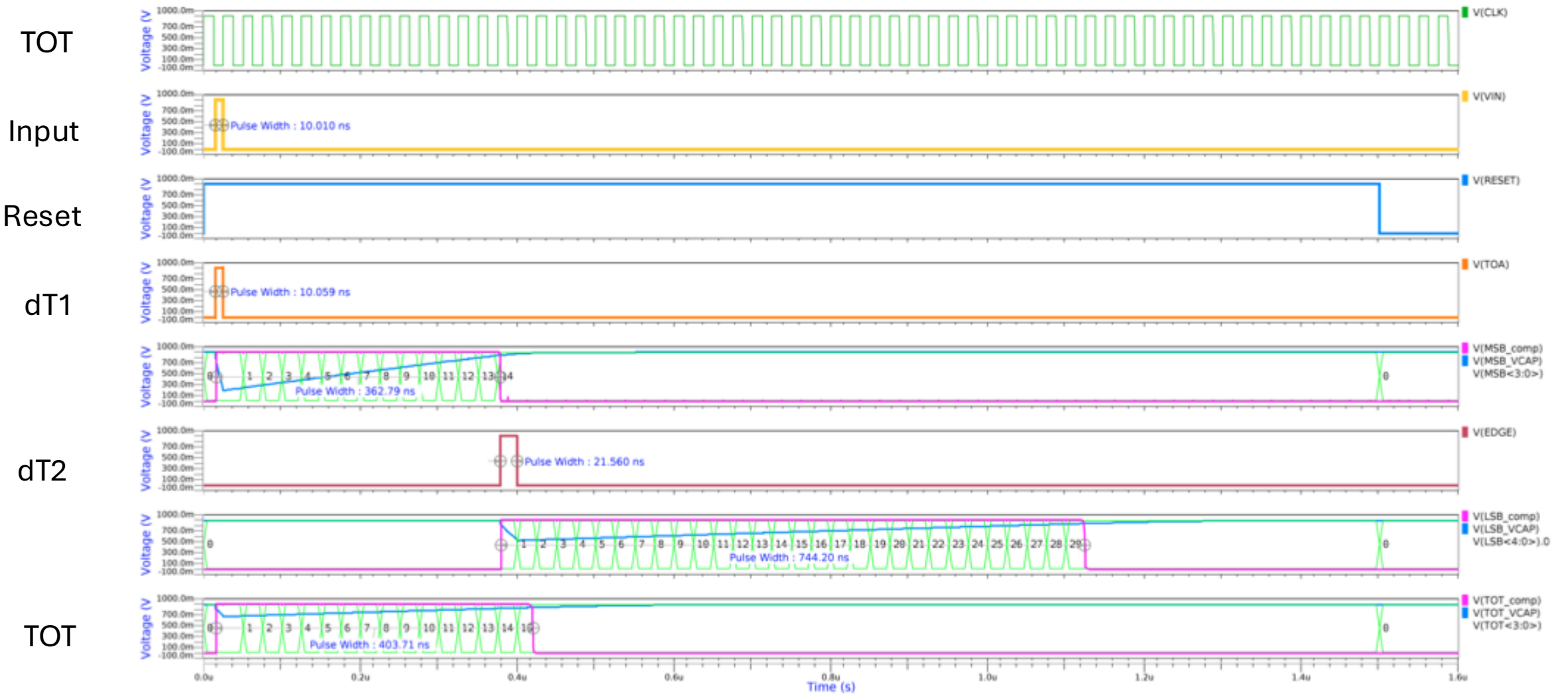
Backup: More on low-power TDC Time Stretching

- Fast charge capacitor, discharge slowly



From Z. Zhang

Backup: More on low-power TDC Time Stretching



From Z. Zhang

Backup: More on the TDC requirements

Variable	Target	Note
Clock Frequency	40 MHz	based on LHC
Dynamic Range	10 ns	must be able to measure nearest clock edge from 10 μ s conversion time with stretching
Hit Rate	100 kHz	

TDC Specs

Variable	requirement	result (simulation)
Time resolution	< 50ps	LSB: \sim 25 ps noise: \sim 30 ps total: \sim 40 ps
Area	< 30 \times 50 μ m	15 \times 13 μ m analog 23 \times 13 μ m digital (counters) 38 \times 13 μ m total
Power	< 10 μ W average	< 5 μ W during conversion
Range	10 ns	13 ns
Hit rate	\sim 100 kHz	max conversion time \sim 2 us (500 kHz)

From Z. Zhang

Backup: More on charge injection circuit

Figure of Merit	Requirement	Simulated Performance
Injection Dynamic Range	100 e ⁻ to 20 ke ⁻	50 e ⁻ to 24.1 ke ⁻
Injection Precision	$\ll 100 e^-$ RMS	12 e ⁻ RMS
Injection Rise Time	≈ 100 ps	40 ps
Injection Fall Time	≈ 100 ps	100 ps
Injection Jitter	< 2 ps RMS	0.69 ps RMS
Supply Voltage	0.9 V	0.9 V
Tolerable Supply Noise	1 mV RMS	1 mV RMS
Radiation Hardness	1000 Mrad	1000 Mrad
Operating Temperature	-10 °C to 50 °C	-10 °C to 50 °C
Silicon Area	$< 60 \mu\text{m} \times 60 \mu\text{m}$	$50 \mu\text{m} \times 30 \mu\text{m}$
Power Consumption	No Limit	6.5 mA peak

Table 3.2: Expected performance of charge injection circuit vs design specifications.

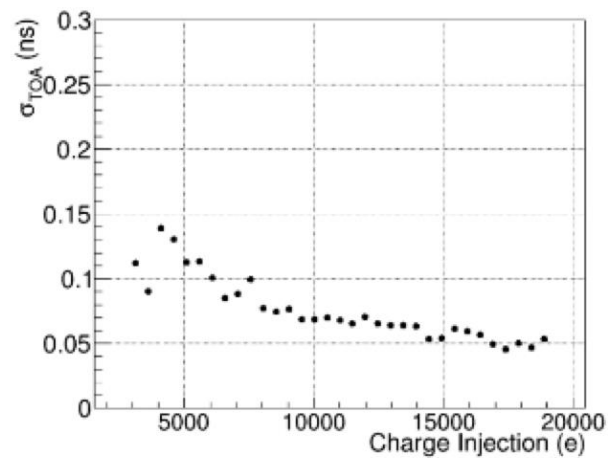
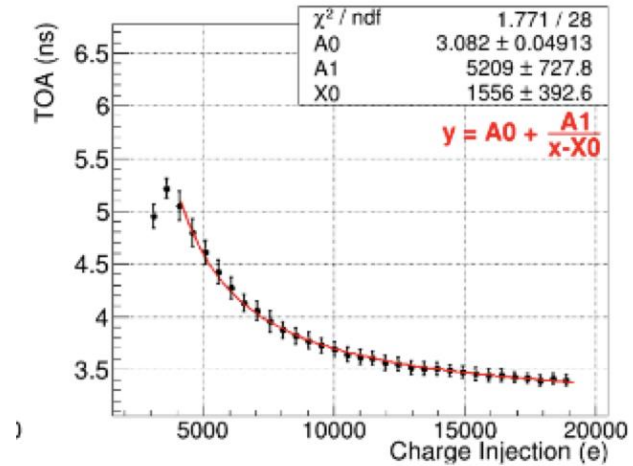
From K. Caisley

Backup: More on Timing Resolution

$$\sigma_{\text{Track}} = \frac{\sigma_{\text{sensor}}}{\sqrt{N}}$$

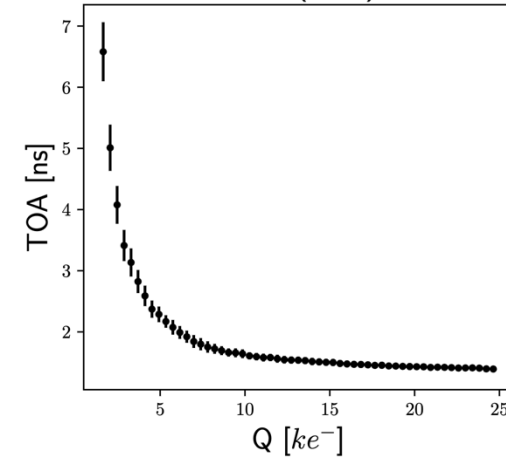
Backup: Effect of the Mismatch Correction

Mismatch Not Fixed

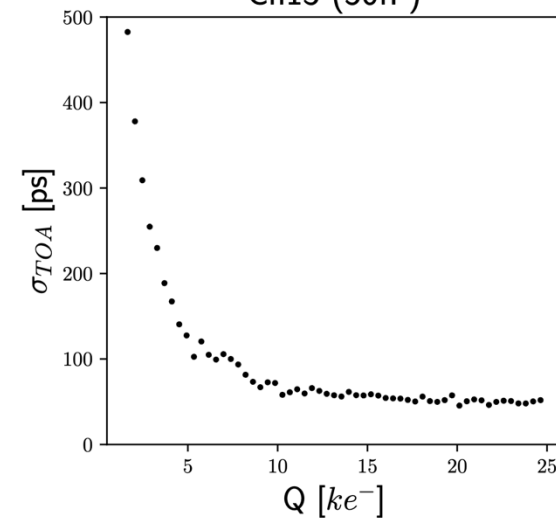


Mismatch Fixed

Ch13 (50fF)



Ch13 (50fF)



Comments from Timon on the hit rate

50 μm x 50 μm (half analog half digital)

Analog – FE, TDC, trimDAQs

- 35 x 35 (FE + TimeStretcher)
- Counters go into digital

Same power density as current detector (10 μW for analog and digital), 5 μW for just analog.

Chose 12.5 ns –

AFE target

- 35x35 μm^2 minus TDC area (they share)
- AFE 50 ps at 3 ke
- 1000e threshold (with 100 ENC at 50 fF)
- 5 μW power (6 μA at .9V) - minus analog TDC

TDC Target Table

- Choose deadtime and dynamic range
- 40 MHz clock in LHC – recycled parameter
 - Time stretching by a factor of 500

Double edge counting doubles clock frequency for counting

Variable	requirement
Time resolution	< 50ps
Area	< 30 × 50 μm
Power	< 10 μW average
Range	10 ns
Hit rate	~100 kHz

Variable	Target	Note
Time Resolution	< 50 ps	at 3 ke ⁻
Analog Area	35 μm × 35 μm	Split with TDC analog component
Analog Power	5 μW	Split with TDC analog component
Threshold	1000 e ⁻	100 e ⁻ ENC

4mW per channel
(HGTD)
1 mm², higher capacitance

Meeting Context

- I am presenting on Wednesday 11/20, 2:45 pm in the **RDC 04 Parallel Session**.
- The talk is 15 minutes (~13+~2).
- In person.
- Before I present there is at least one 4D tracking talk and at least 2 LHC Calorimeter electronics talks.
 - I am going to email Bojan so we don't repeat too many of the same introductory slides.
 - I might add a "optional" collider experiment slide to give context, but I assume it will be mentioned by the other students.
- A lot of the data analysis is incomplete, plots that will be redone are marked with **red star**

Time	Topic	Speaker
13:30 - 13:45	28nm sub-10ps TDC ASIC for 4D tracking - design and characterization	Bojan Markovic
13:45 - 14:00	Embedded FPGA Developments for Machine Learning in Particle Detector Readout	Larry Ruckman
14:00 - 14:15	Front-end electronics of the High Granularity Electromagnetic Forward Calorimeter (FoCal-E) at ALICE	Nicola Minafra
14:15 - 14:30	Design, Testing, and Results of the Multi-channel Fermilab CFD Readout ASIC	Si Xie
14:30 - 14:45	LArPix Pixelated Charge Readout System	Brooke Russell
14:45 - 15:00	Characterization of the MetaRock fast timing analog front end for future HEP experiments	Josef Sorenson
15:00 - 15:15	GammaTPC: A Next-Generation MeV Gamma-Ray Instrument	Bahrudin Trbalic