Analog Photon Processor aka… APP

Mitch Newcomer
for the
Penn Instrumentation group

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The APP photon counting Concept .

Modern PMT’s have excellent <u>Single Photo Electron</u> (SPE) characteristics:

Gain of 10^7 to 10^8 uniform to +/-15%

Transit Time Spread of ~0.7ns

Efficiency > 20%

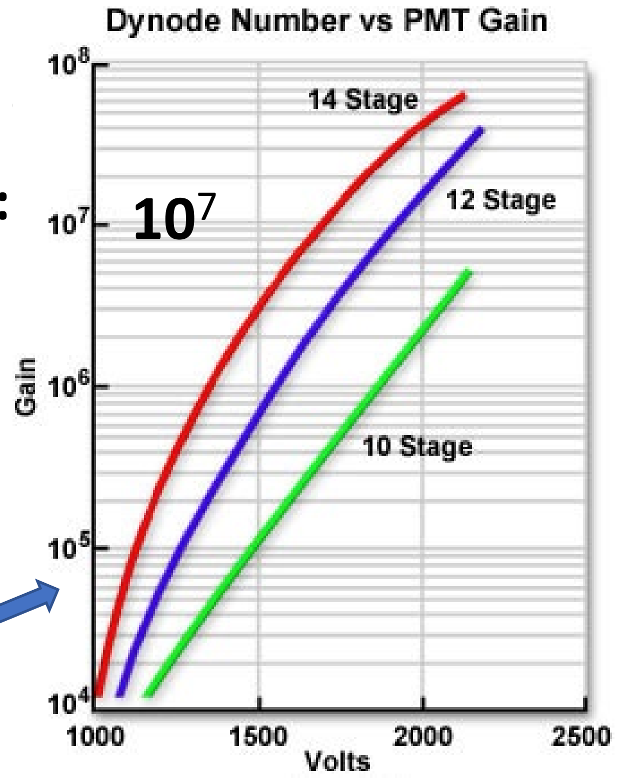
The shape of the output signal is determined by the dynode amplifying chain.

Important features for Photon Counting like:

Time Over Threshold (leading & trailing edge time)

Integral Charge

Time, Amplitude of peak(s)



Can be extracted from analog signal processing to count the number of detected PE especially for low rate underground neutrino experiments where the number of PE / PMT is small.

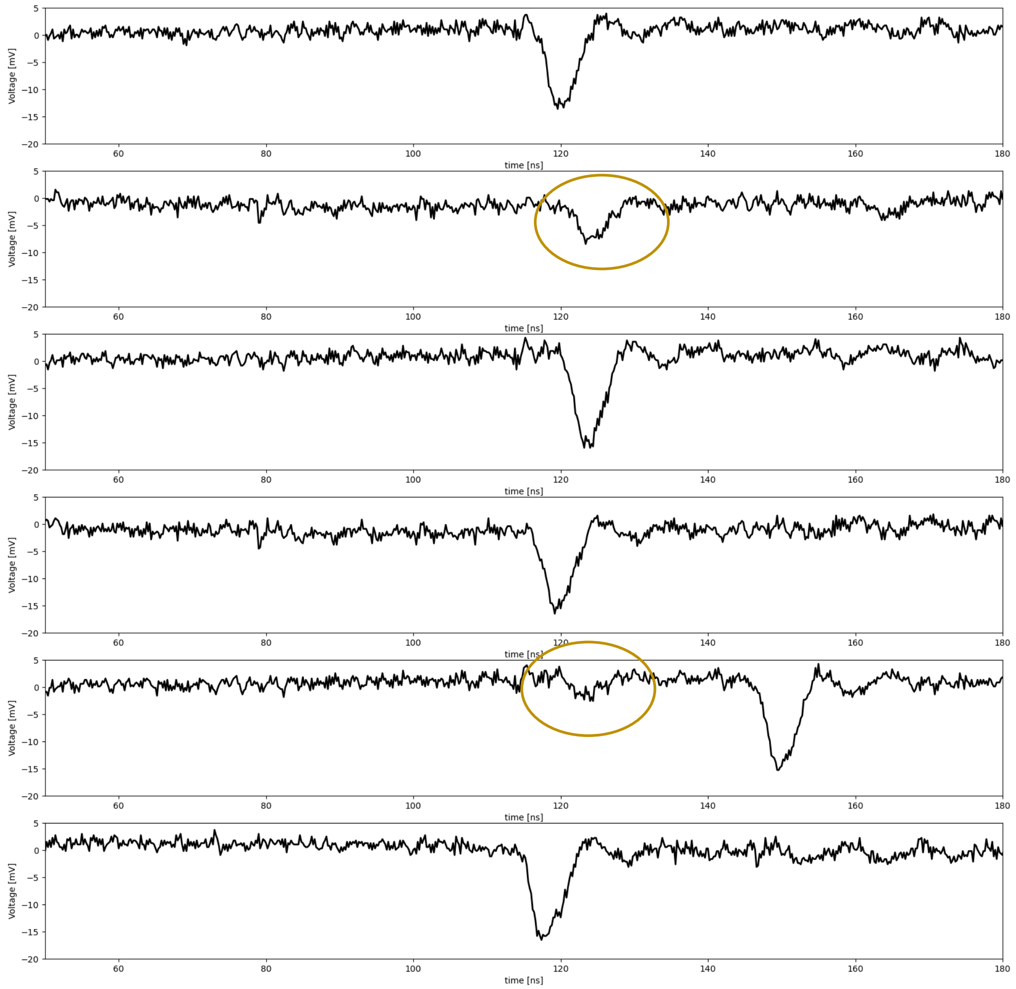
These analog extracted features can be adequately serviced by inexpensive commercial low rate ADC’s perhaps using one ADC per extracted feature.

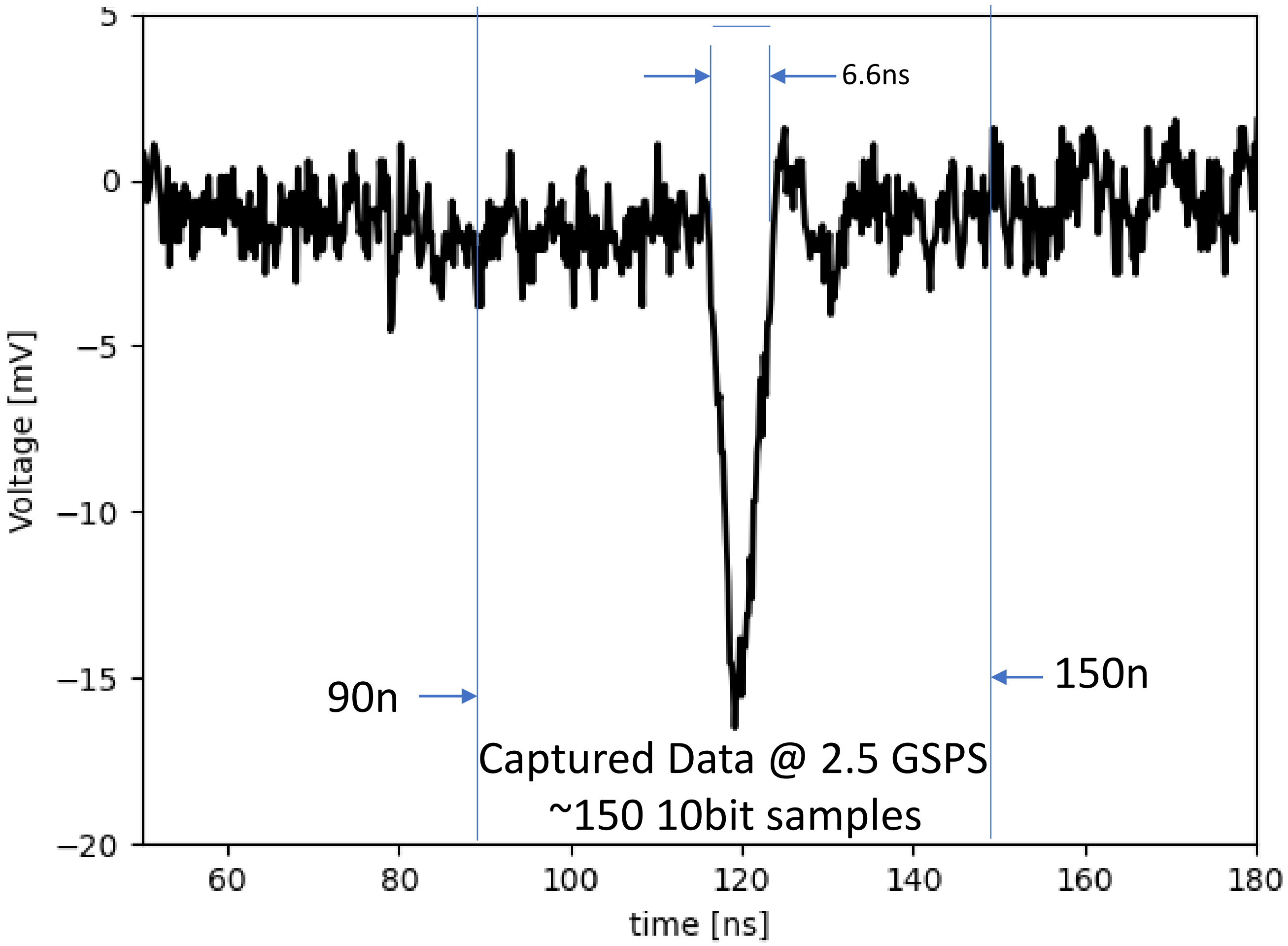
TI ADS794 SAR ADC 12b 2MSPS -- $5 Quantity(100)

***Due to the size of the PMT collection area (square inches) there is no need for high density channel packing. An analog readout ASIC might be best bounded as 1- 4 channels.**

Combined and Individual SPE PMT signals

Hamamatsu 8-inch R14688-100  digitized by CAEN V1742s at 5Ghz





*note Low Threshold trigger is not biased against smaller SPE like signals Most are similar at > 15mV into 50Ω

These PMTs are characterized and described in the following publications

- **Characterization of the Hamamatsu 8” R5912-MOD Photomultiplier tube,** Tanner Kaptanoglu, **Nuclear Instruments and Methods in Physics Research Section A:** Volume 889, 1 May 2018, Pages 69-77, https://doi.org/10.1016/j.nima.2018.01.086
- **Characterization of the Hamamatsu 8-inch R14688-100PMT** https://arxiv.org/pdf/2311.05080

prepared for publication in Jinst by

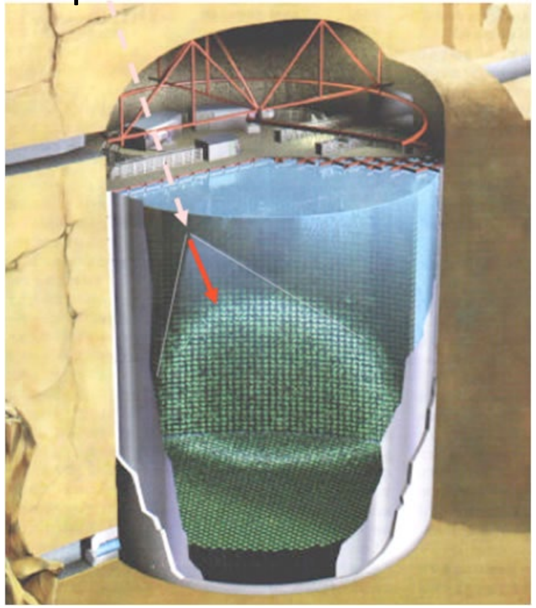
Tanner Kaptanoglu1,2 Ashley Rincon1 Mackenzie Duce4 Sawyer Kaplan1 Joseph Koplowitz1 Skipper Lynch3 Hong Joo Ryoo1 Gabriel Orebi Gann1,2

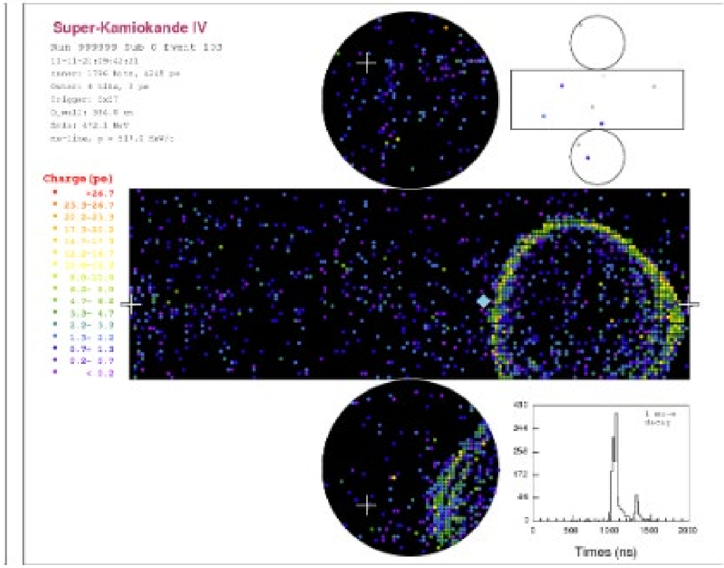
1University of California, Berkeley, 366 Physics North, Berkeley, CA 94720-7300
2Lawrence Berkeley National Laboratory, 1 Cyclotron Rd, Berkeley CA 94720-8153
3Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA 02139-4307
4Georgia Institute of Technology, 801 Ferst Drive, Atlanta, GA 30332-0315

The Read Out Electronics Use Case

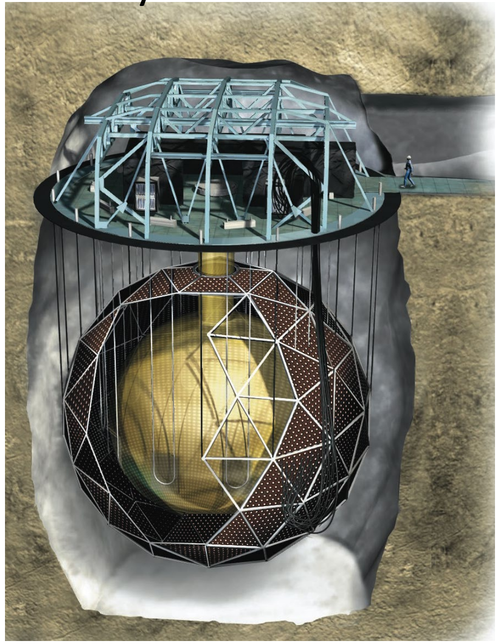
Water Cherenkov neutrino detectors have signals that are primarily single pe with up to 10-20 pe/channel

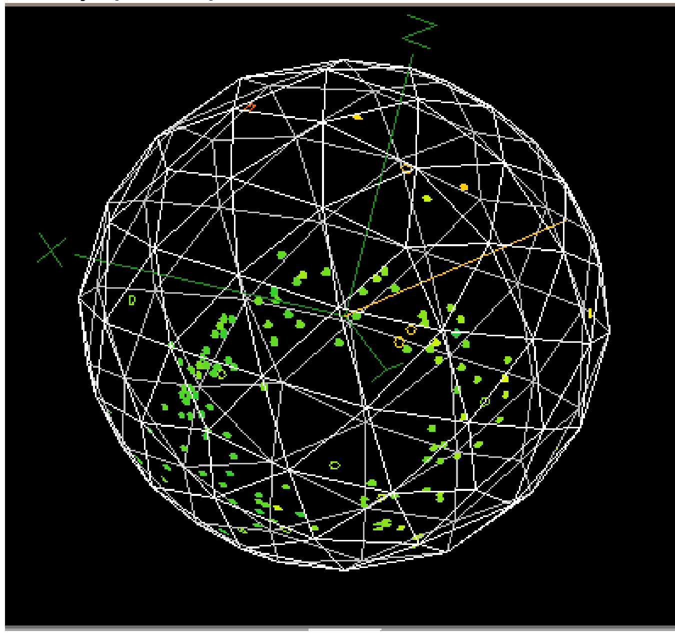
Super-Kamiokande





Sudbury Neutrino Observatory (SNO)



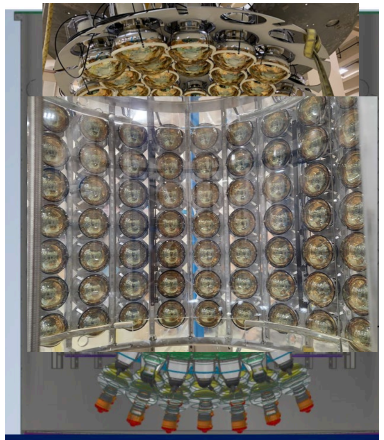


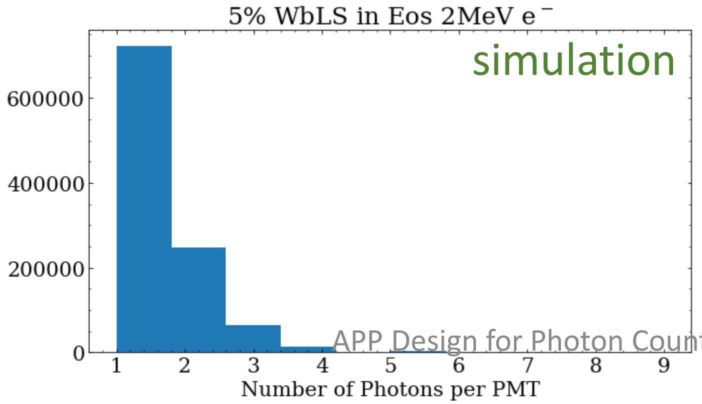
Scintillation or Water-based scintillation have higher occupancies, depending on energy and position

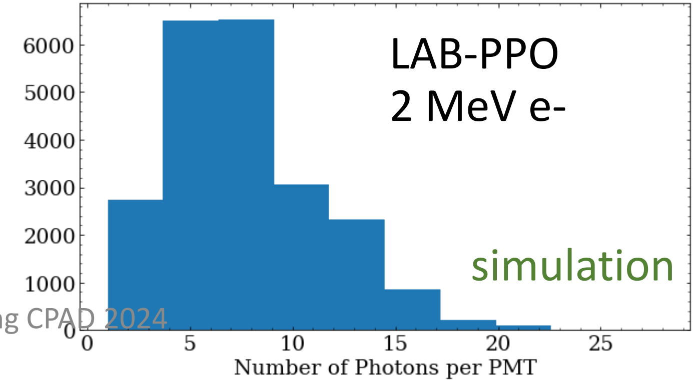
Precision timing on early SPE's can be used to help separate Cherenkov from Scintillator Photons

Eos

(240 PMTs)







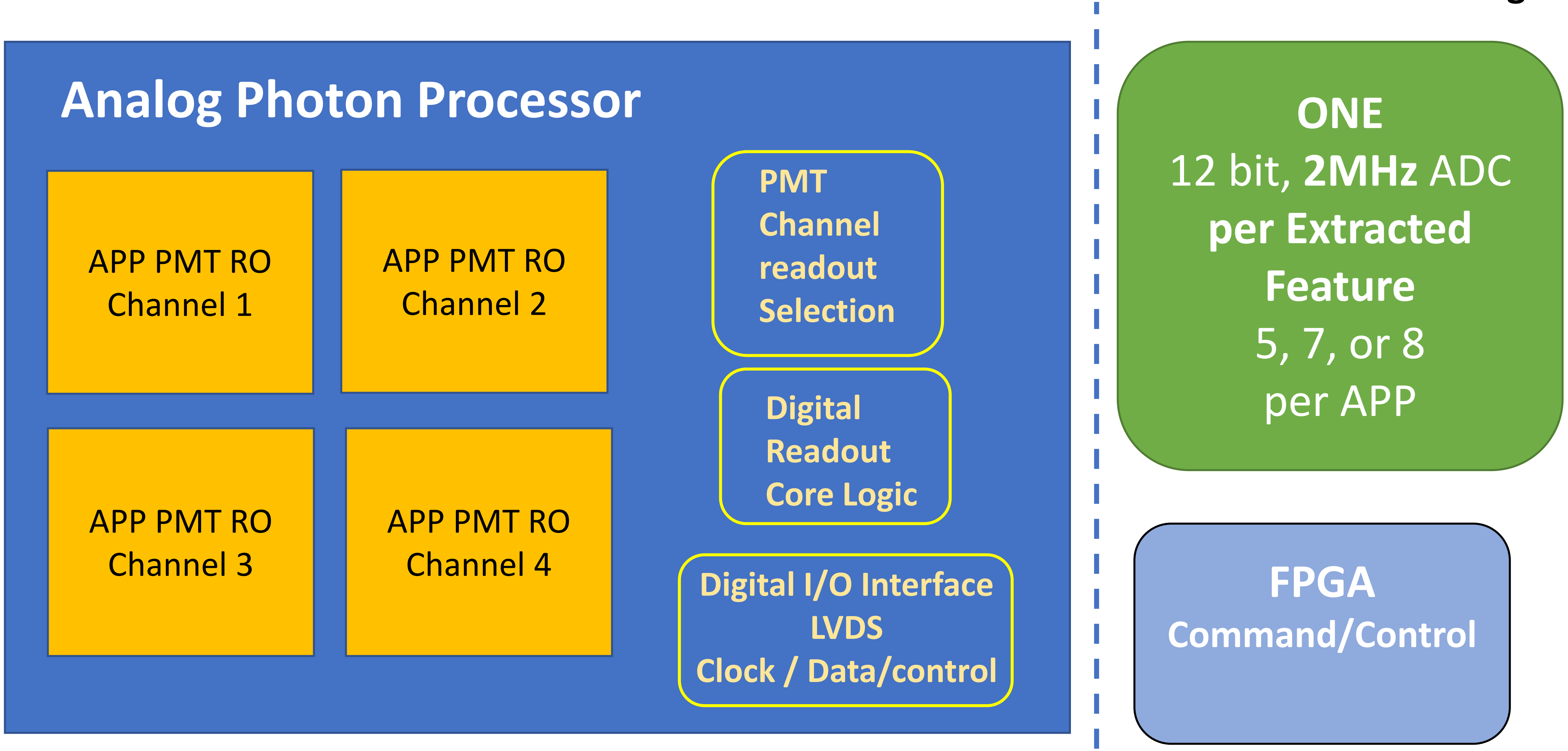
APP ASIC Top Level BLOCK Concept

Custom *Analog Design* *tailored to Unique Analog SPE Signature*

Utilize FPGA's and IP from others or COTs where Possible

Captured Data 8 -12 bit words per self triggered PMT SPE detection

External to APP Analog ASIC



APP analog Block Specification Goals for PMT readout

Technology Node 65nm justified by Minimum Signal size & PMT pulse shape

- Peak detector: Capture 5ns PMT pulse. Amplitude: 5–400 mV ~+/-1 mV; time ~+/- 100ps
- Comparator: ~ 1ns walk @10mV – 600mV with 5mV threshold
- Integrator Range : up to ~200PE → **TBD** (PMT impulse Amplitude limited)
- Analog Delay: 2 – 5 ns; +/- 100ps to minimize effects of discriminator walk.
- TAC: 0 – 25ns; +/- 20ps
- Analog Track and Hold : 0 – 600mV ** +/- 1mv (TBD)
- Analog Memory: planning for 1 ADC/extracted feature with 8 deep analog memory
- Fully Differential Opamp: Each output +/-550mV →Output difference voltage +/- 1.1V
- SE internal to LVDS Driver: prog. 1 – 6mA @ 600mV common mode ~50- 250Mbps.
- LVDS Receiver to SE internal RCVR MAX rate ~50 - 250 Mbps No need for greater Speed
- DAC: 8bit.. Done
- Compiled Logic; TBD

*** consistent with SE opamp measurements but can be increased*

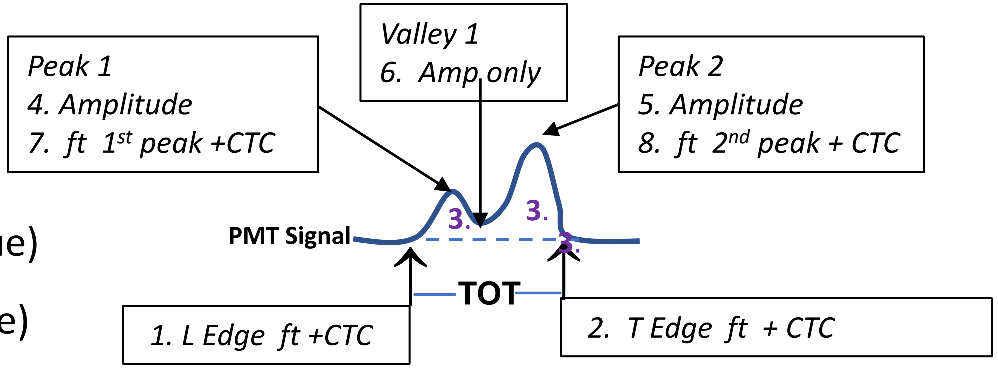
Analog Extracted Features

1. **Leading Edge** Comparator fine time to rising Clock edge (Linked to CTC value)
2. **Trailing Edge** Comparator fine time to rising Clock edge (Linked to CTC value)

TOT when combined wit CTC values

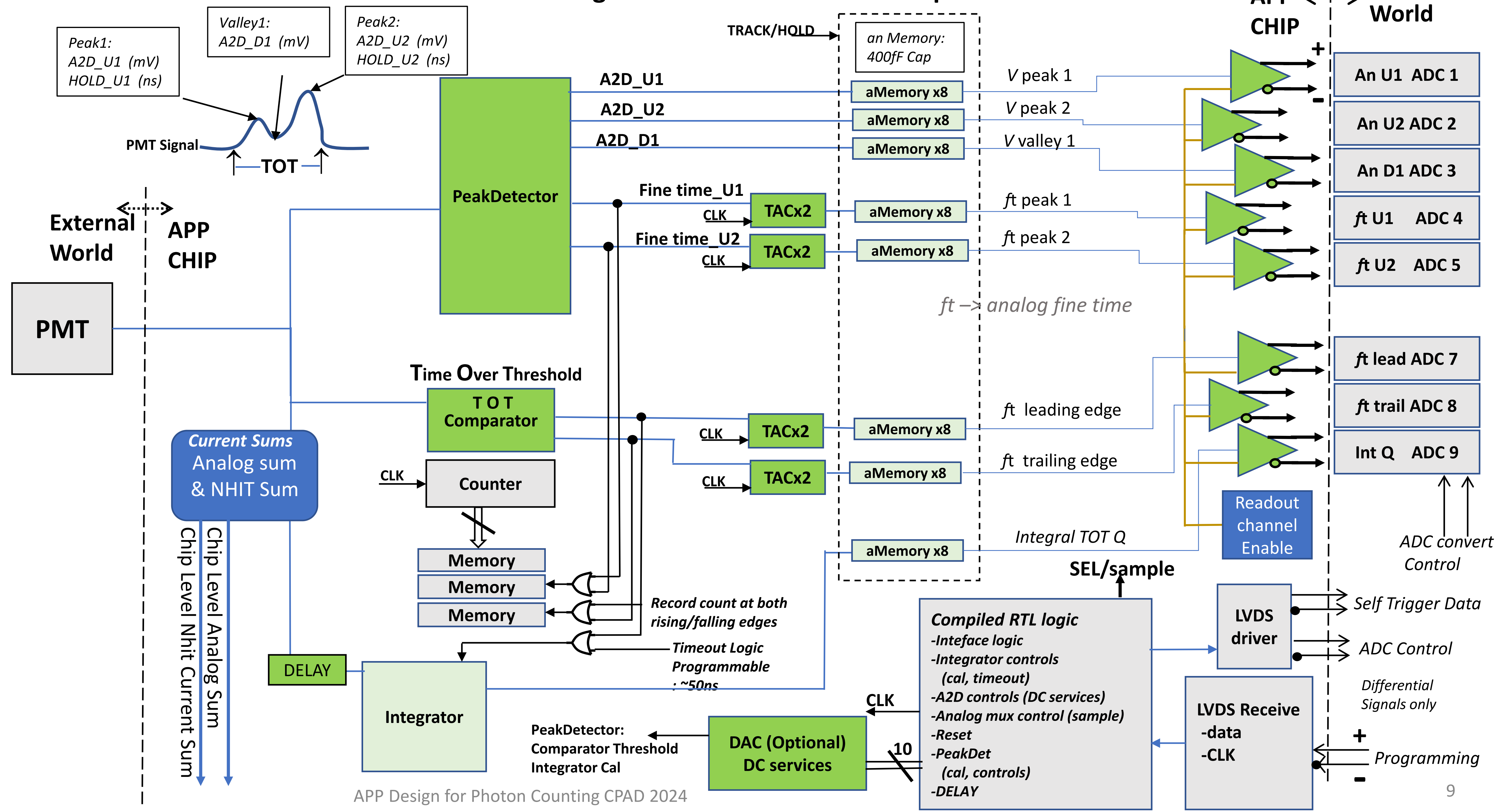
3. **Integral Q** during Time Over Threshold

4. **1st Peak** Amplitude Value
5. **2nd Peak** Amplitude Value
6. **Amplitude of Valley** before 2nd Peak. (optional)
7. **1st fine time** to Rising Clock Edge (Linked to Clock based counter value)
8. **2nd fine time** to rising Clock Edge (Linked to Clock based counter value)



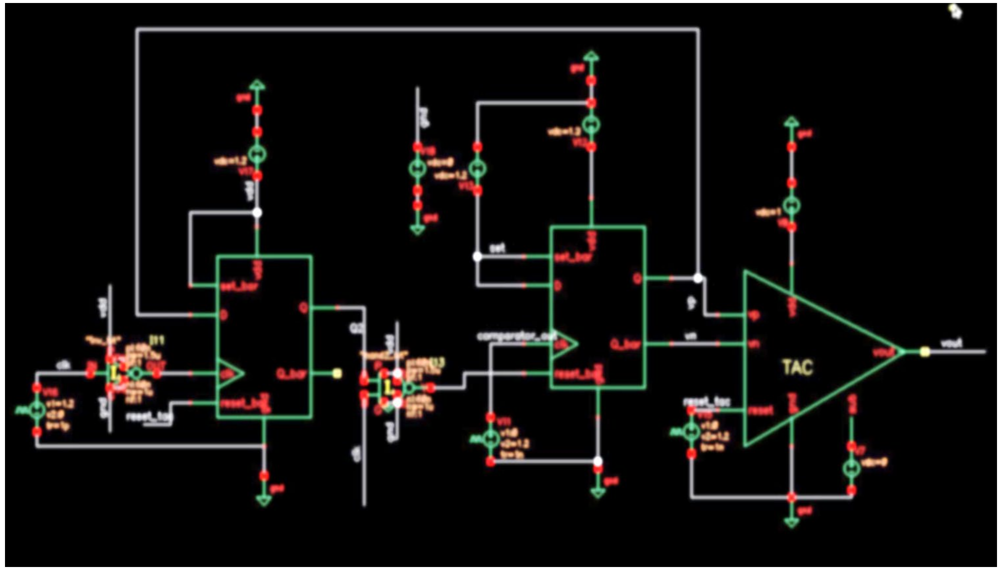
CTC = Coarse Time Clock Counter Value

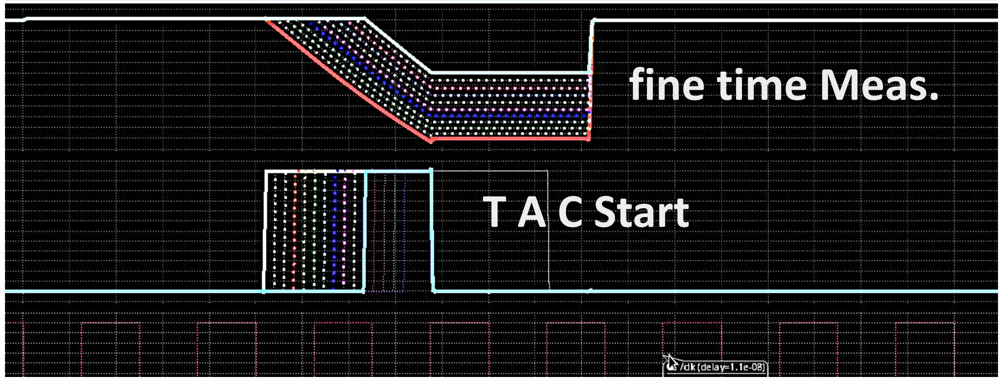
Analog Photon Processor ONE Chip Channel



T A C -- Time to Analog Converter

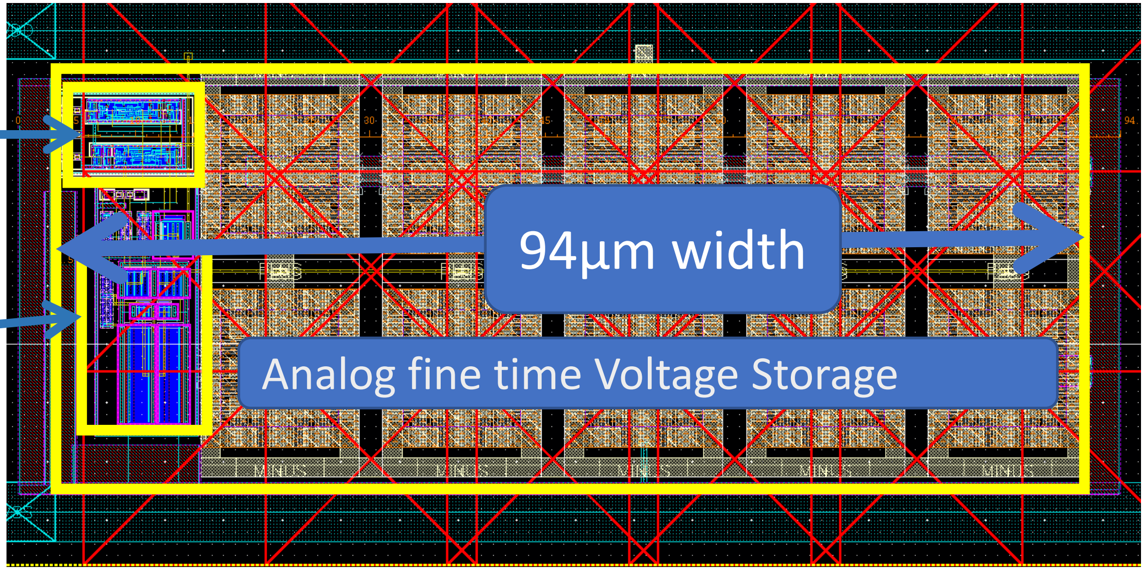
Constant Current Capacitor Discharge (½-1½ Clock pulses)



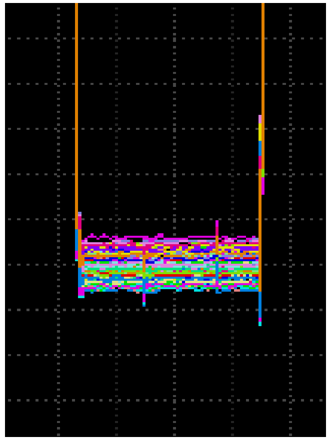


Digital Latch & Clocking Circuit

Analog Circuit Switches current source



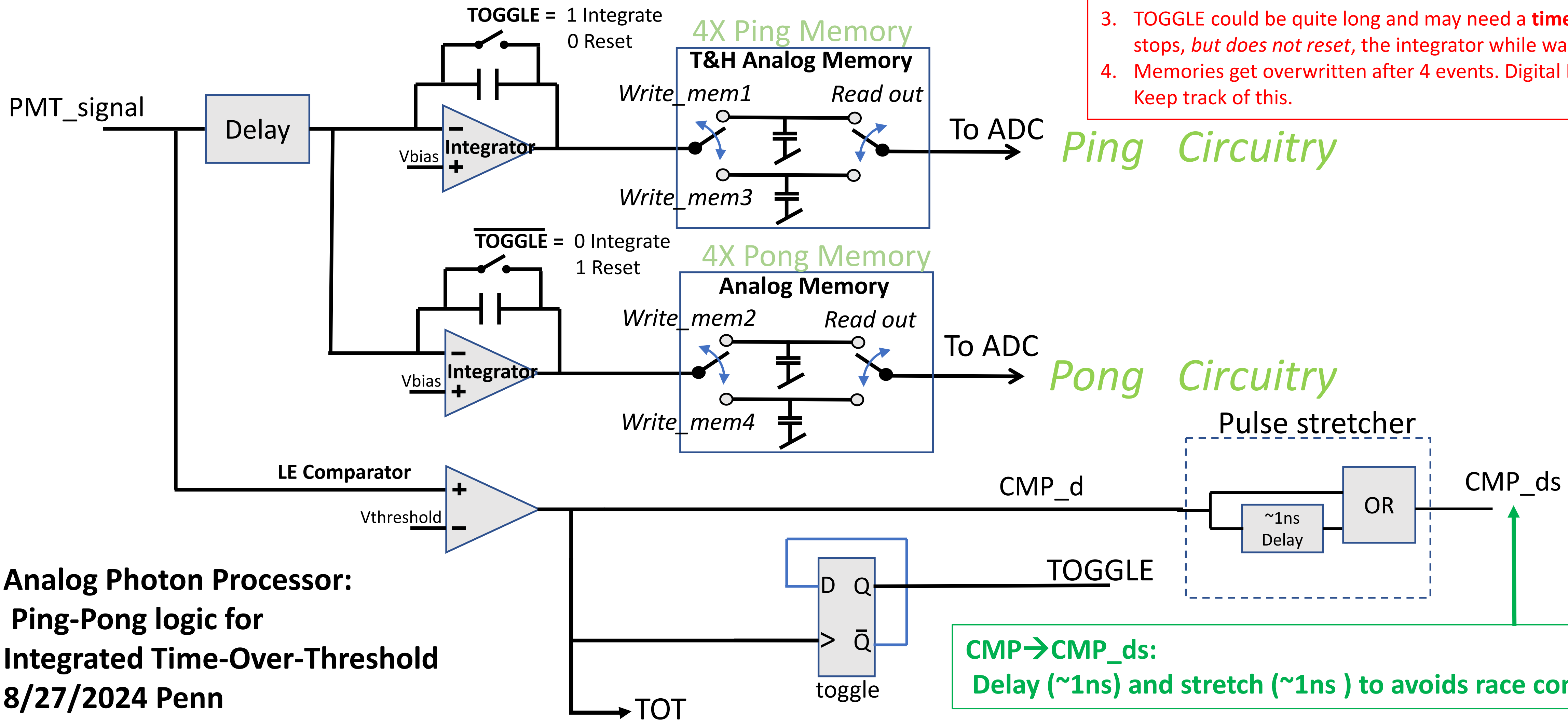
Transient Noise for max *ft*(1.5CLK)
σ=158.17uV @ 13mV/ns ~ σ(t) 12ps



Integrate Q over TOT adding dead timeless Ping Pong Mechanism

Writing Track&Hold Analog memory:
Write switch flips on falling edge of '***CMPstretch & TOGGLE***'

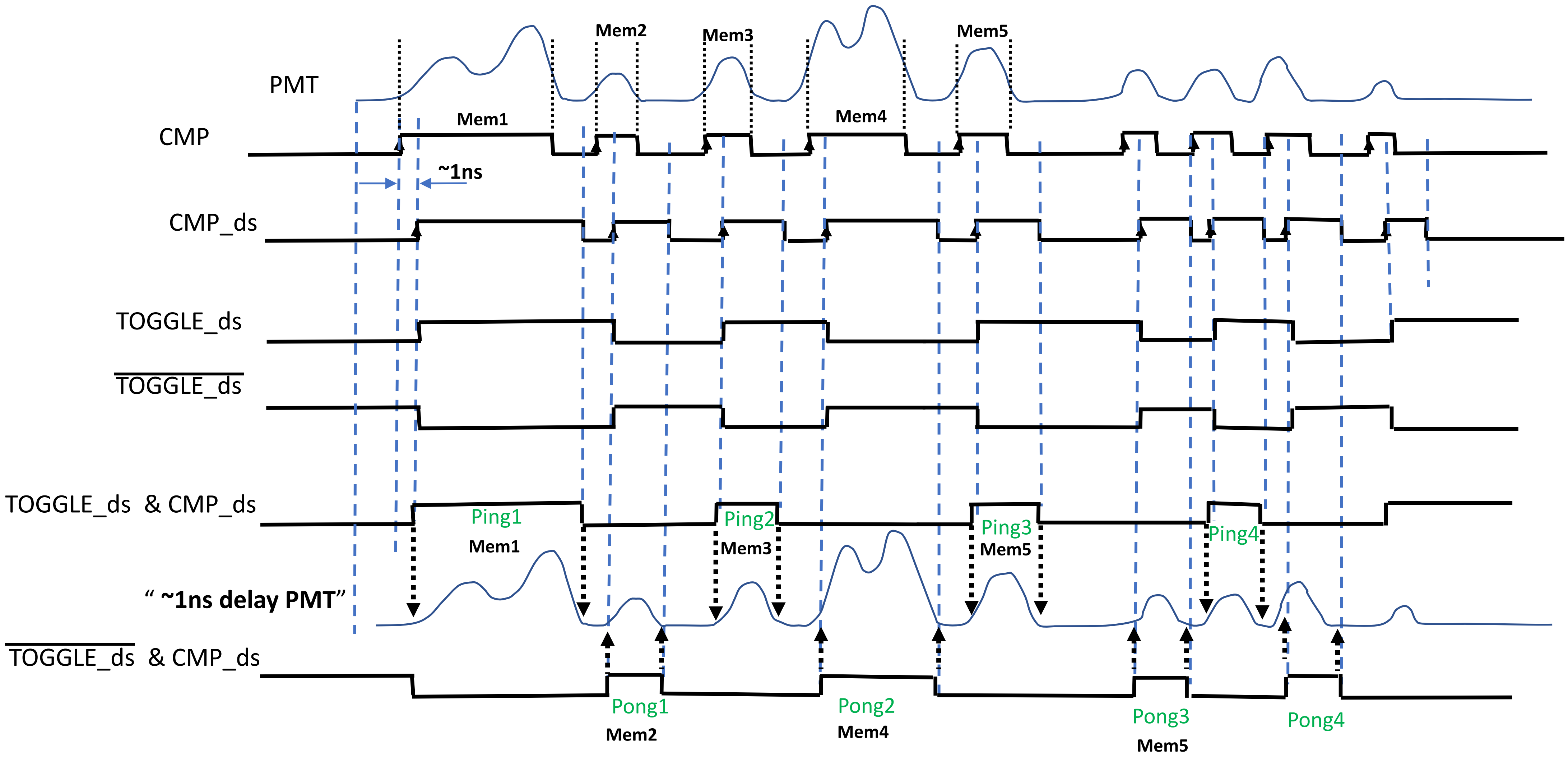
1. State of '**CMPstretch&TOGGLE**' marks time to grab all *other* data: peak Ampl/Times, TACs, event counter, etc.
2. Record state of switches. Mem1-4:
3. TOGGLE could be quite long and may need a **time-out** that stops, *but does not reset*, the integrator while waiting.
4. Memories get overwritten after 4 events. Digital Logic must Keep track of this.



CMP→CMP_ds:
Delay (~1ns) and stretch (~1ns) to avoids race condition

Analog Photon Processor:
Ping-Pong logic for
Integrated Time-Over-Threshold
8/27/2024 Penn

Timing Diagram for the Dead timeless Ping Pong Integrate & Hold



Analog Photon Processor:
ping-pong logic for
Integrated Time-Over-Threshold
8/27/2024 Penn

CMP_ds = Delayed and stretched w.r.t CMP

TOGGLE_ds = Delayed and stretched w.r.t CMP

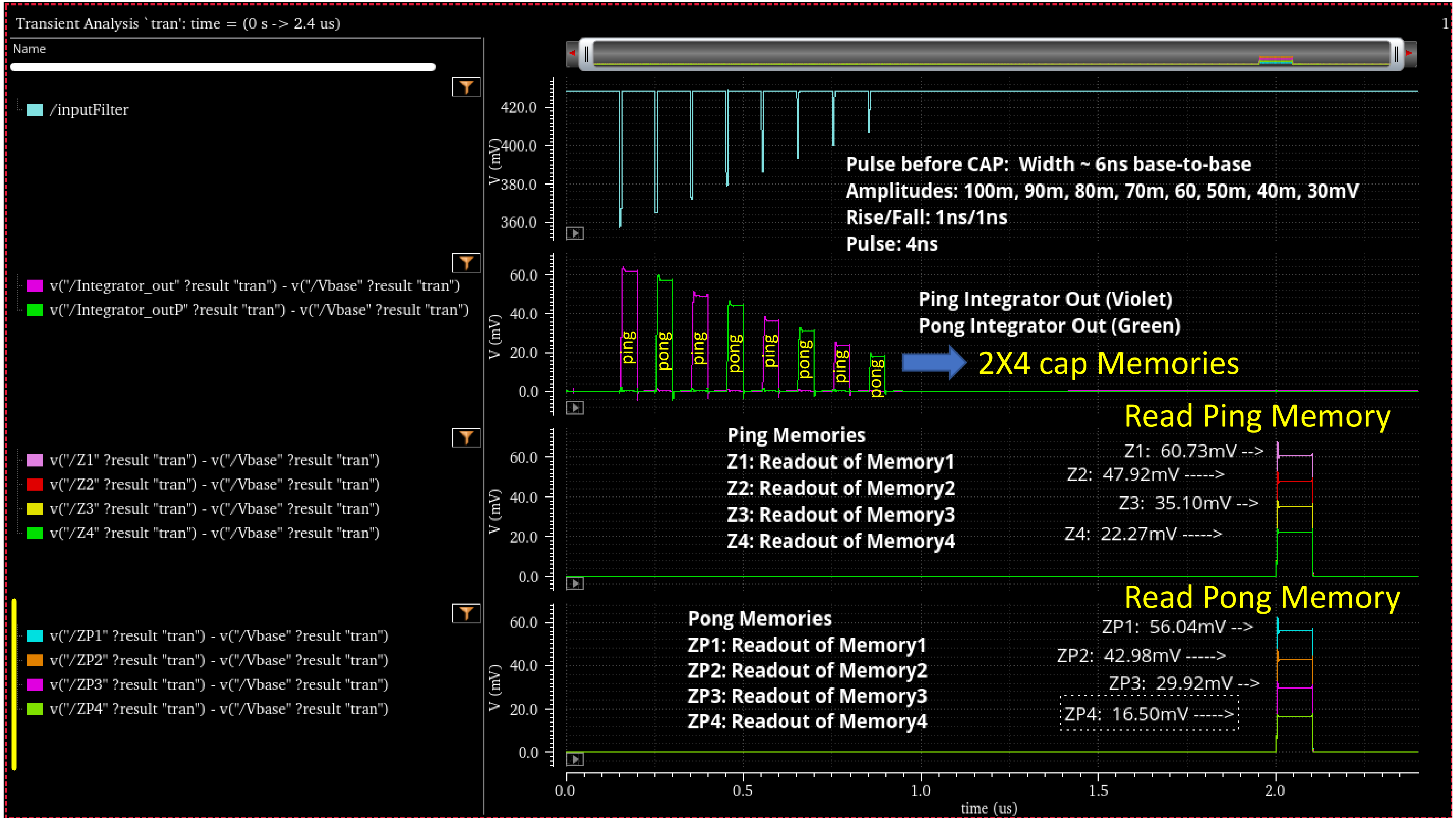
TOGGLE_ds & CMP_ds = 'Ping' Write

$\overline{\text{TOGGLE\_ds}}$ & CMP_ds = 'Pong' Write

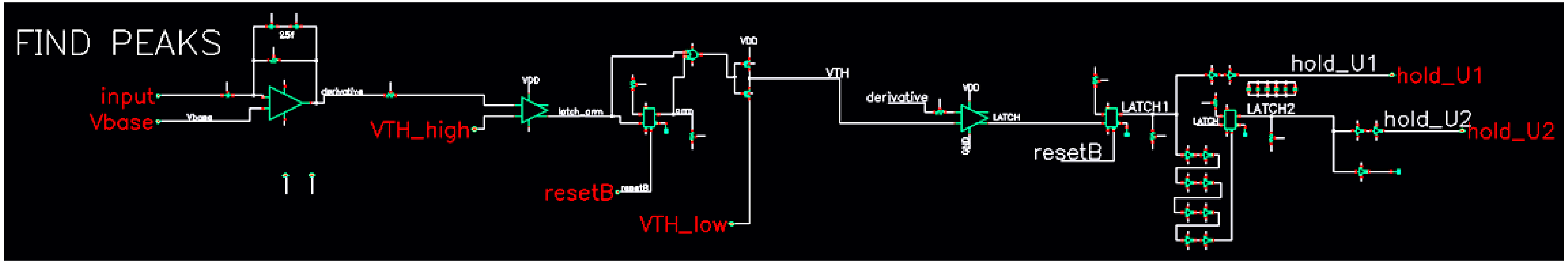
Analog **Input**, Ping – Pong Integrate **&**Memory **Read**

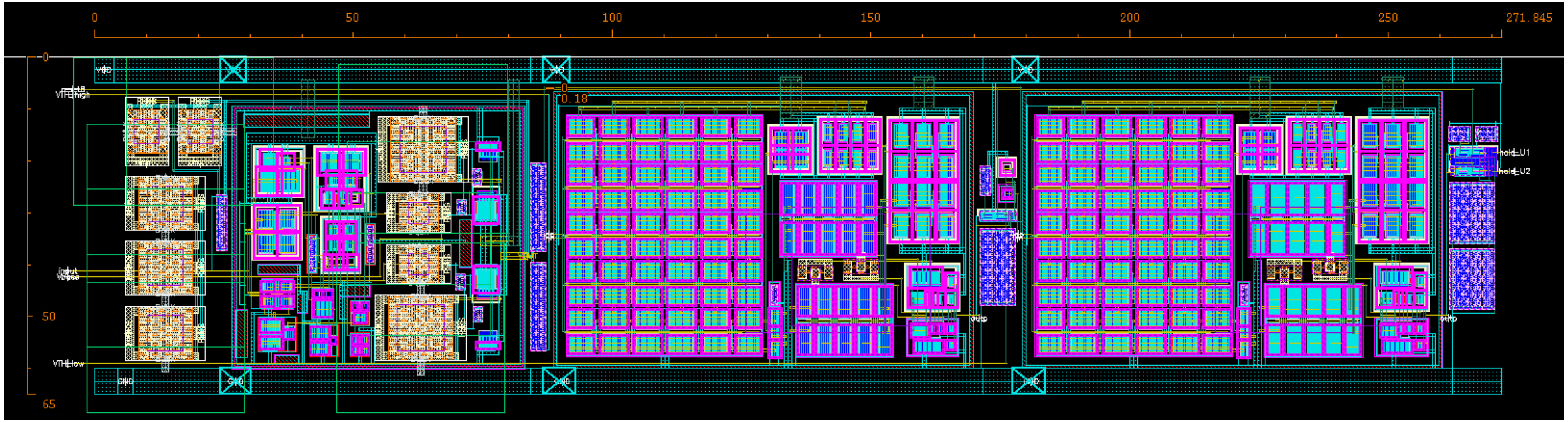
Current Schematic Simulation

T B D (P,V,T) RoomTemp and LArTemp –> then Layout & Extract



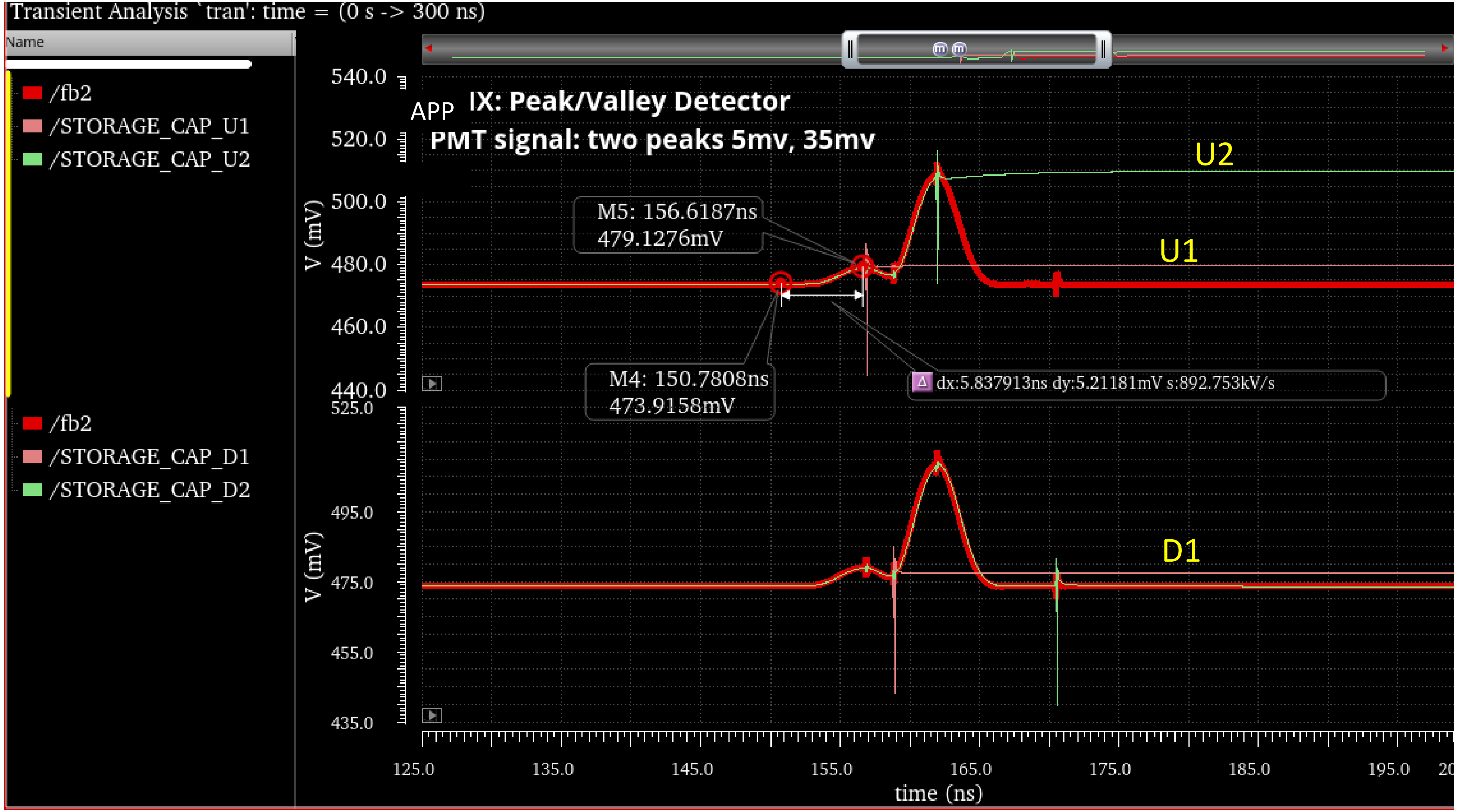
Peak Detection (Schematic & Layout)





Peak Detector Full TSMC 65 nm Model Simulation

U = peak D= Valley



Status & Summary

We are currently assembling circuit blocks into a single channel and fine tuning the Charge integrator Ping/Pong mechanism and associated several ns analog delay.

TBD Chip level readout Architecture and the digital part of the back end is.

Summary

The Analog Photon Processor ASIC is being developed in response to recent improvements in Single Photo Electron sensitivity and signal uniformity (both time precision and charge) in Photomultiplier Tubes.

The APP will target use in low photon statistics underground neutrino detectors offering a cost effective readout that takes advantage of low cost COTs 2Msps ADC's or existing IP and FPGA readout & control where possible utilizing ASIC design resources to develop sub nanosecond precision analog feature extraction with 10-12bit analog accuracy well suited to modern PMT's with excellent SPE characteristics.

In comparison to waveform digitization **Low Data Rate neutrino** experiments will benefit from

- Lower per channel cost for Readout electronics
- Lower operating power due to a reduction in the required front end clock rate by ~ 10+ ***2GHz → ~ 50MHz*** reduction in the data stored per self triggered event
- Smaller Self Triggered Event data/PMT: **21 bytes of data***

* Header + 8,12bit words Analog ADC + 4,16 bit counter data + 8bits + mem@ → **~21** 8b-10b encoded words, **420ns @ 50MHz**