

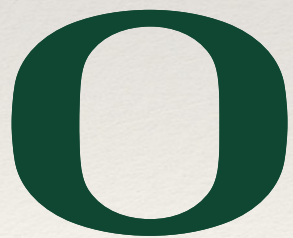


*November 19, 2024*

# The SiD Digital ECal Based on Monolithic Active Pixel Sensors

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University of  
Oregon

on behalf of  
the SiD MAPS Collaboration  
(M. Breidenbach, A. Dragone,  
L. Rota, M. Vassilev, C. Vernieri,  
J.B. et al.)



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OREGON

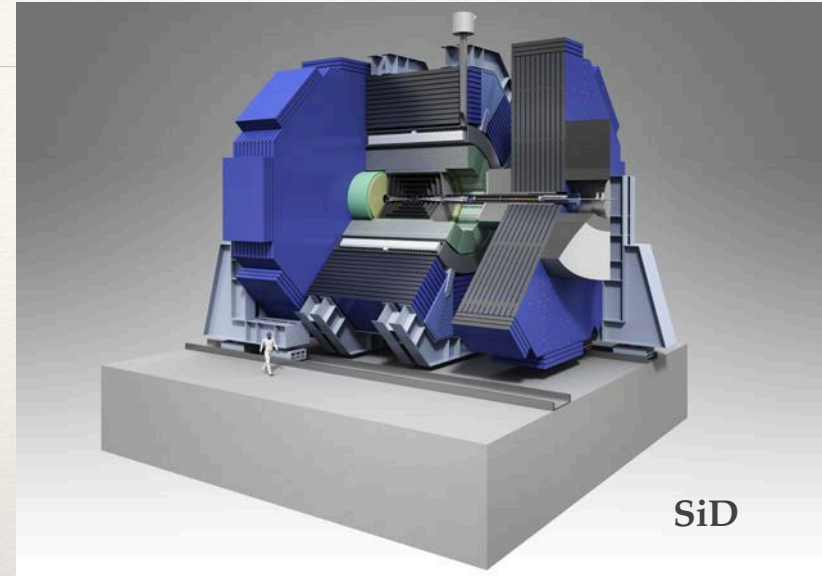
Research partially supported  
by the U.S. Department of Energy

"The SiD Digital ECal Based on Monolithic Active Pixel Sensors",  
10.3390/instruments6040051, Instruments, 6, 51 (2022)



# SiD Digital ECal Based on MAPS

- ❖ SiD upgrade now under development with  $25 \times 100 \mu\text{m}^2$  (or  $25 \times 50/25 \mu\text{m}^2$ ) digital pixels in electromagnetic calorimeter and tracker.
  - ❖ Replacing the ILC TDR ECal design based on  $13 \text{ mm}^2$  analog pixel sensors.
- ❖ Heat management is critical to success.
  - ❖ FCC/CEPC solution?
- ❖ How well can we measure energy and shower structure with this digital system:
  - ❖ Compared to SiD baseline with analog measurements?
  - ❖ Can the detailed structural measurements be used to improve measurement?
  - ❖ Would a neural net optimization offer an improvement?
- ❖ What are the limits of transverse separation and measurement?



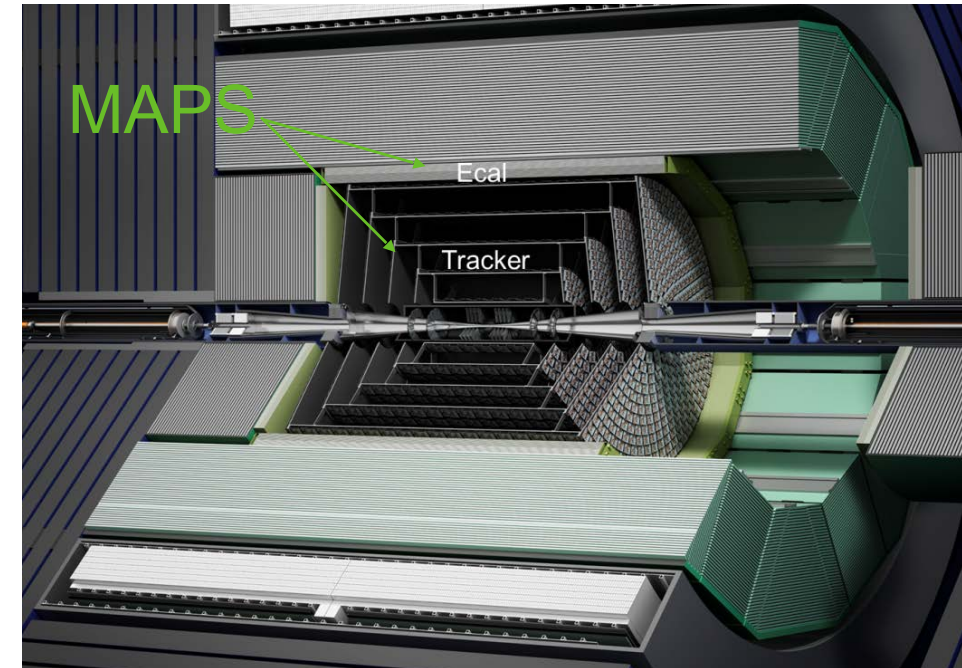
# Large area MAPS for SiD tracker & ECal

## Benefits of large-area MAPS:

- Standard CMOS foundry, low resistivity: **cost** ↓
- Sensing element and readout electronics on same die
  - In-pixel amplification: **noise** ↓, **power** ↓
  - No need for bump-bonding: **cost** ↓
- Area > **5x20** cm<sup>2</sup> → enable O(1) m<sup>2</sup> modules

## Several design challenges:

- Large on-die variations, mismatch
- Yield
- Stitching layout rules
- Distribution of power supply
- Distribution of global control signals/references



An example of the SiD Tracker and the ECal overall design

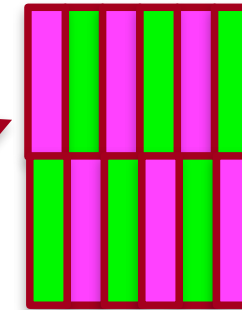
**Goals of R&D: find solutions and explore novel design techniques**

SLAC collaborating with  
CERN WP1.2 efforts

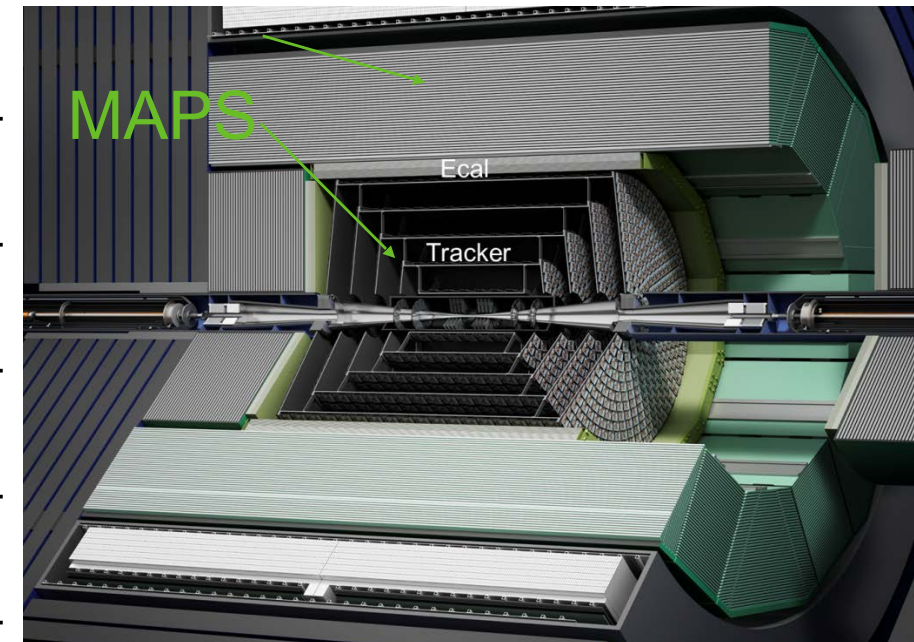
# Main specifications for Large Area MAPS development

L. Rota

Parameter	Value	Notes
Min Threshold	140 e <sup>-</sup>	0.25*MIP with 10 μm thick epi layer
Spatial resolution	7 μm	In bend plane, based on SiD tracker specs
Pixel size	25 x 100 μm <sup>2</sup>	Optimized for tracking (or 25x50/25 μm <sup>2</sup> )
Chip size	5 x 20 cm <sup>2</sup>	Requires stitching on 4 sides
Chip thickness	300 μm	<200 μm for tracker. Could be 300 μm for ECal to improve yield.
Timing resolution (pixel)	~ ns	Bunch spacing: C <sup>3</sup> strictest with 5.3->3.5 ns; ILC is 554 ns
Total Ionizing Dose	100 kRads	Total lifetime dose, not a concern
Hit density / train	1000 hits / cm <sup>2</sup>	
Hits spatial distribution	Clusters	Due to jets
Balcony size	1 mm	Only on one side, where wire-bonding pads will be located.
Power density	20 mW / cm <sup>2</sup>	Based on SiD tracker power consumption: 400W over 67m <sup>2</sup>



25 x 100 μm<sup>2</sup>  
ECal performance same as 50 x 50 μm<sup>2</sup>



SiD Tracker and the ECal

<1 mW/cm<sup>2</sup>  
for 1% duty cycle

# Large Area MAPS - Highlights and Next Steps

## Approach:

- Focus on long-term R&D, targeting simultaneously:
  - ~ns timing resolution
  - Power consumption compatible with large area and low material budget
  - Fault-tolerant circuit strategies for wafer-scale MAPS

## Highlights:

- 1st SLAC prototype on TJ65nm (2023) from CERN WP1.2 shared run
- Performance of 1st SLAC prototype on TJ65nm (2023) evaluated

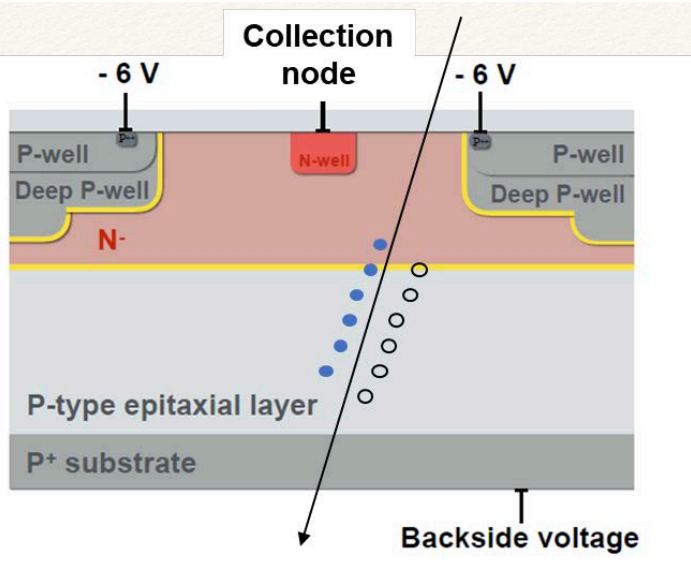
## Next steps:

- New design combining O(ns) timing precision and low-power (2024/2025).
- **Stretch Goals:** design of a wafer-scale ASIC (2025/2026, design only)

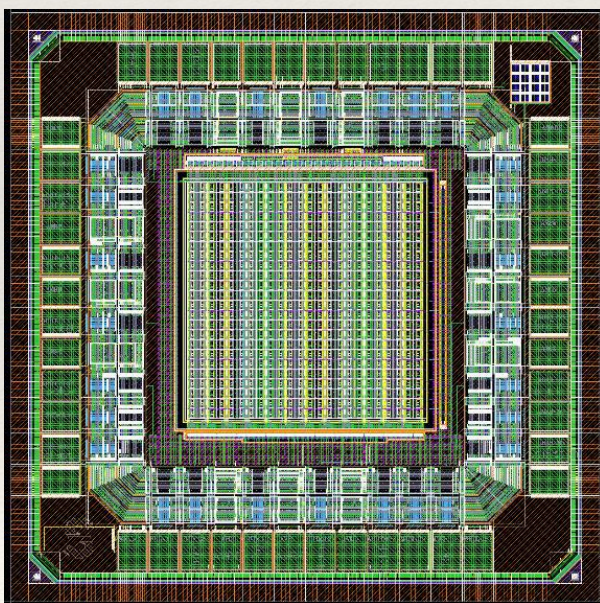
## Engagement :

- Higgs Factory detector initiative R&D
- DRD 3 silicon sensors
- DRD 7.6 on common issues of power distributions compatible with stitching

A. Habib *et al* 2024 *JINST* **19** C04033  
C. Vernieri, MAPS DRD 3.1 talk



Current sensor optimization in TJ180/TJ65 nm process  
Effort to identify US foundry on going



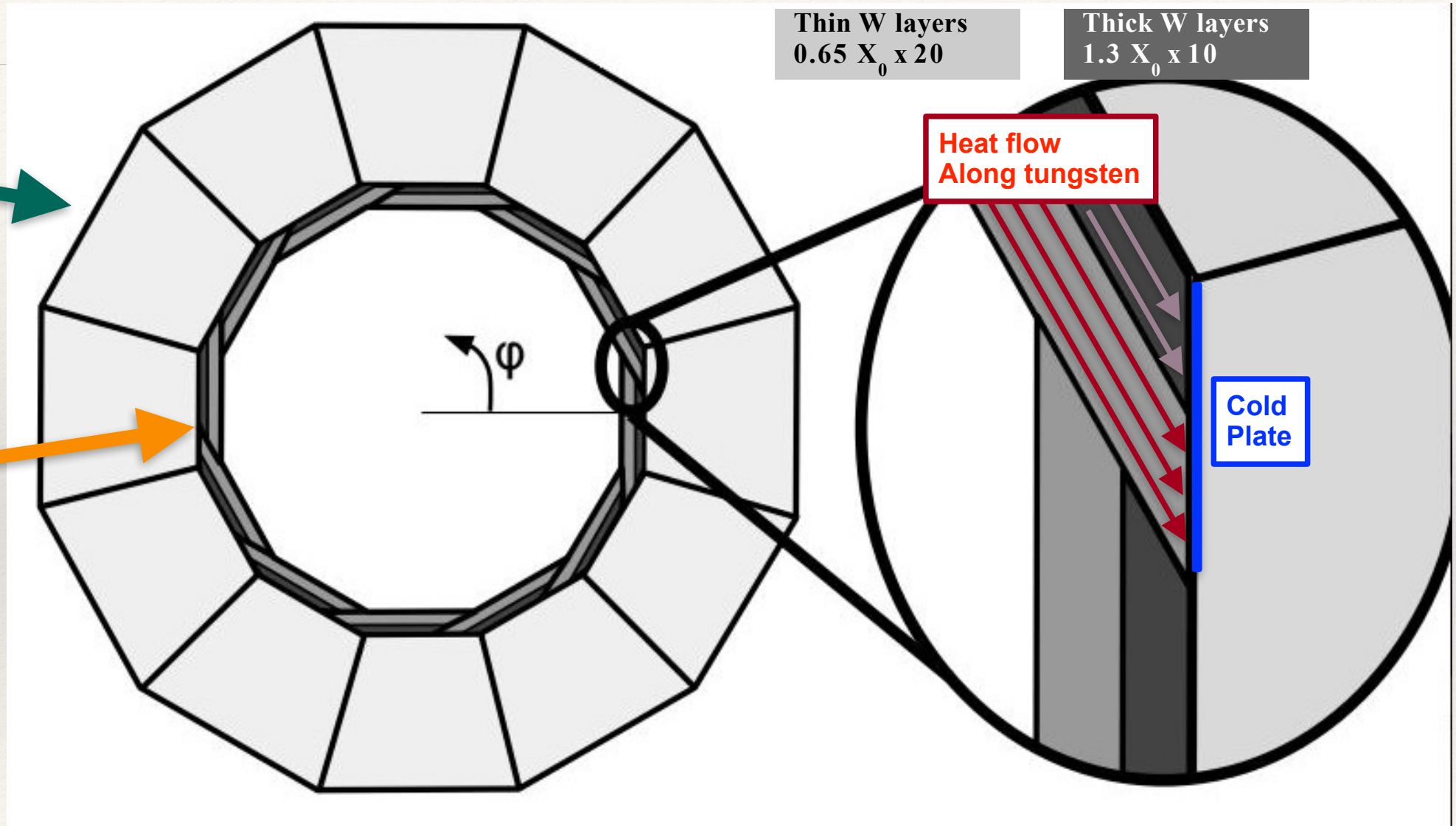
Layout of SLAC prototype for WP1.2 2022  
shared submission on TowerSemi 65nm



# SiD Calorimeter Barrel Geometry

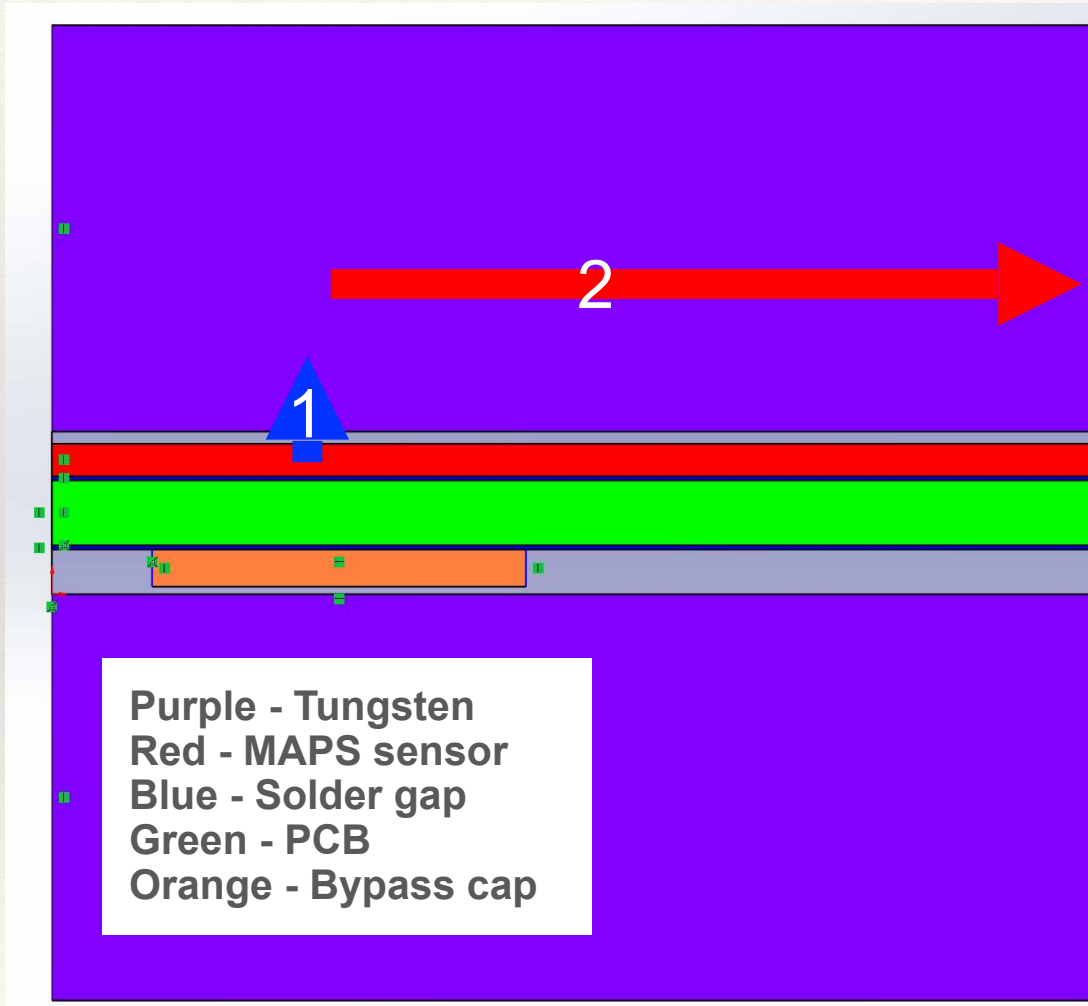
**HCal**  
Scintillator sampling  
Steel/polystyrene

**ECal**  
Solid state sampling  
Tungsten alloy/MAPS  
Built on first layer of HCal





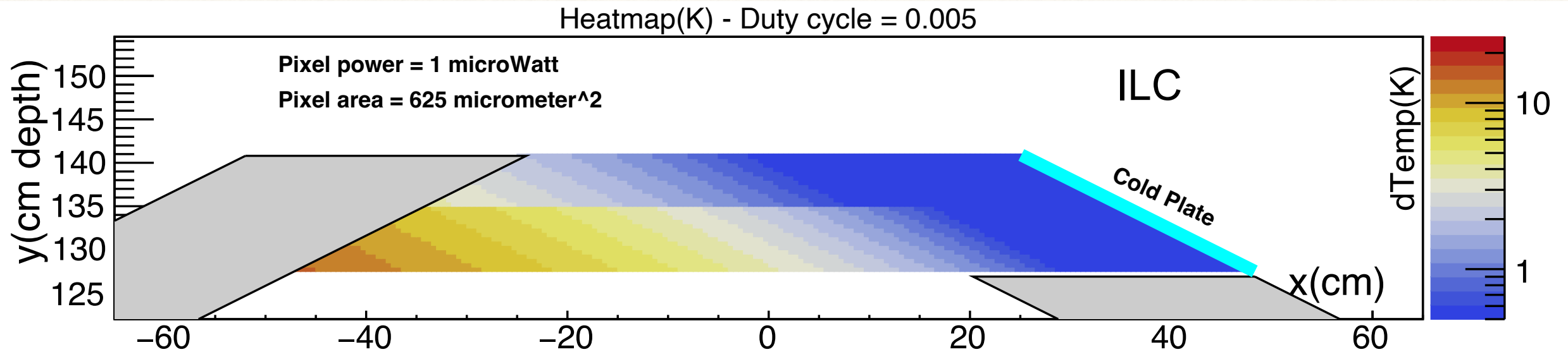
## Heat conduction from ECal sensor to cold plate



- ❖ MAPS generates  $\sim \text{kW/m}^2$  (each sensor is  $100 \text{ cm}^2$ )
- ❖ First heat flows through  $300 \mu\text{m N}_2$  to tungsten
  - ❖  $\Delta T \ll 1 \text{ K}$
- ❖ Then heat flows thru tungsten to cold plate
  - ❖ Tungsten absorber lengths  $0.5\text{-}1.0 \text{ m}$
  - ❖ Temperature rise is length dependent
- ❖ Duty cycle -  $0.07\%$  (C3/CLIC) -  $\Delta T \sim 0.5 - 2 \text{ K}$
- ❖ Duty cycle -  $0.5\%$  (ILC) -  $\Delta T \sim 4 - 16 \text{ K}$ 
  - ❖ Without power pulsing temperature blows up and needs active cooling



# Heat conduction from ECal sensor to cold plate



- ❖ Duty cycle - 0.07% (C3/CLIC) -  $\Delta T \sim 0.5 - 2 \text{ K}$
- ❖ Duty cycle - 0.5% (ILC) -  $\Delta T \sim 4 - 16 \text{ K}$
- ❖ **Without power pulsing** temperature blows up and needs **active cooling**
  - ❖ such as for FCC/CEPC

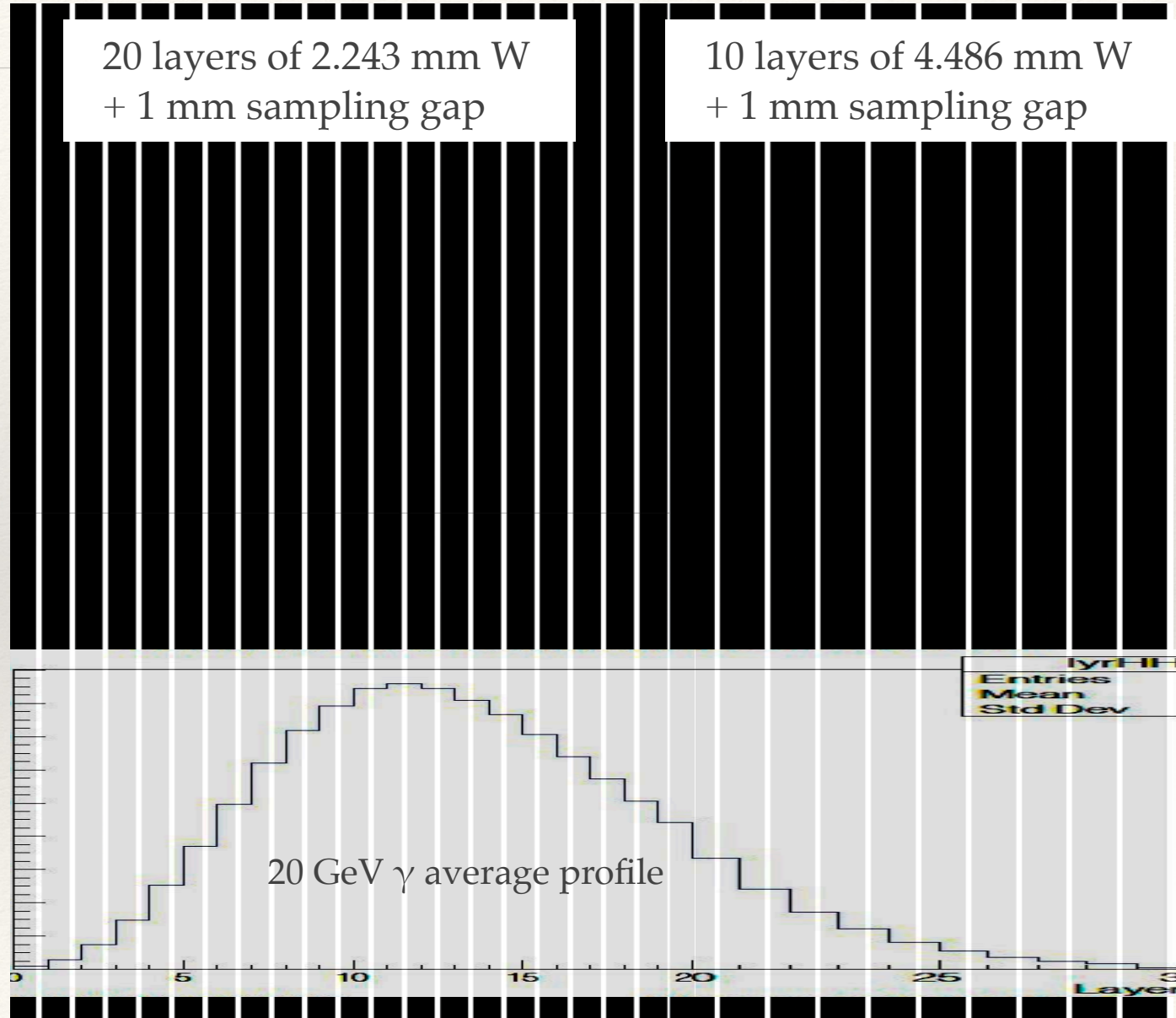


# Model of longitudinal structure of SiD ECal

Total =  $27 X_0$



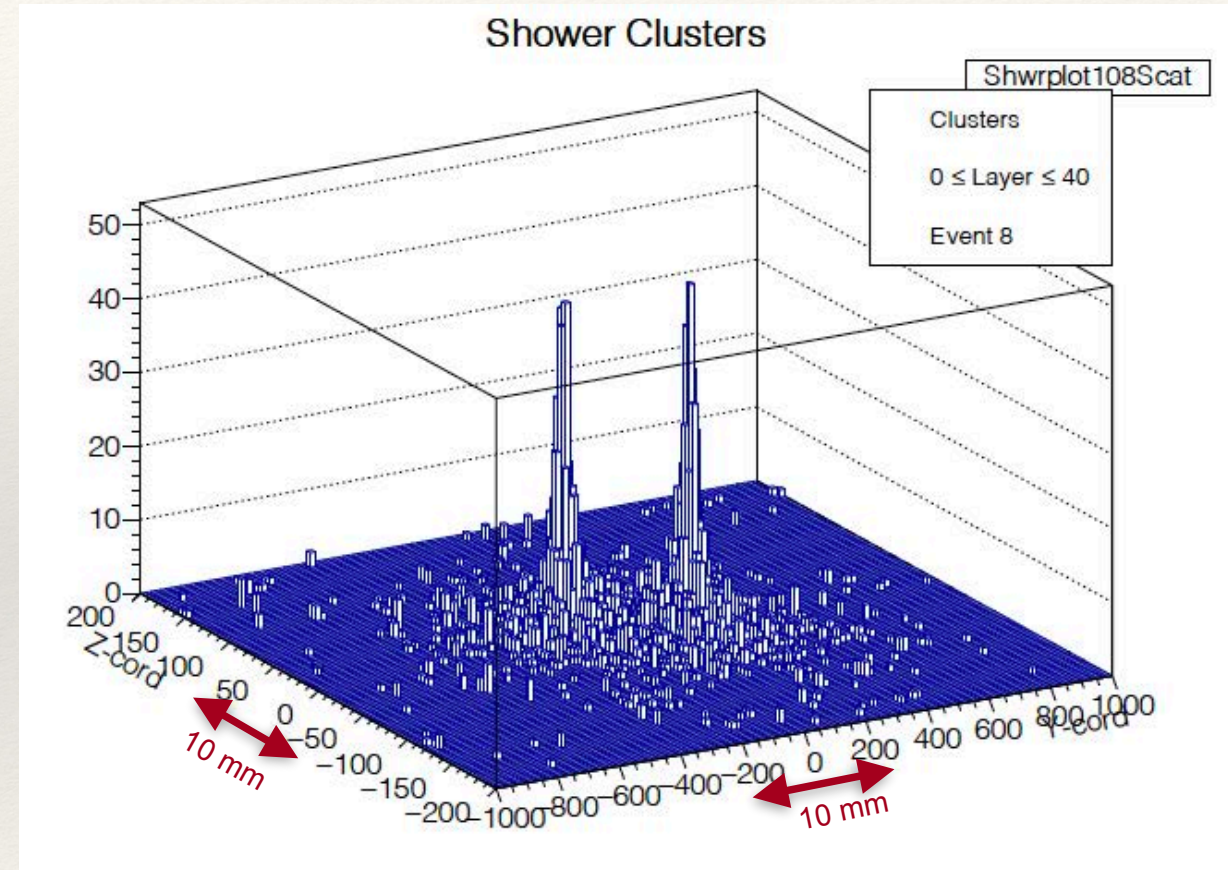
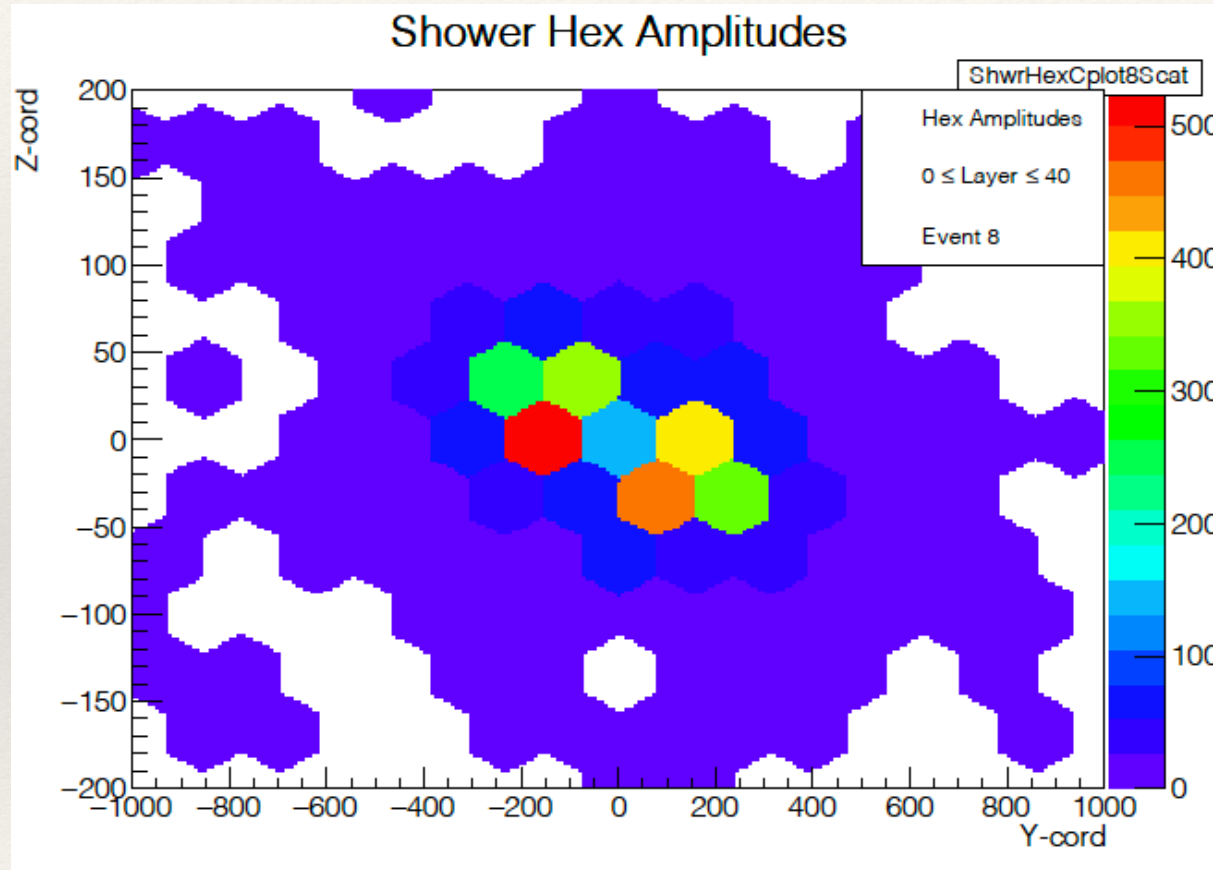
Minimize sampling gap to achieve optimal Moliere radius (14 mm) & shower separation



HCAL

# Multi-shower of SiD MAPS compared to SiD TDR

40 GeV  $\pi^0 \rightarrow$  two 20 GeV  $\gamma$ 's



SiD TDR hexagonal sensors  
13 mm<sup>2</sup> pixels

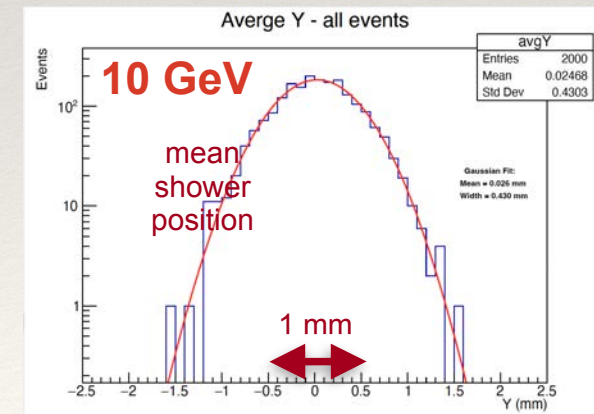
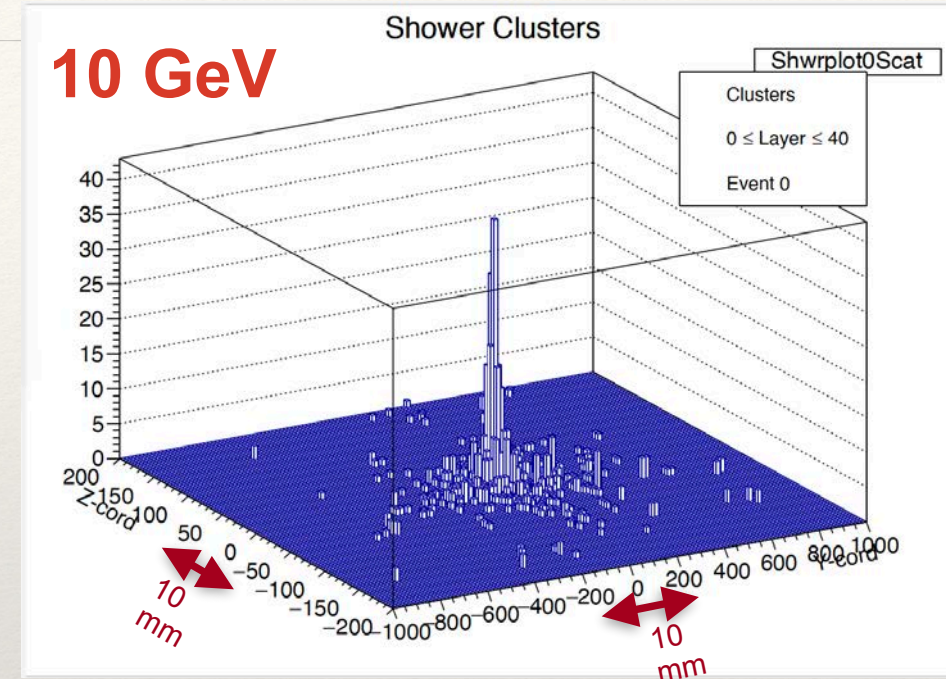
Illustrates PFA  
Potential

New SiD fine pixel sensors  
25  $\mu$ m x 100  $\mu$ m pixels



# Shower transverse position measurement

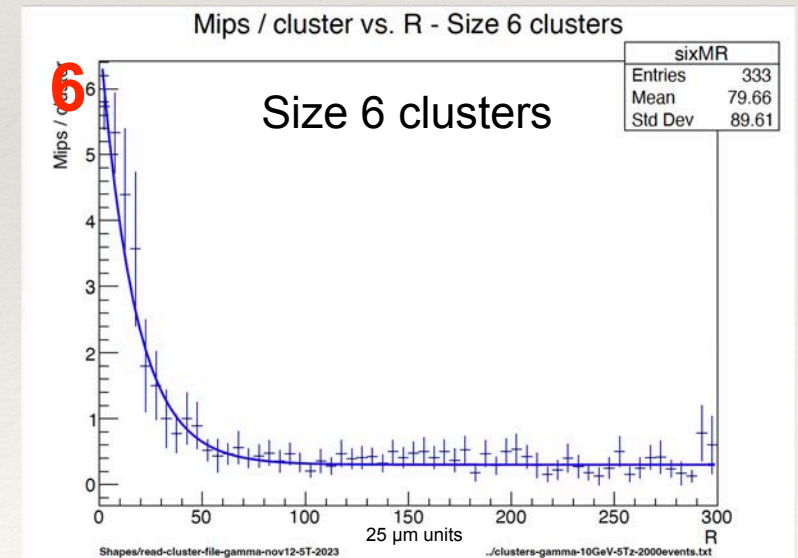
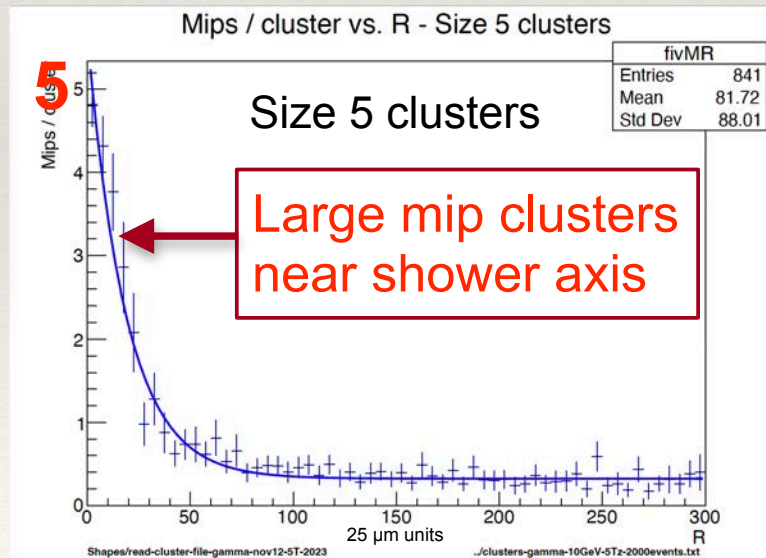
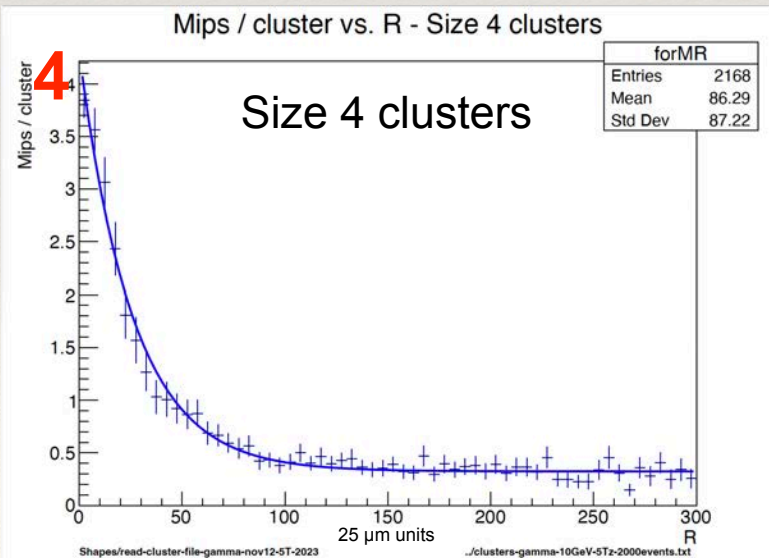
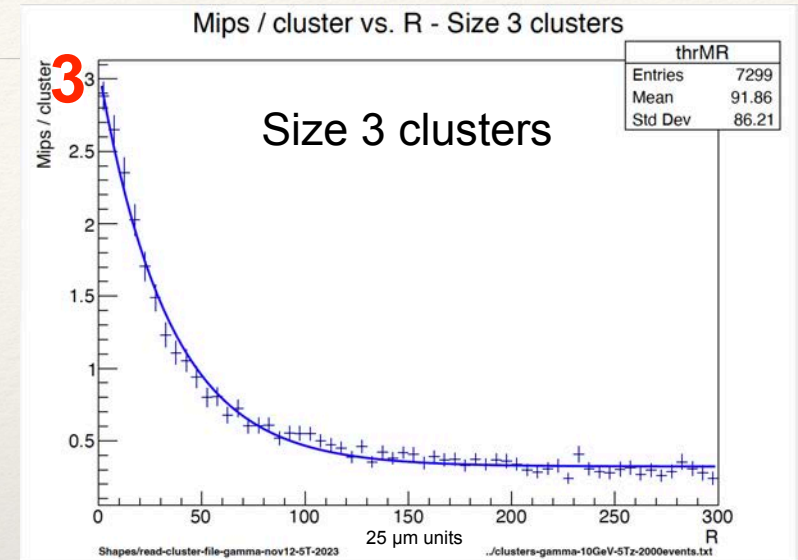
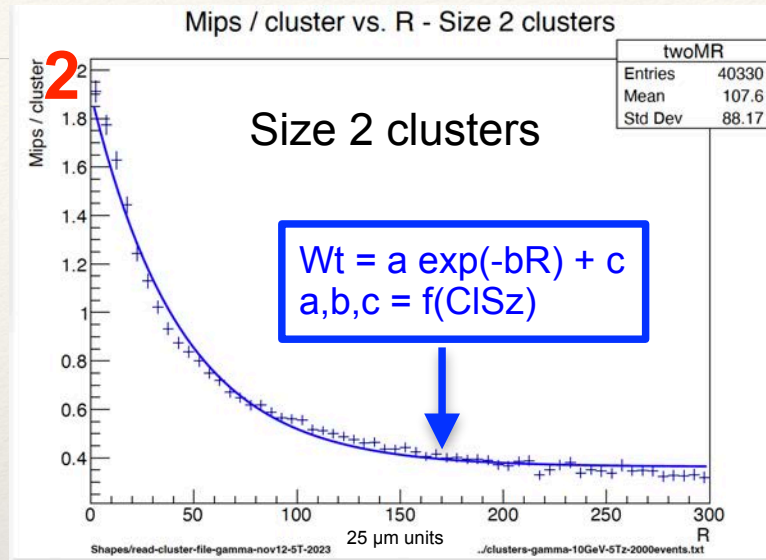
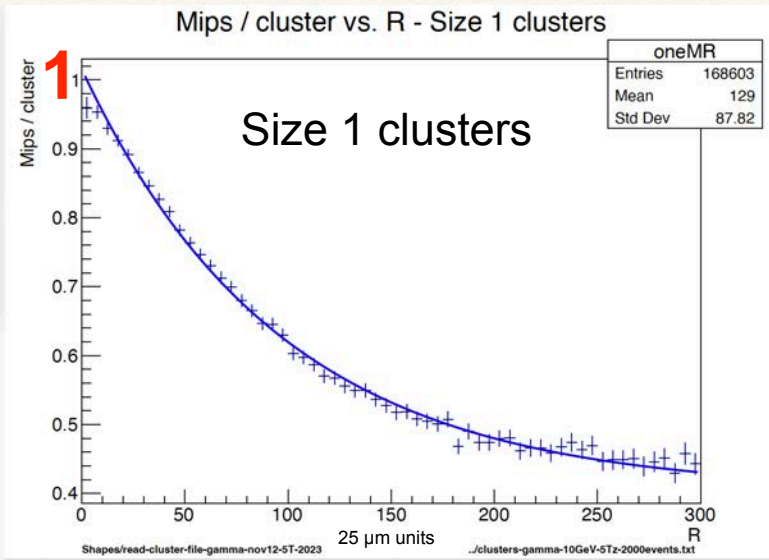
	Simulated measurements			
	Y-spread (rms)	Z-spread (rms)	$\delta Y$	$\delta Z$
1 GeV	4.7 mm	4.2 mm	1.17 mm	1.04 mm
10 GeV	4.8 mm	4.3 mm	0.43 mm	0.37 mm
50 GeV	5.1 mm	4.6 mm	0.21 mm	0.20 mm



- ❖ This precision can be improved - naive, simple average used
- ❖ Important for jet particle flow measurements

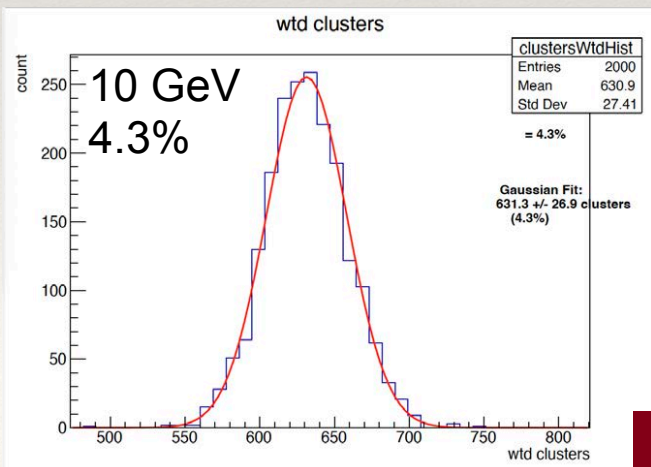
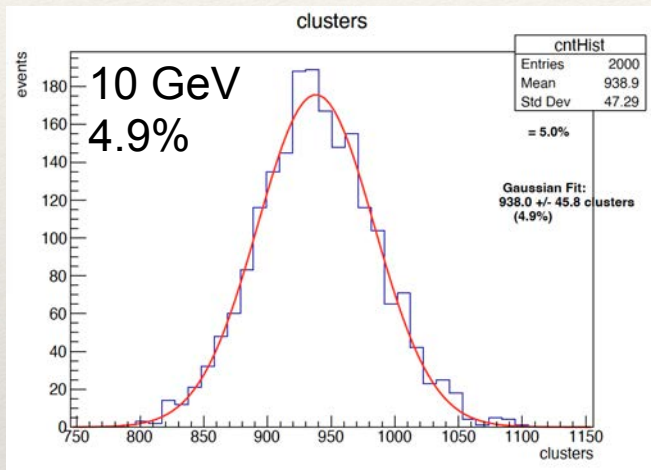


# Mips/cluster vs. showerR 10 GeV $\gamma$ s - 2000 showers

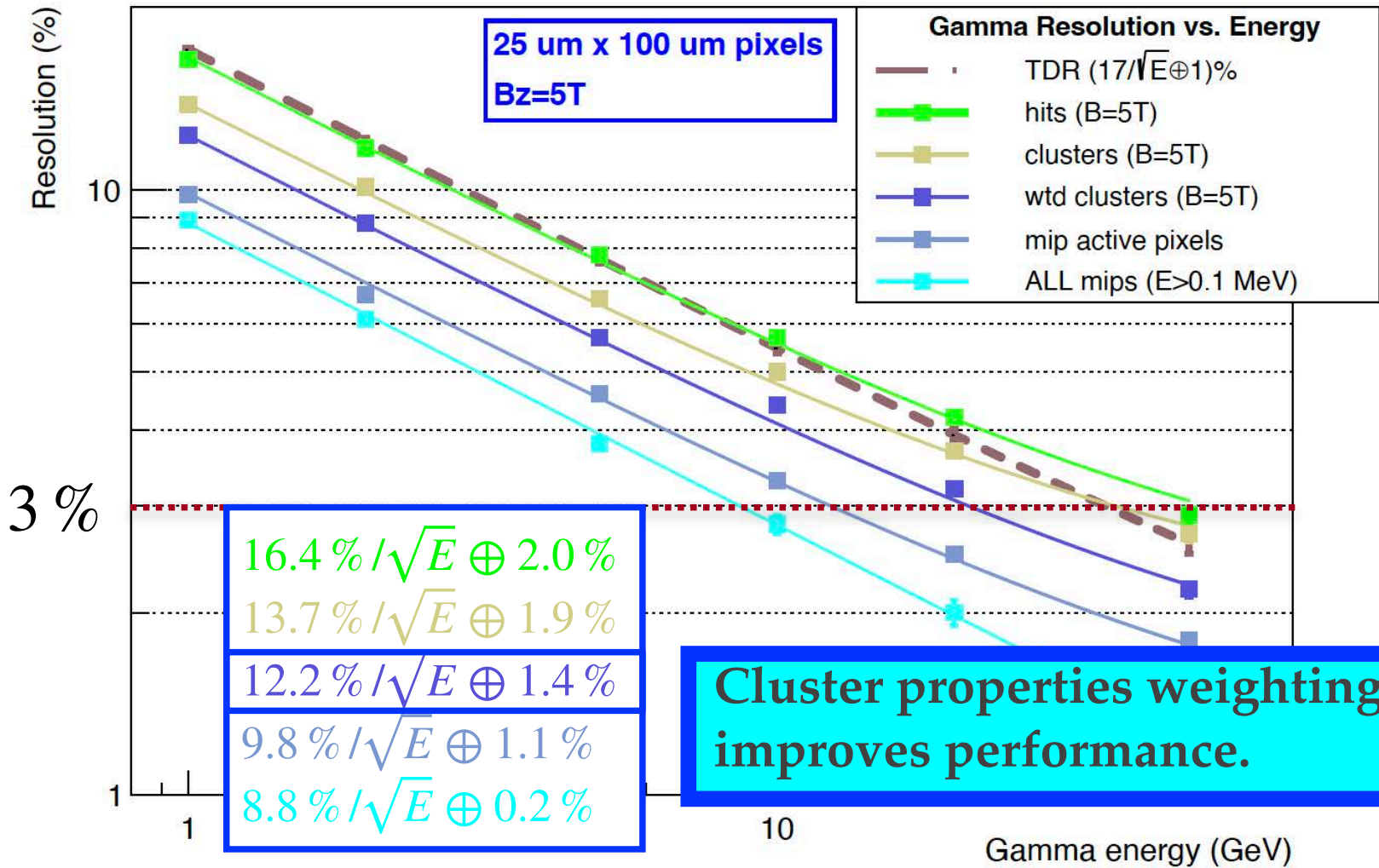


# Resolution vs. Energy (hits/clusters/mips)

Resolution vs. Energy  
(hits / clusters / mips)  
& weighted clusters.



## Gamma Resolution vs. Energy (B=5T)



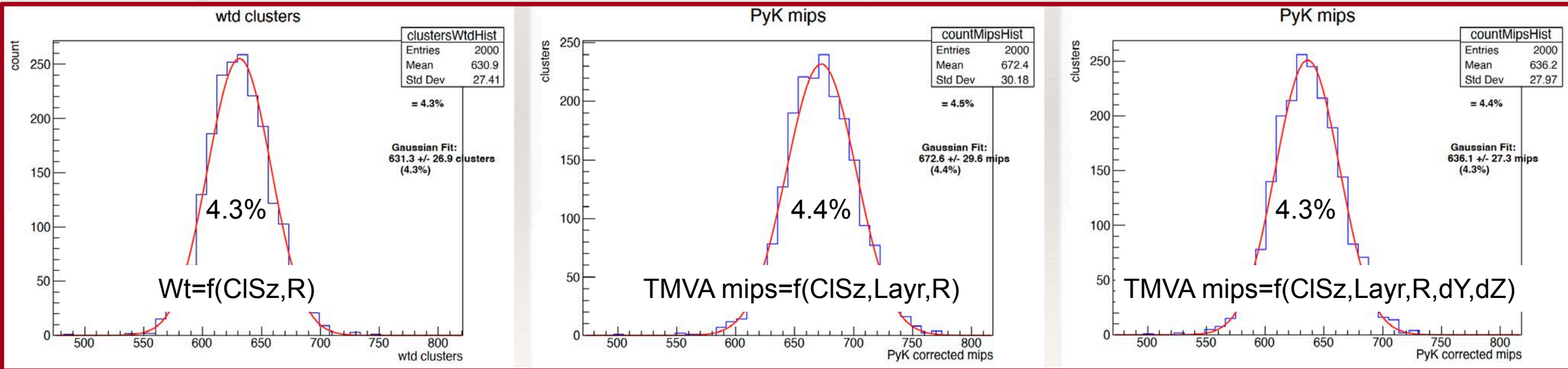
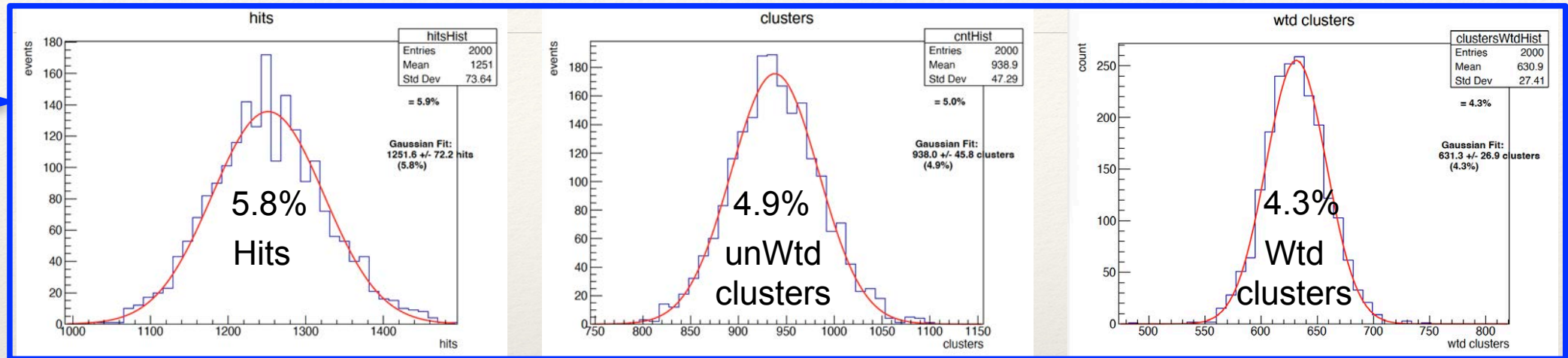
Can a Neural Net Improve Performance?



# Weighted function vs. TMVA neural net (10 GeV $\gamma$ s)

Weighted Clusters Analysis

Neural Net Analysis





# Results: Energy Resolution

Energy	1	2	5	10	20	50
clusters	13.8%	10.1%	6.6%	4.9%	3.7%	2.7%
wtd clusters	12.3%	8.8%	5.7%	4.4%	3.2%	2.2%
3 par TMVA	12.6%	9.5%	6.2%	4.4%	3.4%	2.2%
5 par TMVA	12.8%	9.4%	5.9%	4.3%	3.1%	2.2%

- ❖ Weight fits for 2, 10, 50 GeV; extrapolated for 1, 5, 20 GeV.
- ❖ NN optimized for each energy
- ❖ 3 par = cluster size, layer, radius
- ❖ 5 par = cluster size, layer, radius, dY, dZ

Weighted clusters already achieve performance of this neural net.



## Conclusion

- ❖ Application of monolithic active pixel sensors (MAPS) to SiD digital ECal offers excellent performance:
  - ❖ Energy measurement
  - ❖ Transverse energy containment & particle flow separation
- ❖ Well defined EM shower structure allows simple algorithmic optimization of energy measurement.
- ❖ An effort led by SLAC is progressing on the needed MAPS development.
- ❖ Neural nets have been studied to improve energy measurement:
  - ❖ They have not yet provided improvement over the “informed” algorithm.
- ❖ Passive heat management works for linear colliders given the very low duty cycle.
  - ❖ FCC/CEPC solution?
- ❖ The digital ECal will add valuable performance for particle flow reconstruction.
- ❖ Future - simulation of full SiD detector with high granularity of MAPS ECal.



# Extras

