



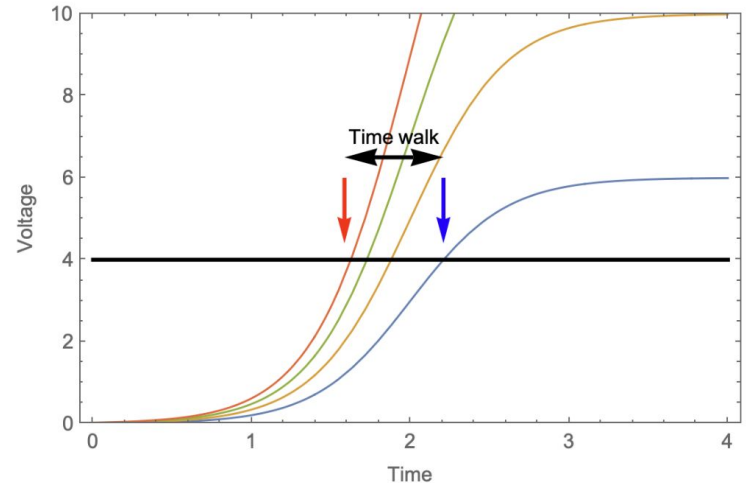
Second-Generation Fermilab CFD Readout ASIC for LGAD sensors

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CPAD Meeting 2024

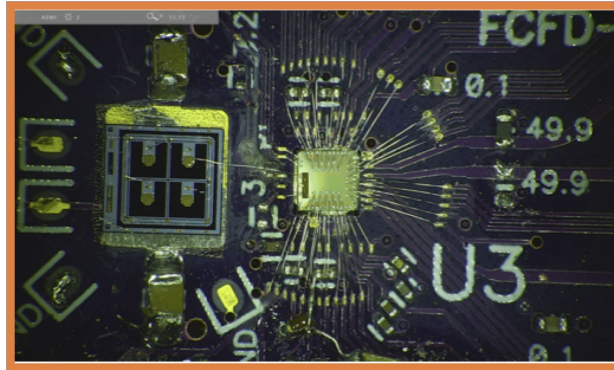
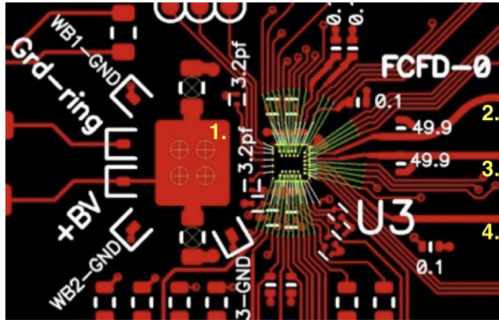
Hardware-enabled CFD Readout for Timing Detectors

- Time-walk effect is well known & must be corrected for best performance
- Conventionally addressed with online or offline corrections via some type of LUT
- But under harsh radiation environments of future colliders, corrections may be time-dependent and messy!
- We propose a **hardware-enabled correction** via CFD built into the readout ASIC design



Fermilab CFD (FCFD) Chip

- Primary application is (AC-)LGAD sensors for MIP signals
 - But can be used for many types of precision timing detectors
- Previous version of the FCFD chip and performance presented at CPAD 2023 : <https://indico.slac.stanford.edu/event/8288/contributions/7544/>



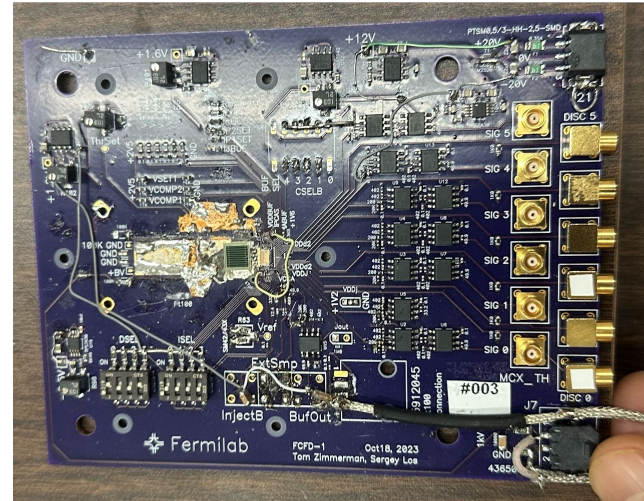
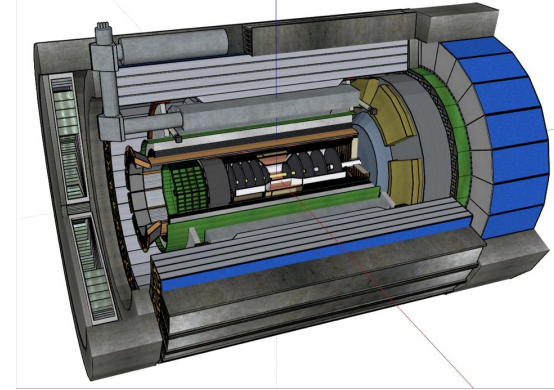
Published here: Xie et al., NIM-A V1056 168655 (2023)
<https://doi.org/10.1016/j.nima.2023.168655>

FCFD v1: 2nd-Gen ASIC

- New Features:
 - 6-channel readout
 - Design targets EIC TOF barrel detector AC-LGADs
 - 1cm long AC-LGAD, 500 μm pitch, 50 μm thickness
 - Wider dynamic range
 - Sensitivity to smaller signals
 - Additional signal amplitude readout for position measurement

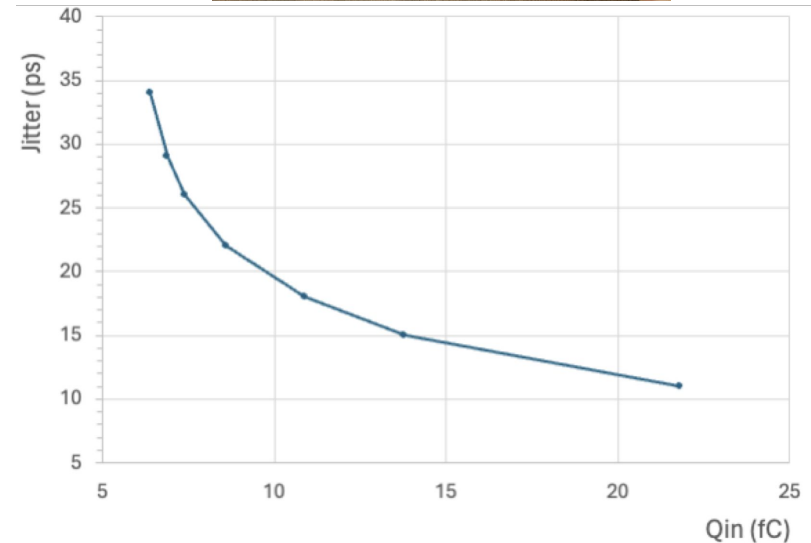
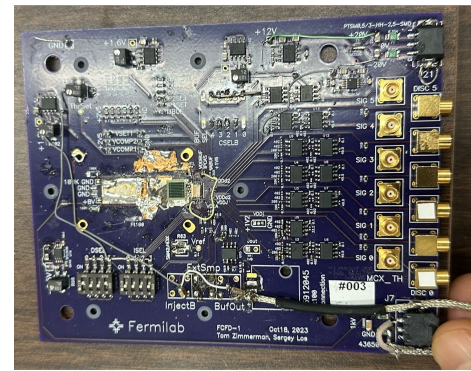


Barrel TOF
AC-LGAD



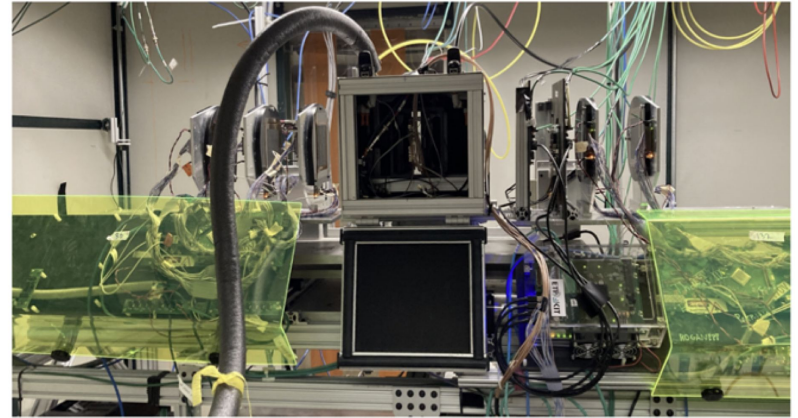
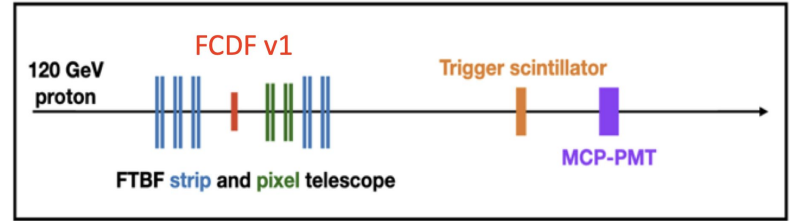
FCFD v1: Charge Injection Characterization

- Use internal LGAD-like signal charge injection mechanism (same as v0)
- Achieved 11 ps time resolution with input capacitance at 3.5 pF
- Analog output linear over range of input charge between 7-60 fC



Fermilab Testbeam Facility Setup

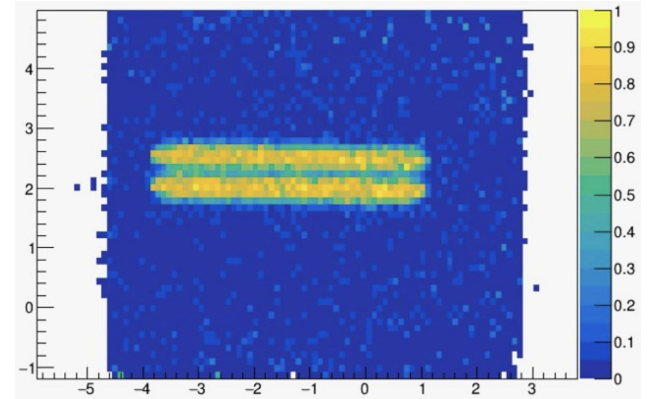
- Use 120 GeV protons to characterize FCDFv1 in realistic operating conditions
- Tracking provided by 5 layers of strip silicon sensors and 2 layers of pixels
- Reference time measured by MCP-PMT (~10ps resolution)
- Maintain temperature at 20 C



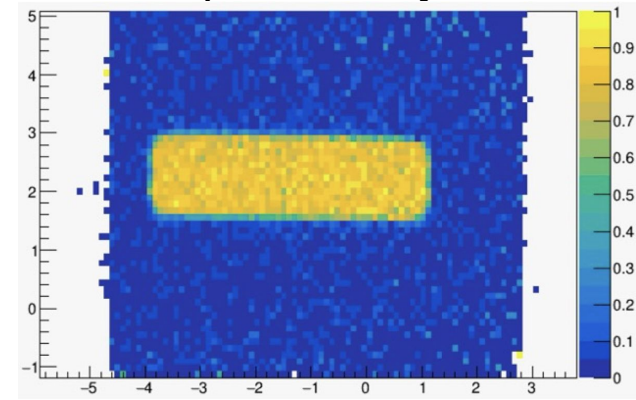
Beam Test Results

- Two-strip efficiency at 100%
 - Initial noise levels were high
 - Comparator misled by fake noise hits
-
- Temporary solution:
 - Added 7-pF capacitor in series to the AC-LGAD to mitigate noise (at cost of signal strength reduction)
 - Also tested FCFDv1 with 2-pixel DC-LGAD to verify design performance specifications

Single -channel efficiency

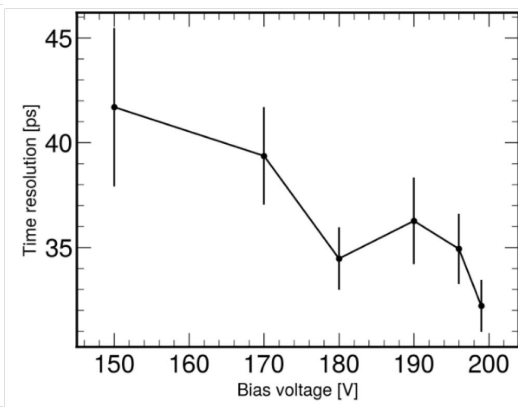
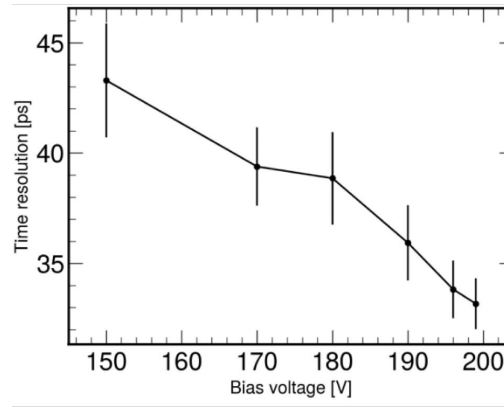


two-strip efficiency



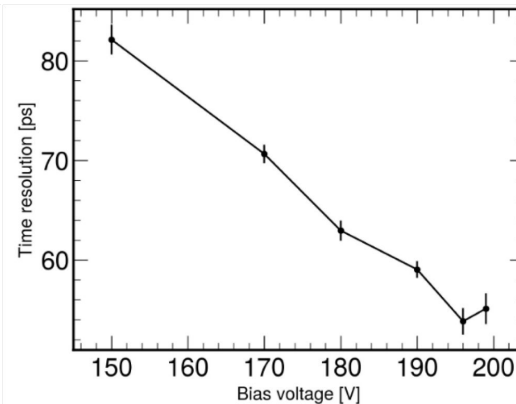
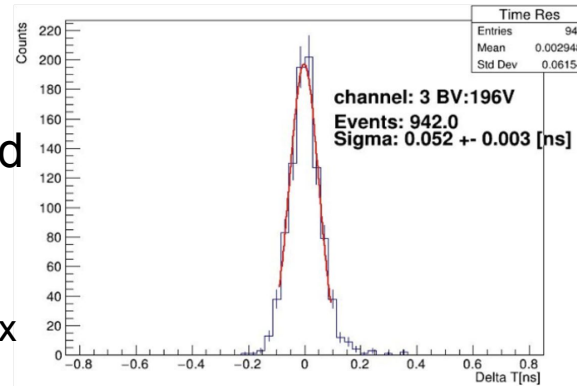
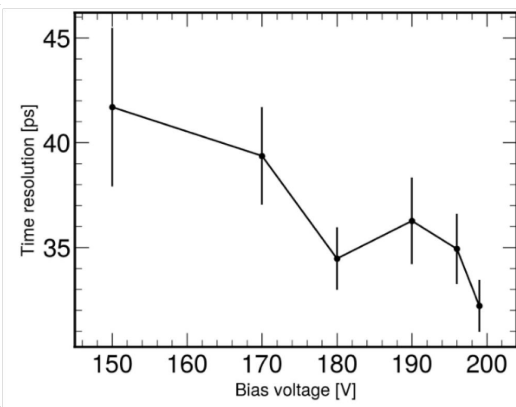
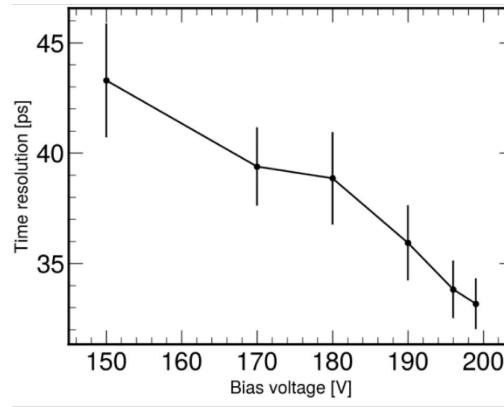
Beam Test Results

- Confirmed performance on DC-LGAD matches design specifications
 - Achieved 32 ps total resolution (for amplitude $\sim 300\text{mV}$)
 - No time-talk observed



Beam Test Results

- Confirmed performance on DC-LGAD matches design specifications
 - Achieved 32 ps total resolution (for amplitude $\sim 300\text{mV}$)
 - No time-talk observed
- AC-LGAD resolution measured to be 52 ps
 - For smaller signal amplitude 130 mV due to the temporary noise fix



Summary

- Presented performance of 2nd-Gen FCFD ASIC optimized for EIC AC-LGAD applications
- For DC-LGAD, performance matches design specifications
- For AC-LGAD, larger noise observed and temporary fix resulted in slightly worse timing performance due to attenuated signal size

- Next steps:
 - Working on re-design of RC-coupling, accounting for sensor parameters
 - Design of full size FCFD v2 ASIC with EIC-DAQ compatible readout

Backup