OAK RIDGE National Laboratory

Schedule and Discussion

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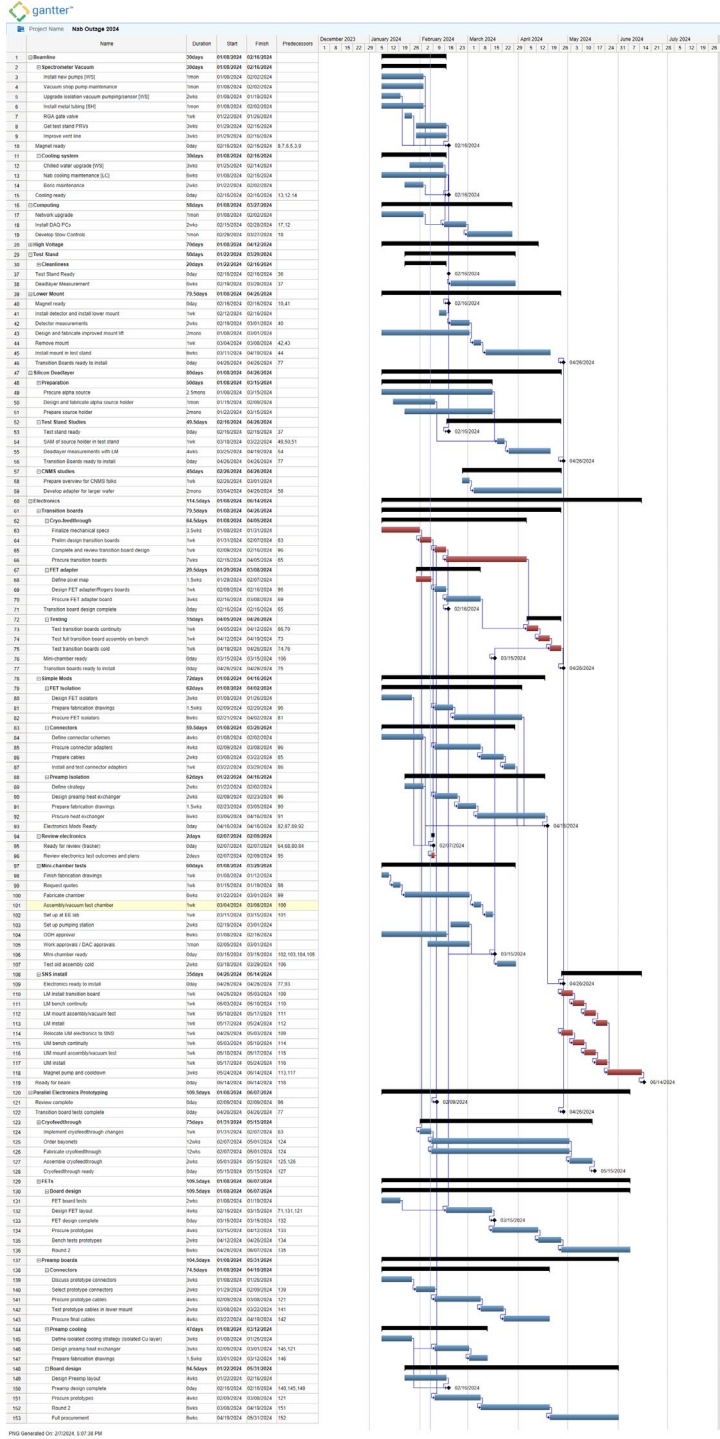
8 Feb 2023

U.S. DEPARTMENT OF ENERGY

Outage Schedule

- Outage activity schedule supported by gantt chart
  - Electronics activities (esp. transition board redesign) represent critical path
- Investigate oscillations: December – March
  - Prepare mini-chamber for cold tests: ready mid-March
- Design and test transition boards: January - April
  - **[MILESTONE]** Transition Board design approved February 16
  - Fabricate and test transition boards: mid-February through April
- Prepare for SNS beamtime
  - Reinstall detector systems: May
  - **[MILESTONE]** Magnet cold: June 14
  - Detector calibrations: 2nd half June
  - **[MILESTONE]** Ready for SNS beam-on: July 4



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Charge Items

- **Stability investigation**: Suggestions from the reviewers for further investigation and interpretation of results are appreciated
- **Remediation strategy**: Is the proposed strategy the one most likely to meet the immediate and long-term goals of the Nab experiment?
- **Pixel mapping improvements**: We request a mail review of the design before it is procured.

Reminder: October Review Recommendations

1. **Investigation and Optimization of System Ground, Power, and Signal Connectivity (HIGH)**

A detailed system connectivity diagram must be developed showing all ground (earth ground, power ground, signal ground), power, and signal connections. The system circuit diagram is a very important tool for understanding the present detector electronics and for planning and discussing necessary improvements. A detailed analysis will result in specific action items for improved ground, power, and signal routing/connectivity that will optimize system stability and general detector system performance, including cooling system modifications that remove contact to electronic grounds (potential ground loops). This analysis will also extend to the printed circuit board (PCB) level and will involve detailed analysis of the PCB ground and power partitioning, routing, and connectivity to system components external to the PCB.

2. **System Specifications Refinement (HIGH)**

A clear list of electronics specifications must be developed for the detector amplifier channels including rise time, noise, and gain. A study of the analog signal produced by the preamplifier must be performed, supported by simulations, to provide the maximum rise time (or minimum bandwidth) required to meet the physics goals of the experiment. Any reasonable reductions in channel bandwidth/rise time will improve the channel stability and move the systems towards more stable operations.

Reminder: October Review Recommendations

3. Bench Testing of Hardware (HIGH)

A thorough testing of the detector electronics is a pre cursor for identifying and implementing successful improvements. Two levels of bench testing must be performed for better understanding of the observed electronics issues, leading to realizable design modifications:

***a) Single Electronics Channel Bench Testing* (HIGH)**

The following boards and combinations of boards need to be carefully evaluated on the bench:

- FET amplifier PCB
- Preamplifier PCB
- Combined FET Amplifier – Preamplifier PCBs. Each FET amplifier PCB includes 8 channels, and each Preamplifier PCB includes 6 channels. The way grounds can be separated is limited. Care must be taken to prevent undesired mixing of the grounds and to prevent the introduction of channel crosstalk.

In addition to operating each board channel separately, all channels on a single board must be operated simultaneously as well.

These tests should be set up to best emulate the actual detector channel connectivity including detector input signals, parasitic capacitance and inductance, realistic power supplies, impedance loading effects, and the effect of the single input pulser.

The testing must be performed in a qualified electronic laboratory space.

b) ***Electronics Assembly Testing* (HIGH)**

A detector subsystem bench setup including either a full upper or lower detector assembly (128 upper or 128 lower), a full complement of preamplifier channels (128 upper or 128 lower), data acquisition electronics (full system), and high voltage (HV) and low voltage (LV) power supplies collectively provide an acceptable setup. As this may not be practical, at least an upper or lower detector assembly with associated electronics (128 channels, without HV) should enable regeneration of the oscillatory behavior of the system observed during commissioning data collection. If time allows, the HV may be added as a second phase of testing. A 'clean' laboratory space will be required to support these aggressive testing goals and will need to permit 30kV supply use and cryogenic operations. Since the detector mounts are likely too cumbersome to operate in this environment, the design of a mechanical support is likely required to provide appropriate safe operating conditions for the detectors. A mechanical engineer should investigate a minimal mechanical design for bench testing individual detectors with their full electronics readout.

Reminder: October Review Recommendations

6. Grounding/Disabling of Unused Detector Channels (HIGH)

In the commissioning run, some channels that were not working (due to mechanical issues, connectors, pogo-pins, etc.) or not used were left powered in the detector assembly. To prevent detector bias problems and crosstalk in electronics channels, a test procedure must be developed to identify unconnected channels, and straightforward methods to enable power/ground disabling of these channels must be determined. The silicon detector pixels cannot be left floating when disconnected from the electronics.

7. Reduced Pixel Simulations & Transition PCB Redesign (HIGH)

The full detector testing, where all the pixels were connected to the front-end electronics resulted in consistent oscillating behavior of many channels that prevented the use of the detector for measurements. Periodic stability was achieved by removal of multiple channels. One method to help in obtaining stable detector system operation was suggested during Leah Broussard's presentation. This approach involves removing the perimeter pixel channels and remapping the electronics channel connectivity within the remaining pixels to obtain stable overall detector system operation. It is crucial that the Nab collaboration validates this approach via simulation to verify that the removal of perimeter pixels can be performed without any reduction in the physics performance of the Nab experiment. If a decision is done to remove the perimeter pixels, a straight-forward redesign of the transition PCB will become necessary. If valid, this method provides an excellent fallback position if the present configuration (using all 128 pixels of the upper and lower sections) cannot achieve stable operation, after investigating all of testing and electronics modifications suggestions provided in this document.

Reminder: October Review Recommendations

11. System Assembly and Disassembly Optimization (HIGH)

Assembly and disassembly of the Si-detector hardware and electronics at the Instrument Hall of the SNS is a difficult task having many opportunities for damaging the detectors, electronics, connectors, cables, and mechanical structures. To facilitate more efficient and safe system installation and removal, a thorough review of the detector hardware, including detector mounts, is crucial to ensure system cleanliness, connectivity, handling, and storage. In addition, a thorough review of the installation and removal procedures of the system must be performed. Mechanical designs of the detector stand must be re-evaluated and may require redesign. Cabling and especially connectors have been observed to be significant points of failure. Analysis is needed to assess present methods and identify where new methods would improve these operations. One suggested improvement involves significantly shortening the BNC cables from the detector electronics to the ADC. A solution could involve use of a patch panel that would significantly ease the installation of the detector systems. The use of new mechanical material handling aids should be considered as they may greatly improve the safety of these operations, (safety of the staff and the experiment hardware) and will decrease the cost and time associated with future installation and removal operations.

12. Project Management (HIGH)

Multiple tasks have been outlined in this document that must be completed in time for the next SNS run cycle that will start in July 2024 – ranging from straight-forward and short in duration to more complex and time consuming. These tasks are additions to the already existing Nab task list for the next run cycle. Proper and timely execution of the tasks also involves multi-disciplinary teams of physicists, scientists, and mechanical and electrical engineers. Effective execution of all or part of these tasks within the short timeframe afforded will require efficient manpower and scheduling of multiple tasks. For these reasons, the assignment of a project manager, who will be specifically assigned to directing this work, is crucial for Nab experiment success.