Alphacore's CMOS IP Update

Streaming Readout Workshop, December 2021

Date: 12/09/2021

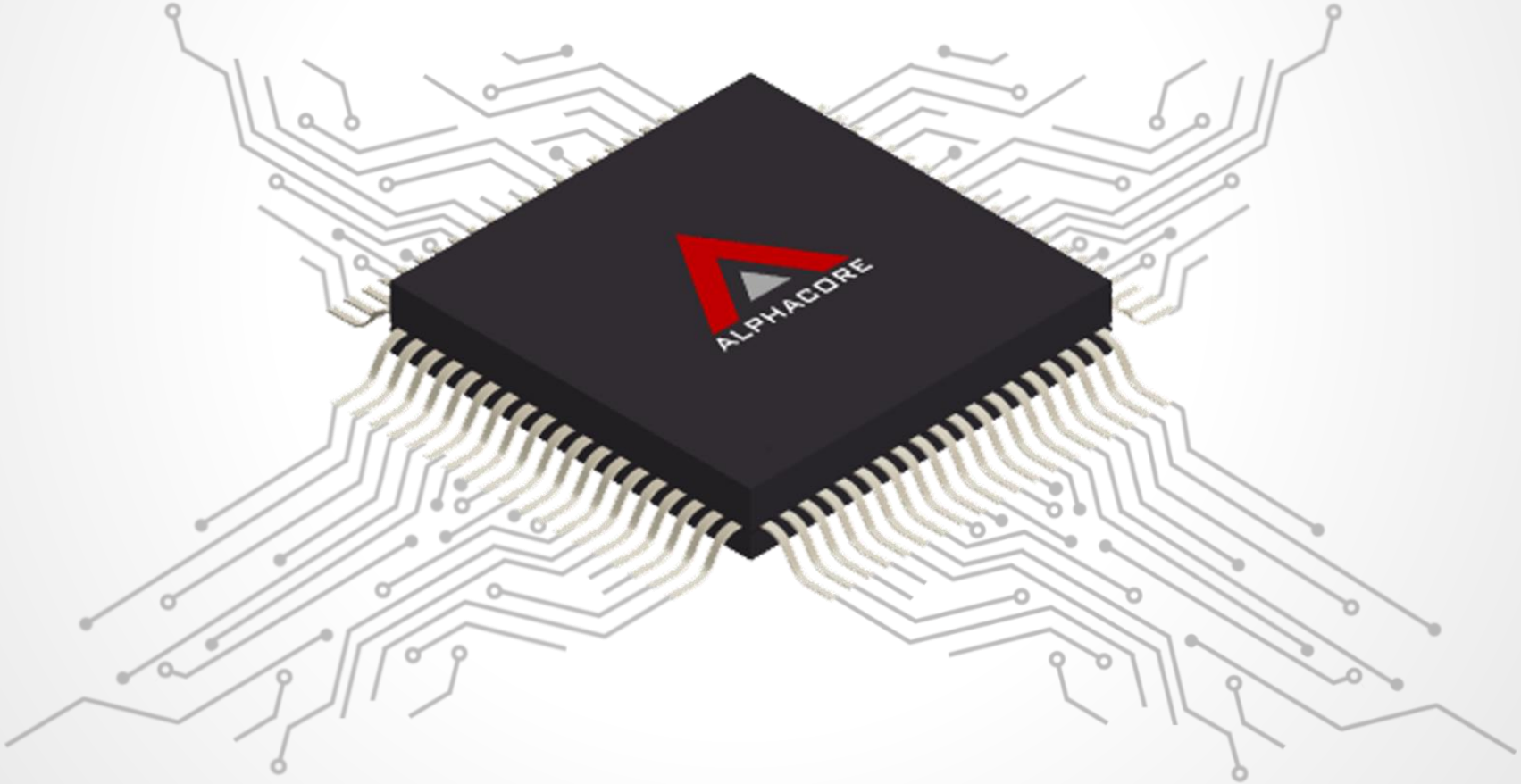
Outline

- Alphacore's 90nm - 180nm CMOS preamplifiers and ADCs status.
- Alphacore's 22nm – 28nm CMOS ADCs status.
- New developments in 2021
- Future plans

Alphacore's Goals

- Alphacore has been the performer in a DOE STTR Ph2 program entitled: "Multi-Channel Readout IC for Nuclear Physics Experiments and in a DOE SBIR Ph2 program entitled: "Picosecond Digitizer".
- Status: The funded technical periods ended in May and August, 2020, respectively. Alphacore is seeking further funding opportunities.
- Key goal of this work has been to develop versatile detector readout solutions, both IP and ICs.
- The IP blocks can be used to relatively quickly build the exact, compact readout ASICs configurations most suitable for a target application when the need arises. Alphacore can build the exact ASIC for a customer in need using the tested IP.

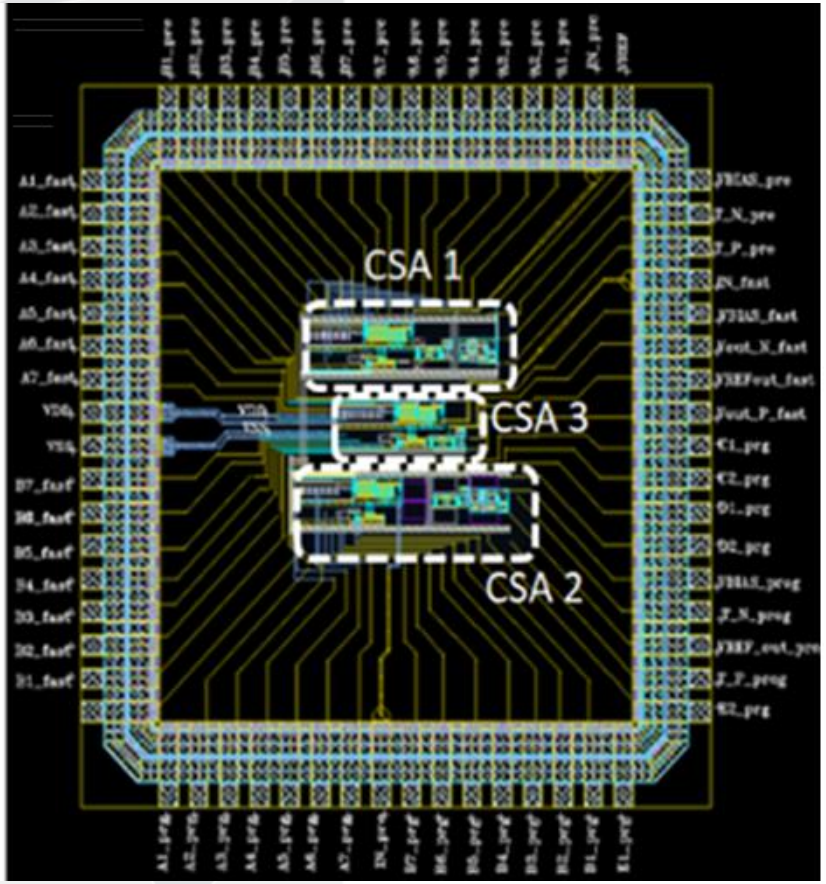
90nm – 180nm CMOS ANALOG AND MIXED-SIGNAL SOLUTIONS



Summary of Recent Readout Ckt Designs

	90nm - 180nm CMOS readout ckts	22nm – 28nm CMOS readout circuits
Main funding source	DOE NP STTR Ph2 (until May 2020)	DOE HEP SBIR Ph2 (until August 2020)
Evaluated Design #1	180nm programmable preamplifier	28nm, 10b, 300MSPS, 0.8mW ADC
Evaluated Design #2	180nm 10b, 50MSPS, 7mW ADC (1-ch, 6-ch)	28nm 10b, 500MSPS, 1.2mW ADC
Evaluated Design #3	180nm 12b, 100MSPS, 60mW ADC (1-ch, 6-ch)	28nm, 9b, 1GSPS, 2mW ADC
Evaluated Design #4	180nm serializer interface with PLL	28nm, 10b, 2.4GSPS, 6mW ADC
Evaluated Design #5	90nm 14b, 50MSPS, 35mW ADC	22nm, 10b, 5GSPS, 19mW ADC (recently taped out)
Deliverables now	Preamplifier and ADC single channel test boards, multichannel bare die	Test boards for all ADCs (the output interface is not suitable for actual detector readout experiments)
Deliverables with small amount of additional funding	Packaged multi-channel 180nm test chips with PLL-driven Serializer and 1Gb/s LVDS Interface	ADC chips and test boards with FIFO output interfaces suitable for detector readout experiments
Deliverables of potential follow-on program	Multi-channel 90nm chips, FPGA based evaluation boards, improved specifications, more channels per chip	Multichannel chips, FPGA based evaluation boards, improved specifications

Charge Sensitive Amplifiers (CSA) Tapeout



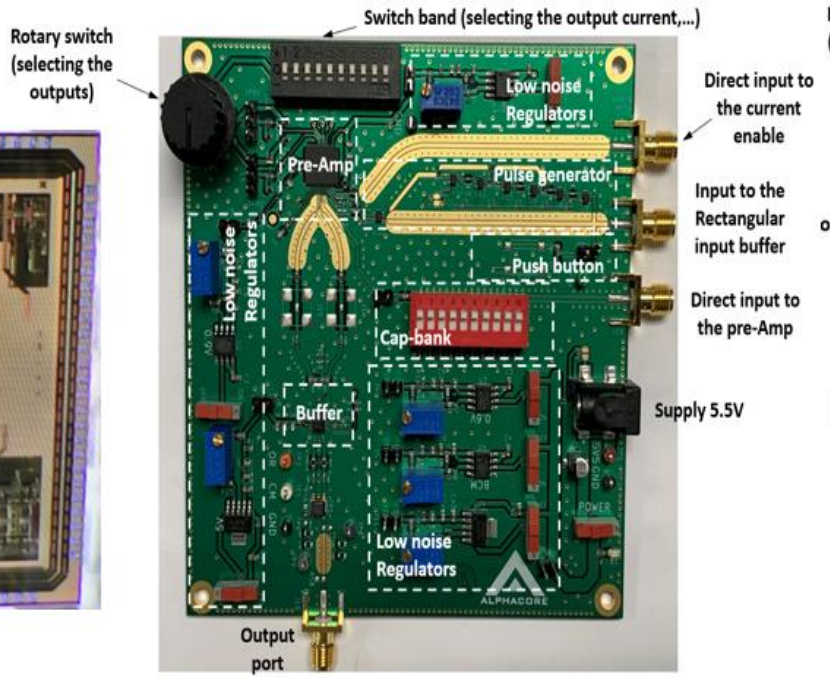
Test chip for 3 CSAs

# Simulated specifications	CSA1 with programmability	CSA2	CSA3
Equivalent Noise Charge(ENC) worst case (electrons)	556	1.8K	480
ENC increase rate (electrons/pF)	22.25	negligible	22.25
Rise Time typical (ns)	92	208	20
Gain (mV/fC)	30.45	29.8	2.3
Rise time programmability (ns)	50n-200	NA	NA
Gain Programmability (mV/fC)	15-60	NA	NA
Fully Differential Output	Yes	Yes	Yes
Common Mode of Full Differential Output	0.8-1	0.8-1	0.8-1
Shaper Circuit	Yes	Yes	No

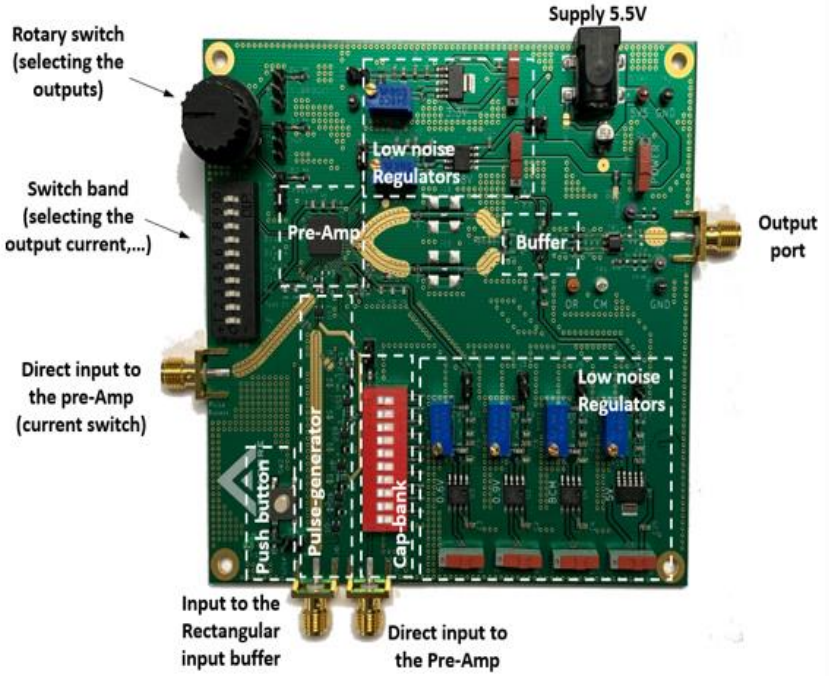
CSA Micrograph and Evaluation Boards

CSA evaluation boards and/or packaged chips are available for customers. 16-ch preamplifiers are available as bare die.

Die micrograph

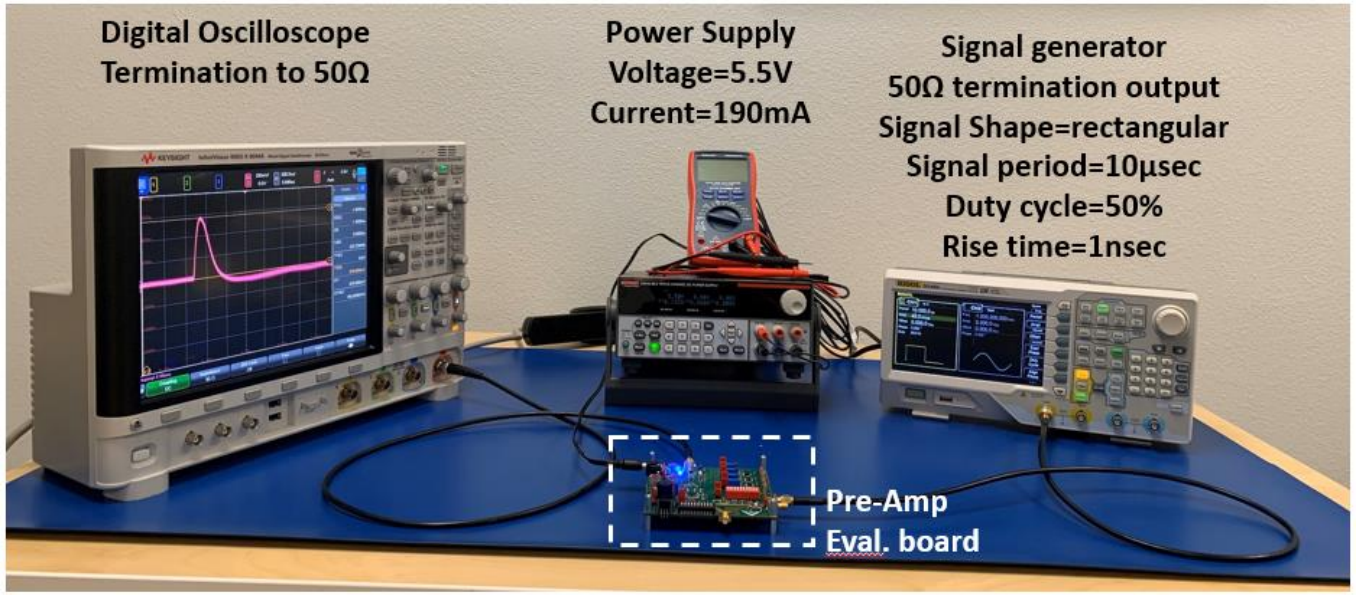


CSA evaluation board 1

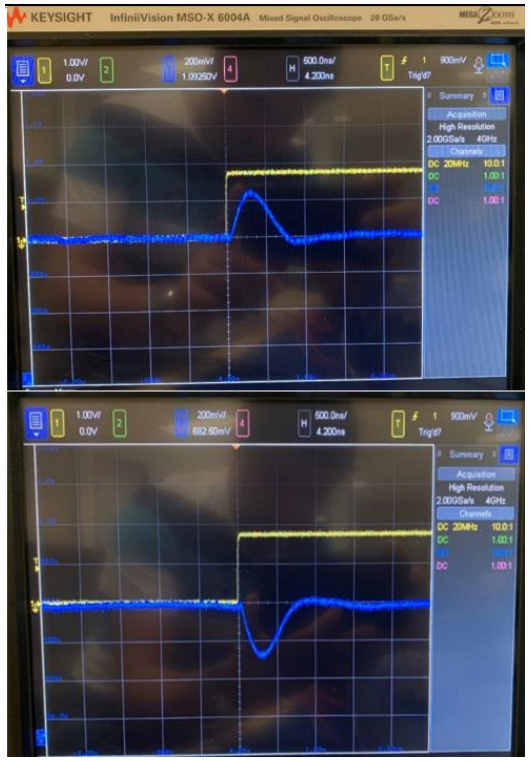


CSA evaluation board 2

CSA measurement setup



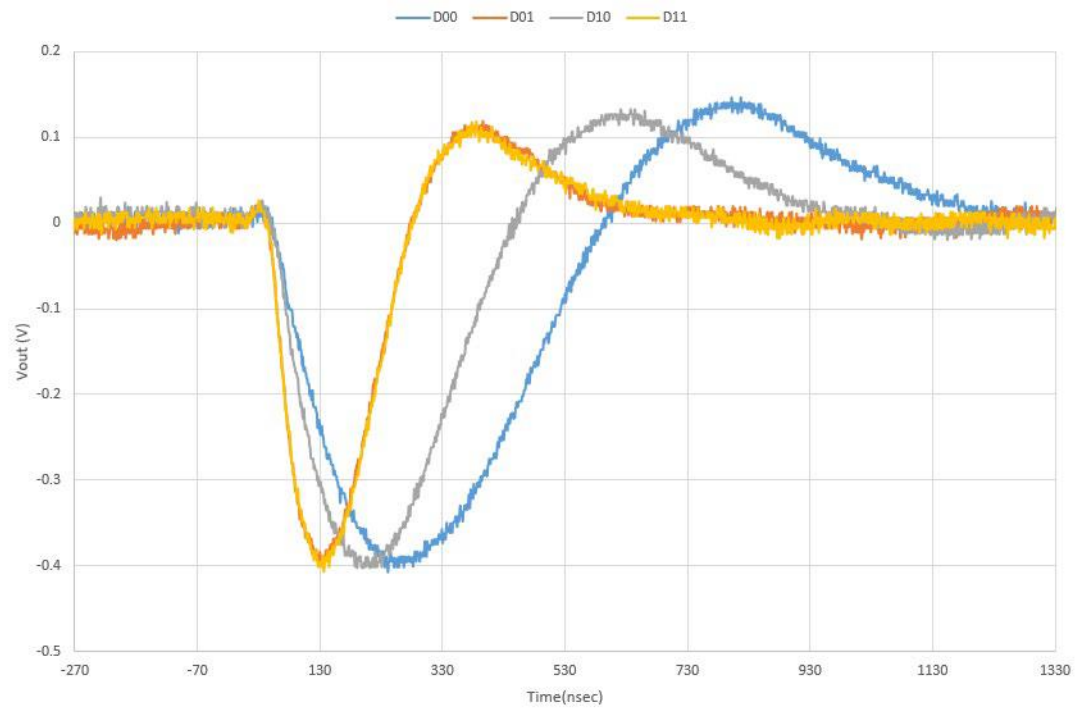
CSA measurement test setup



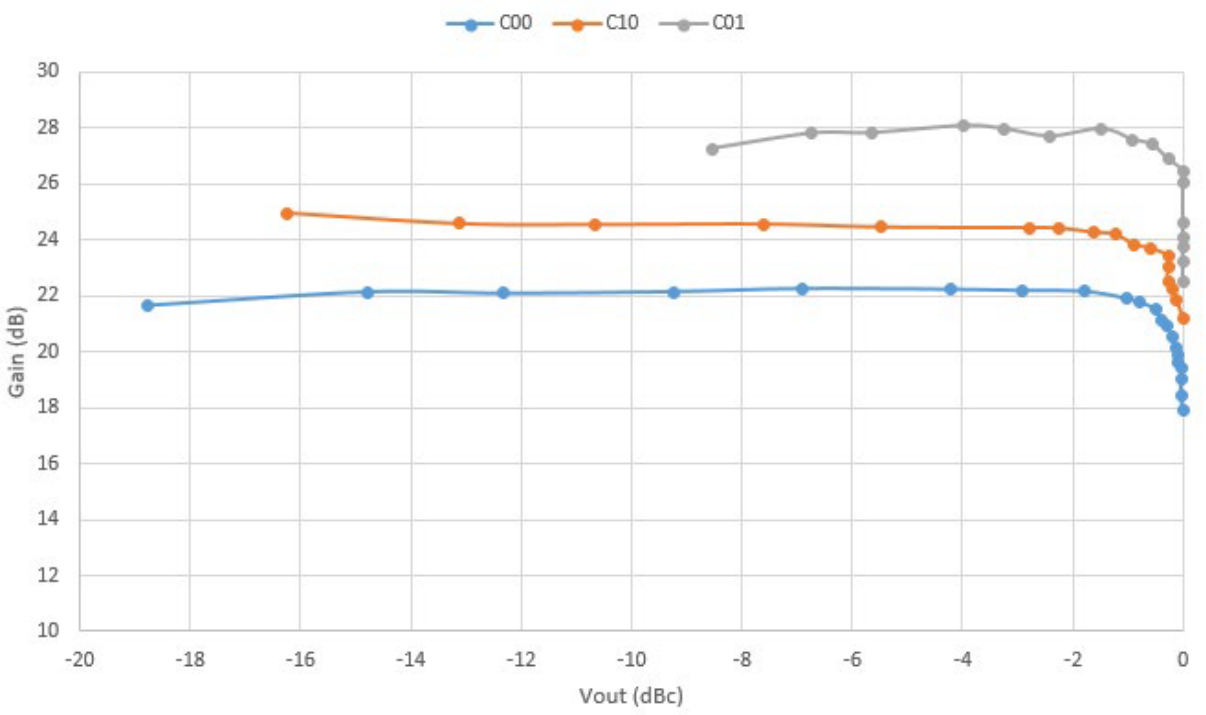
Measured pulse waveforms on an oscilloscope

Noise measurement with logic analyzer

CSA1 Test Results



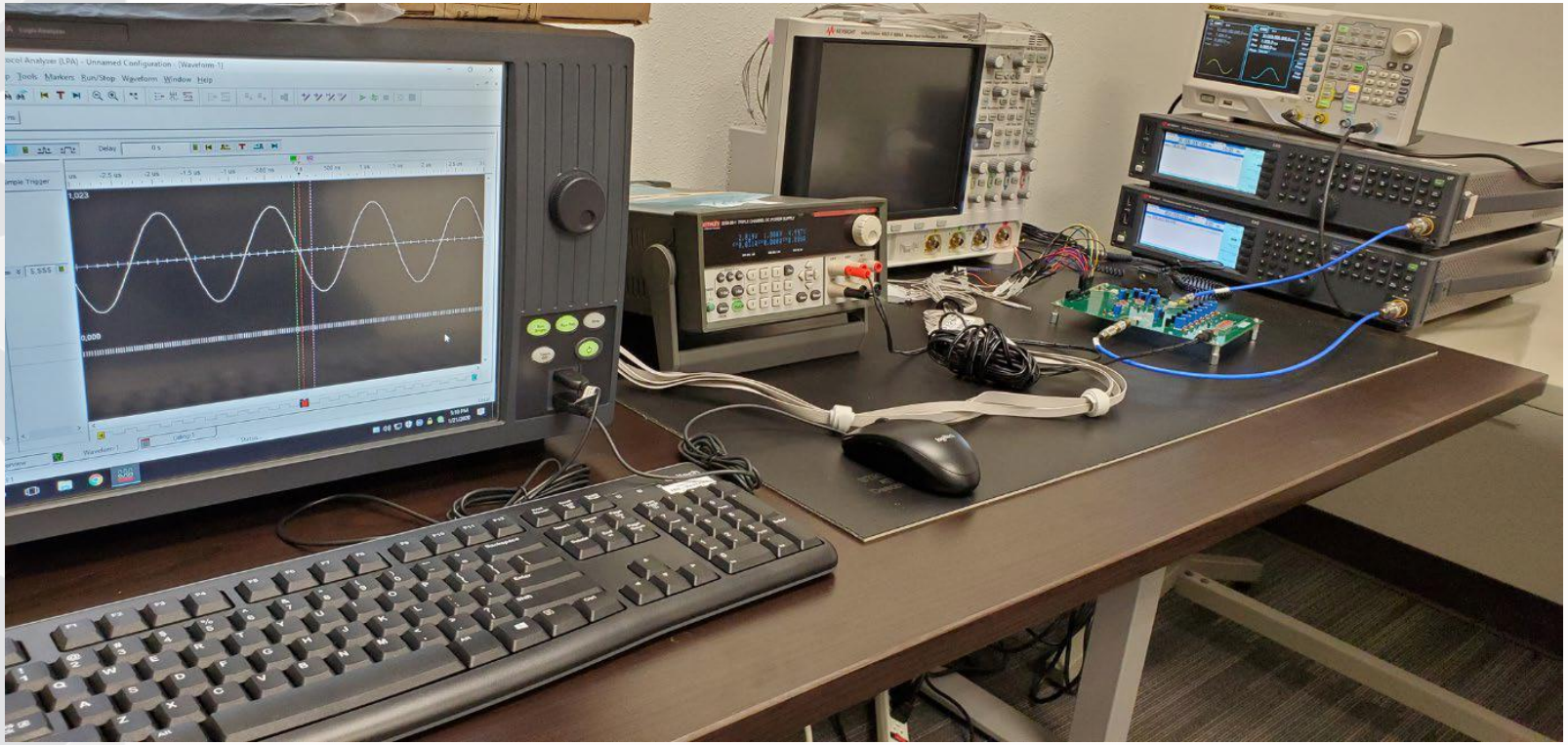
Shaping time programmability measurements



Gain programmability measurements

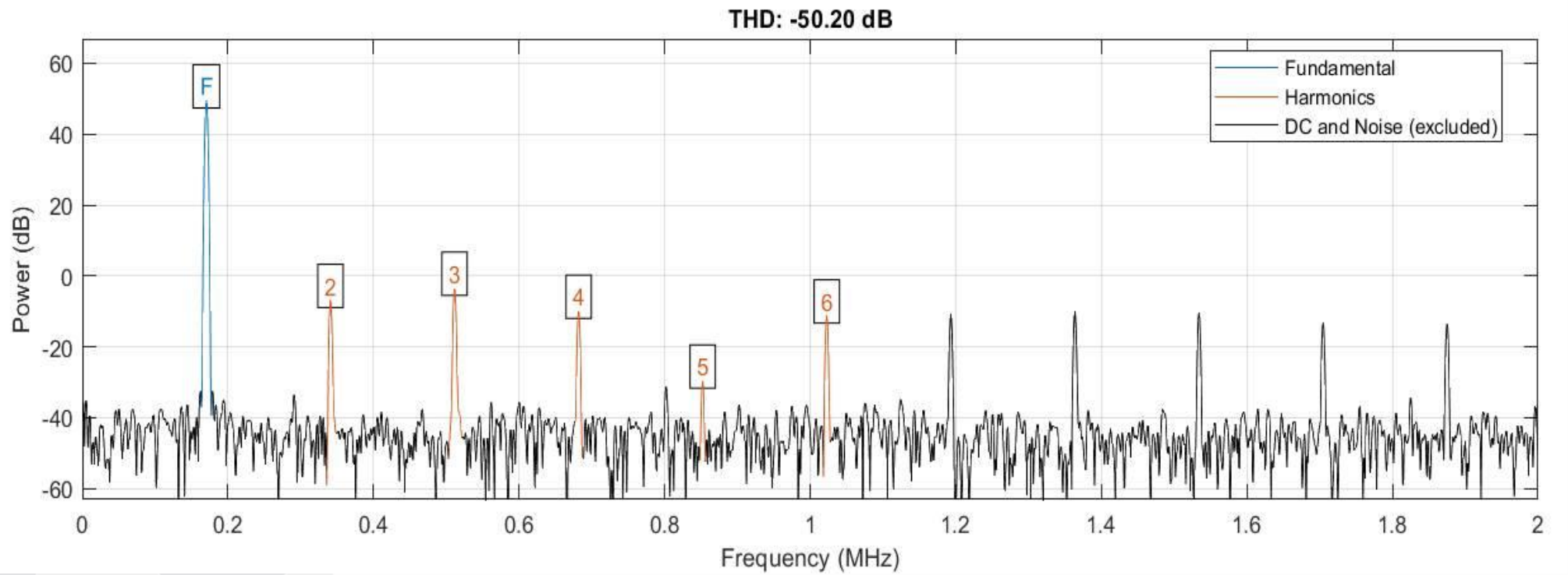
Noise was measured as 712 electrons at room temperature.

90nm – 180nm CMOS Analog to Digital Converters Test Results



ADC Test Setup

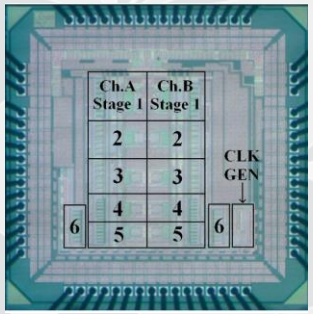
180nm, 10-bit, 50MS/s, 7mW ADC Test Results



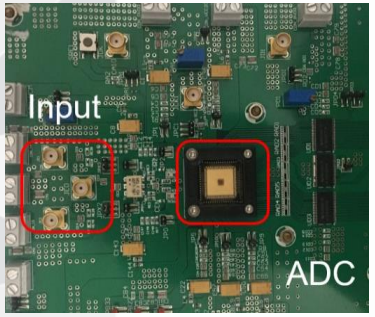
SINAD = 44.04 dB
SNR = 45.24 dB
SFDR = 52.83 dB
THD = -50.20 dB
ENOB = 7.31 Bits

ADC test boards and/or packaged chips are available for customers. 6-ch ADCs are available as bare die.

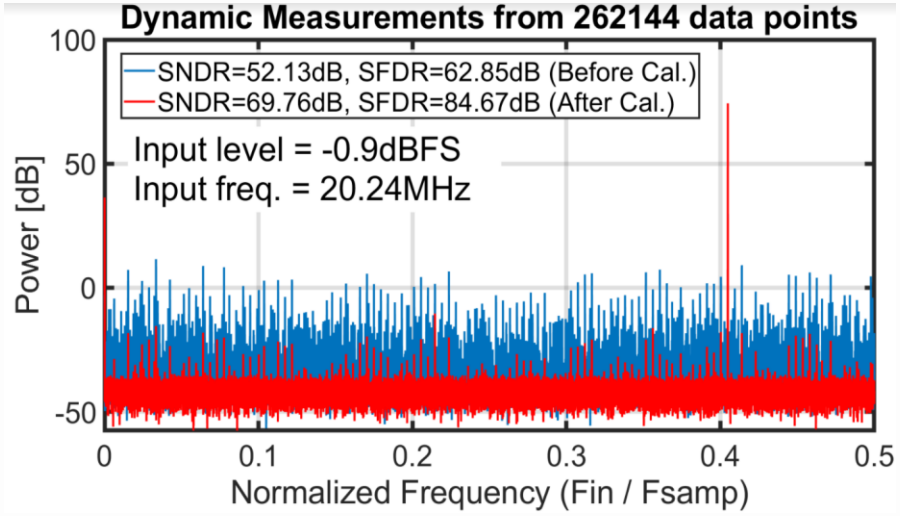
90nm CMOS, 14-bit, 50MS/s, 35mW ADC



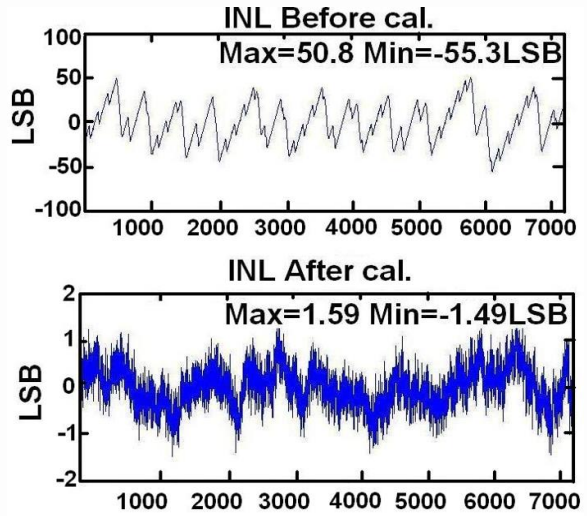
ADC micrograph



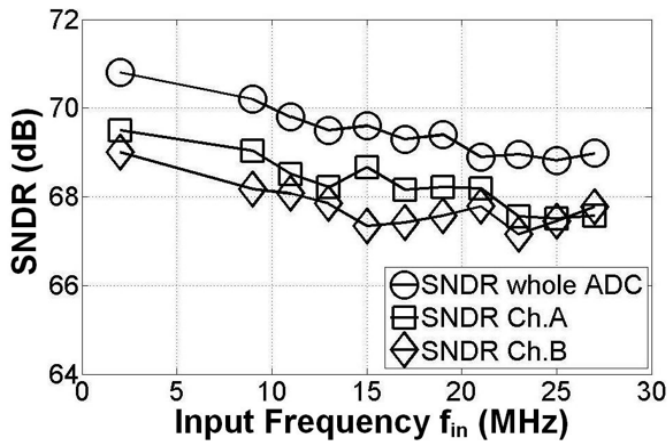
Packaged die and test board



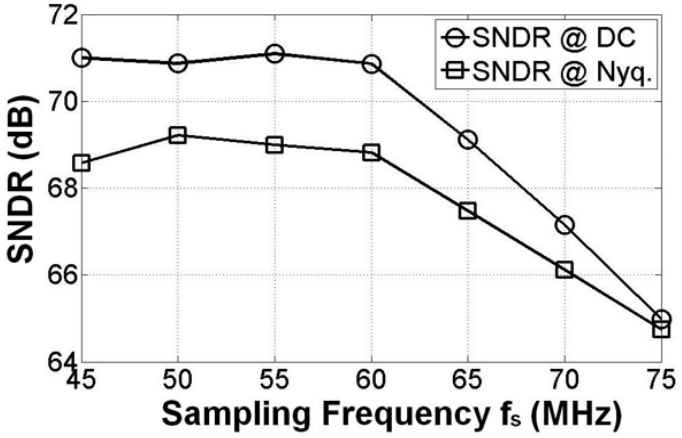
Test results, FFT



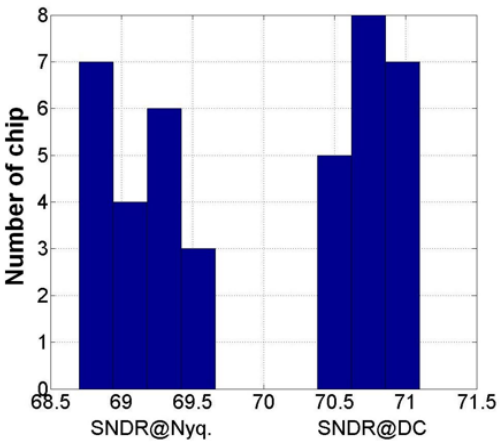
Test results, INL



SNDR vs. Input f

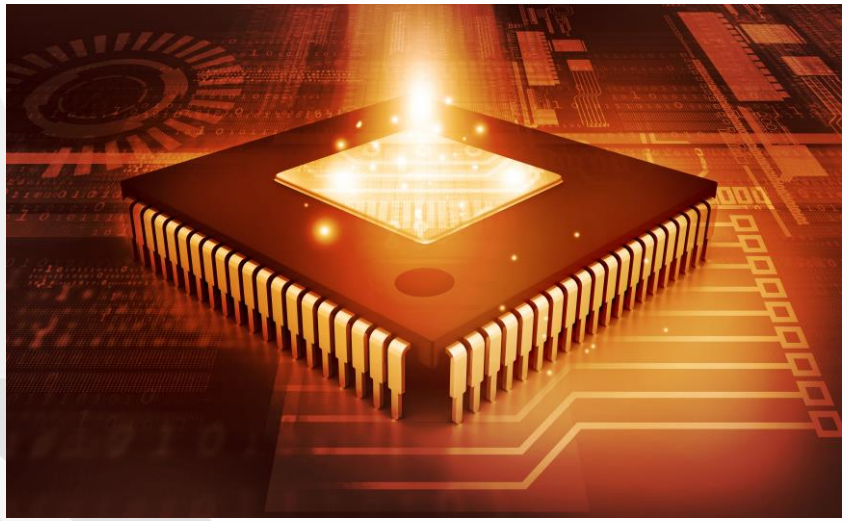


SNDR vs. Sampling f



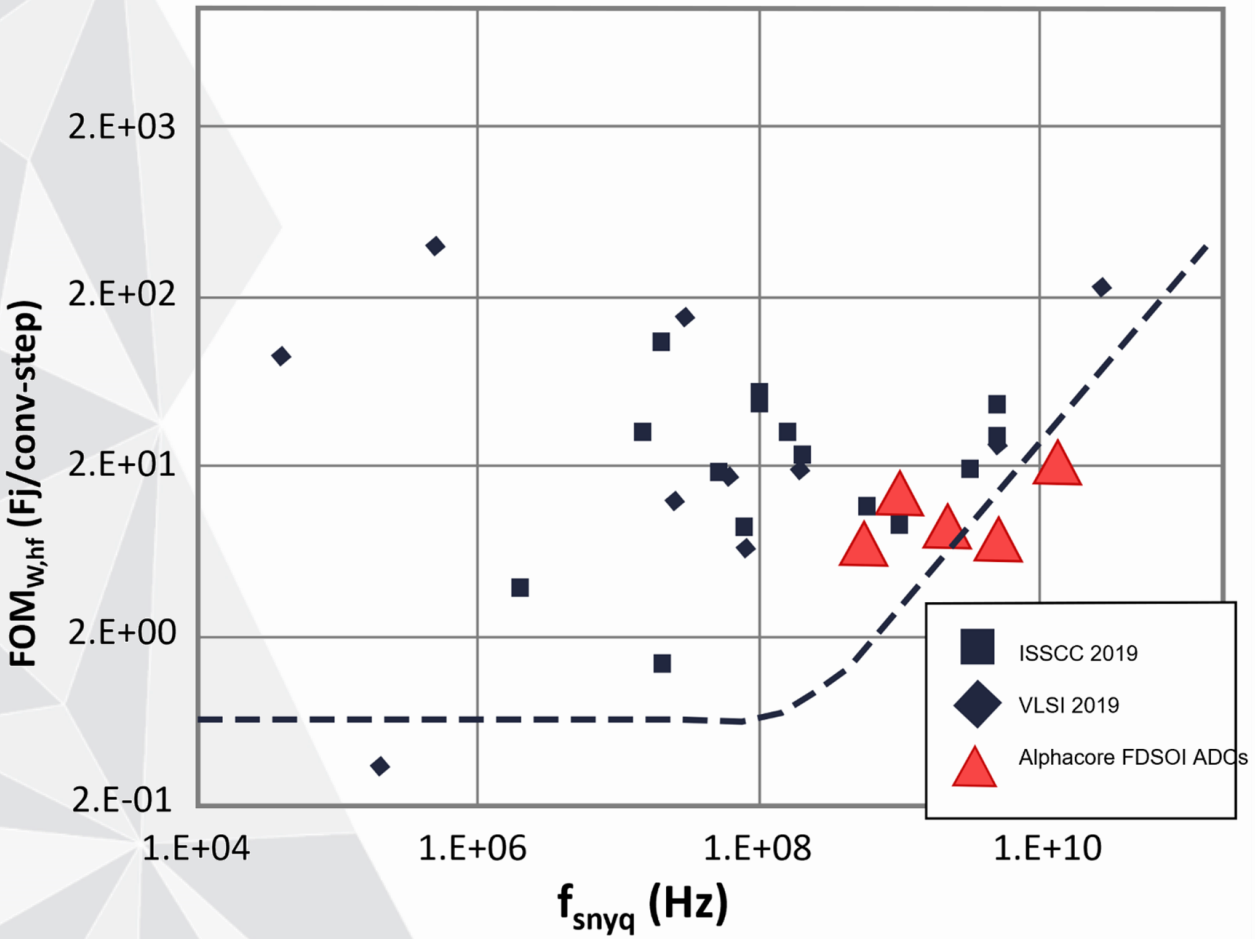
Die Yield

22nm – 28nm Digital CMOS ADCs



- ST-Micro 28nm
- GF 22nm
- Portable to other CMOS processes
- High Bandwidth
- Low Power
- Small Area
- Suitable for Multi-Channel Readouts (up to 64 channels)

Best-in-Class Data Converter IP



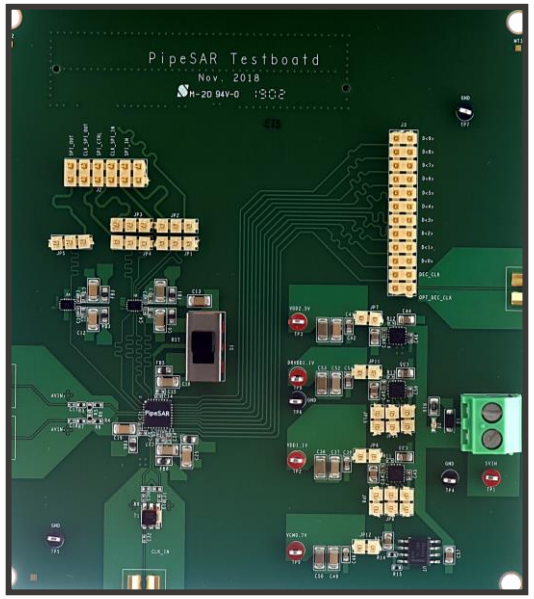
World-class performance levels

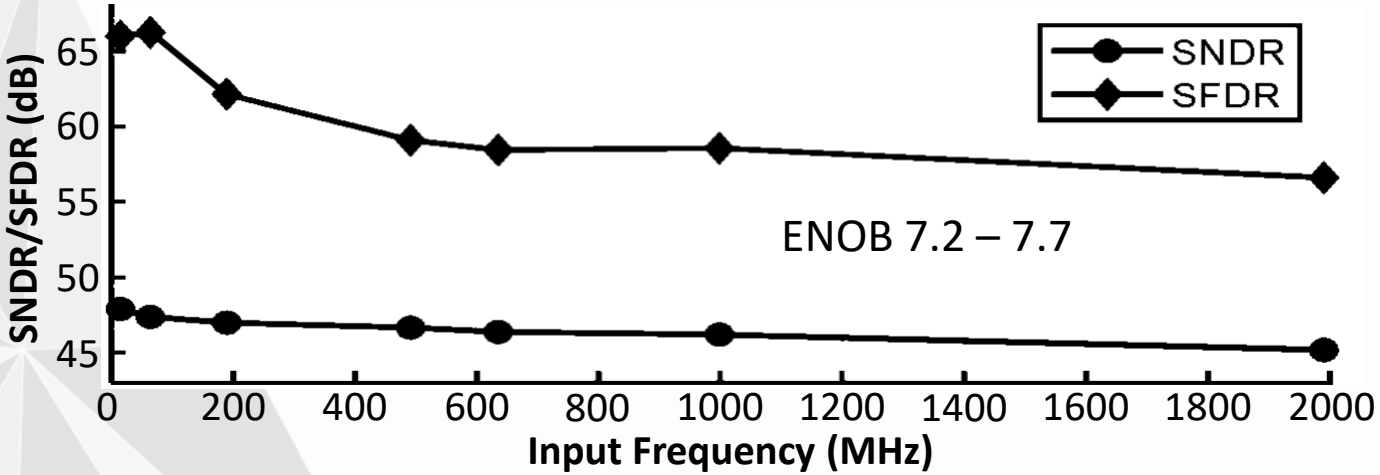
- GS/s conversion rates
- 10X lower power
- Wide bandwidth
- Automatic calibration

Enables

- Faster time-to-market
- Lowest System Power
- Sample rate flexibility

A9B1G STM 28nm

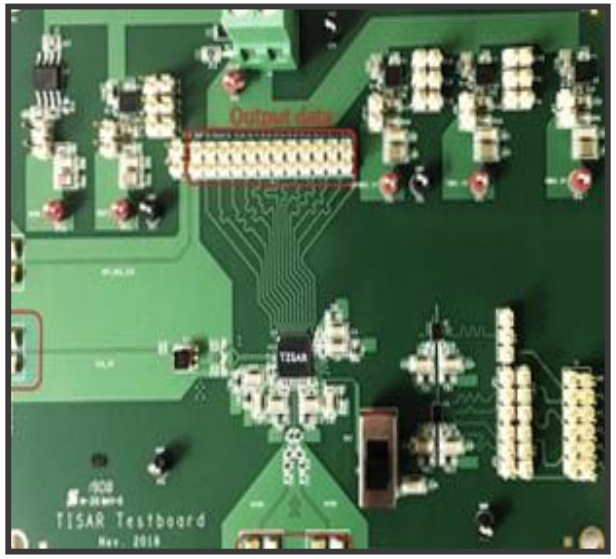


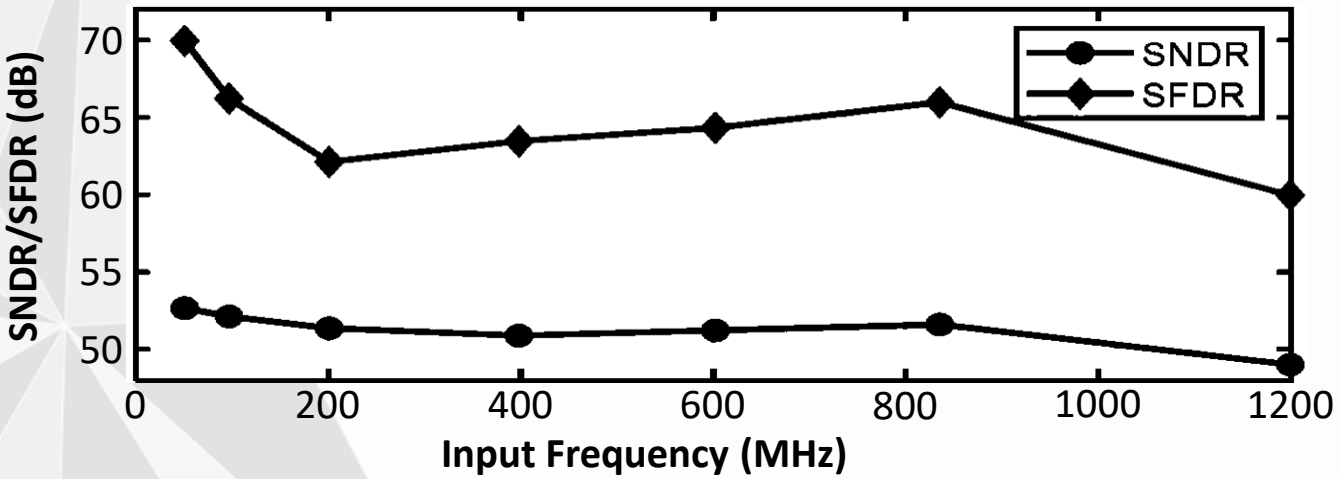


Silicon evaluation results

- 9-bit, 1GS/s
- 2mW
- Wide input bandwidth (beyond 4th Nyquist zone)
- ENOB = 7.2-7.7
  - 1st-4th Nyquist bands

A10B2G STM 28nm

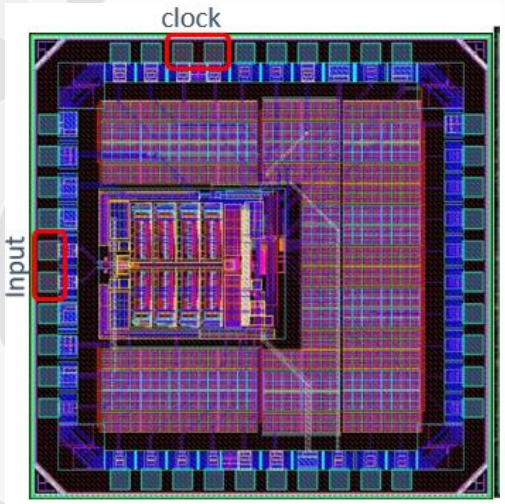


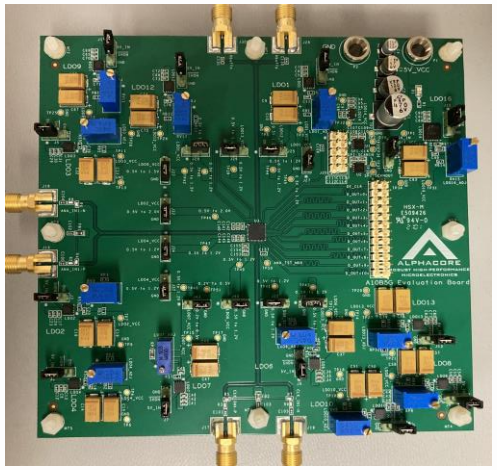


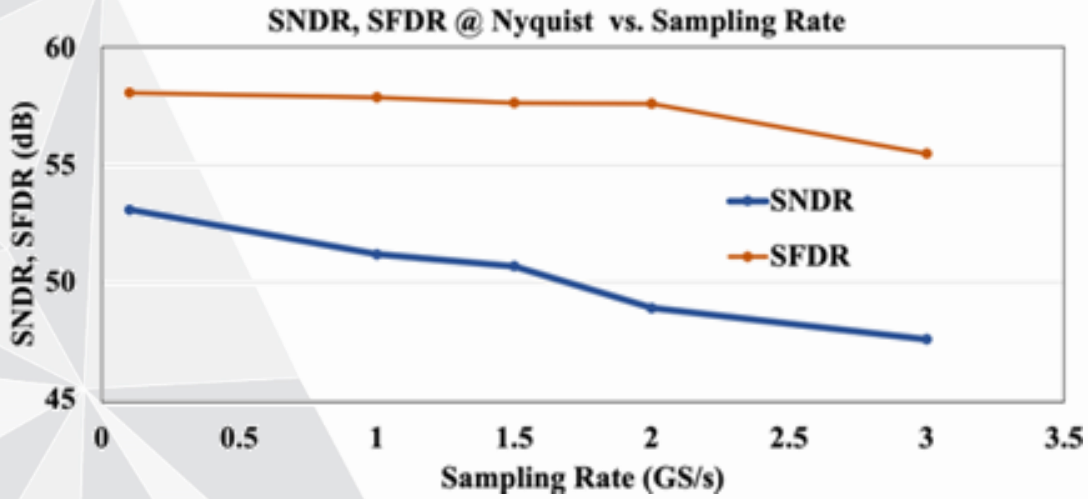
Silicon evaluation results

- 10 bit, 2.4GS/s
- 6 mW
- 8-way interleaved architecture
- Auto-calibration algorithm for interleaving spurs
- ENOB
  - 7.9 to 8.5 in the first Nyquist band

A10B3G GF 22FDX



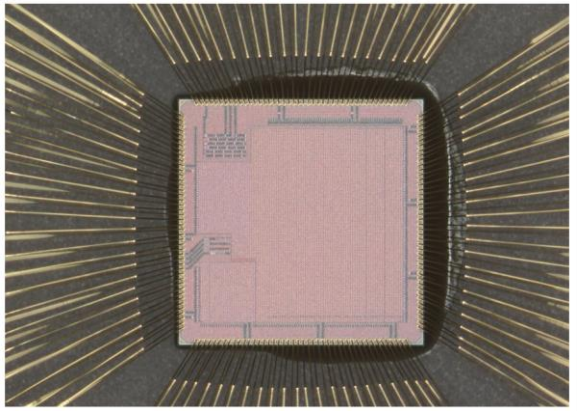




- 10-bit, 3GS/s
- 13mW
- 8.6 ENOB
  - 8.6 @100MS/s
  - 8.2 @1.5GS/s
  - 7.6 @3GS/s

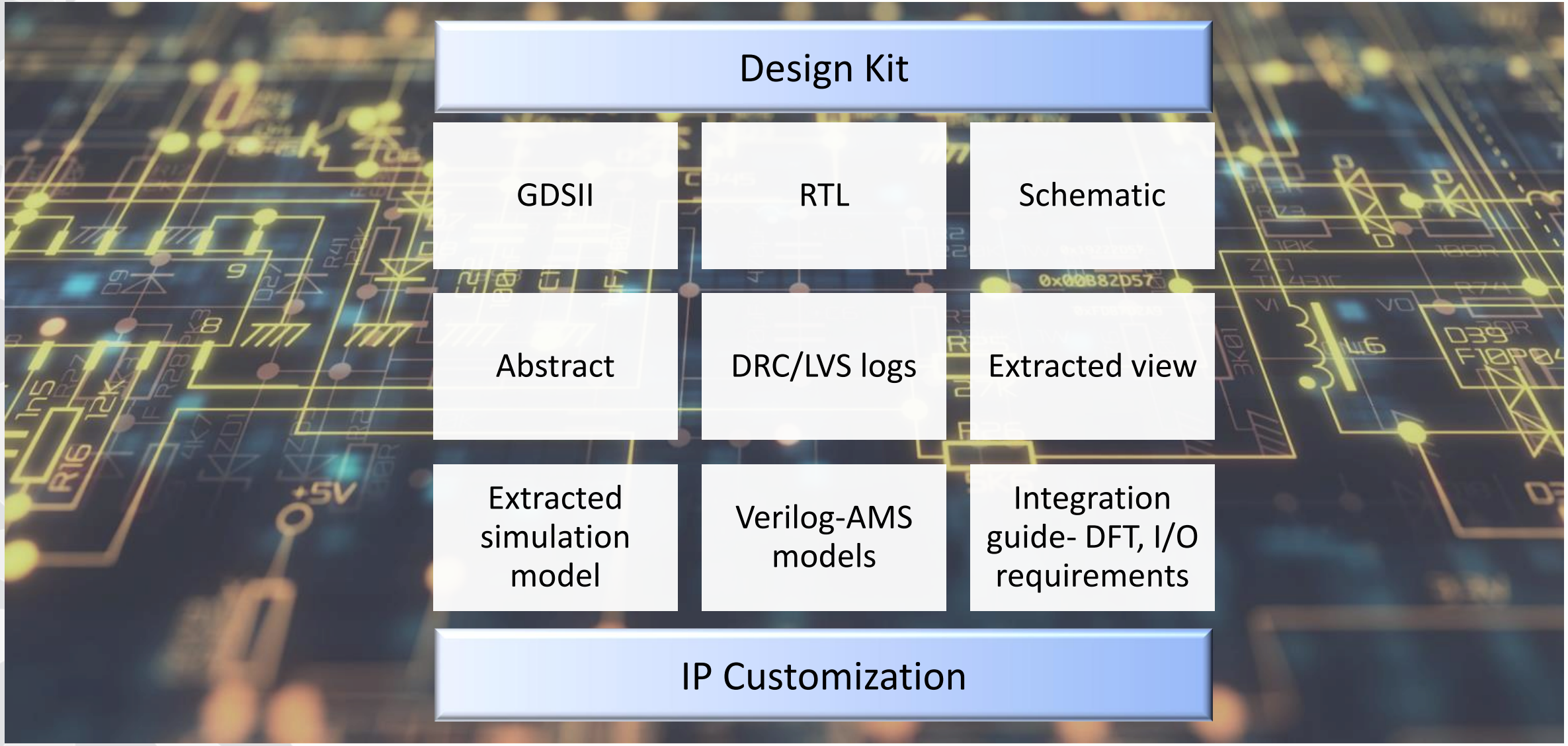
22nm – 28nm ADC Summary

- Alphacore's 22nm – 90nm CMOS ADCs IP Cores can be used to build 16 – 64-channel Readout Digitizer ASICs that have both "full data rate" and SRAM based digital buffer (e.g. 2,048 samples) output interfaces.
- Resolution 10-12 bits,
- Sample Rate 100MSPS – 5GSPS
- Bandwidth up to 10GHz
- Power as low as 1mW per channel for GSPS Digitizer



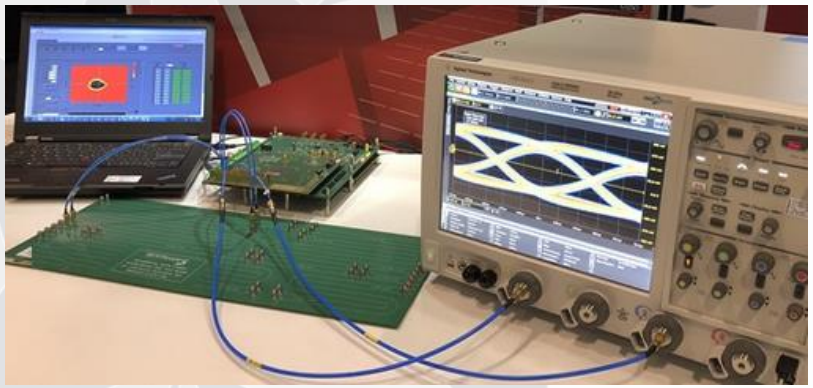
SRAM Test Chip

Design Kit Support



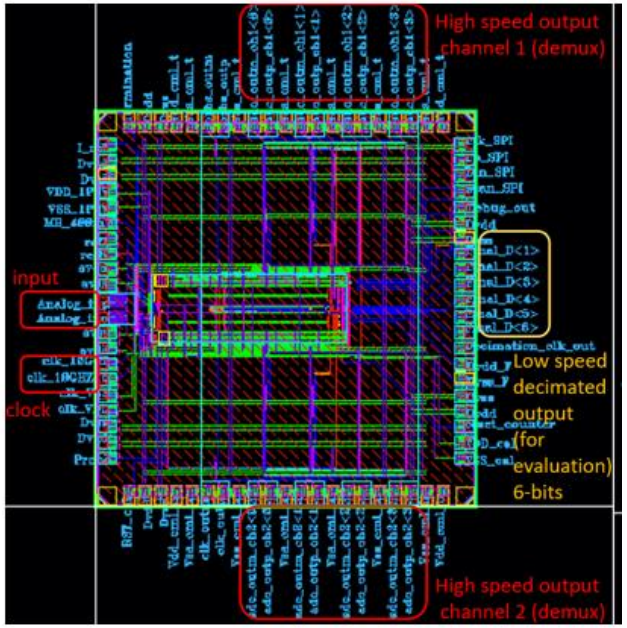
New in 2021: SerDes and High-BW Data Interfaces

Industrial Quality SerDes in TSMC 28nm



Eye diagram testing for 16Gbps (per lane) SerDes IP in 28nm CMOS (TSMC)

- Wide operating range – data rates from 1Gb/s to 16Gb/s
- Configurable pre-emphasis and post-emphasis control
- Programmable Continuous Time Linear Equalizer to compensate for high frequency losses
- Compatible with PCIe, JESD204, SATA, SRIO, and SG-MII

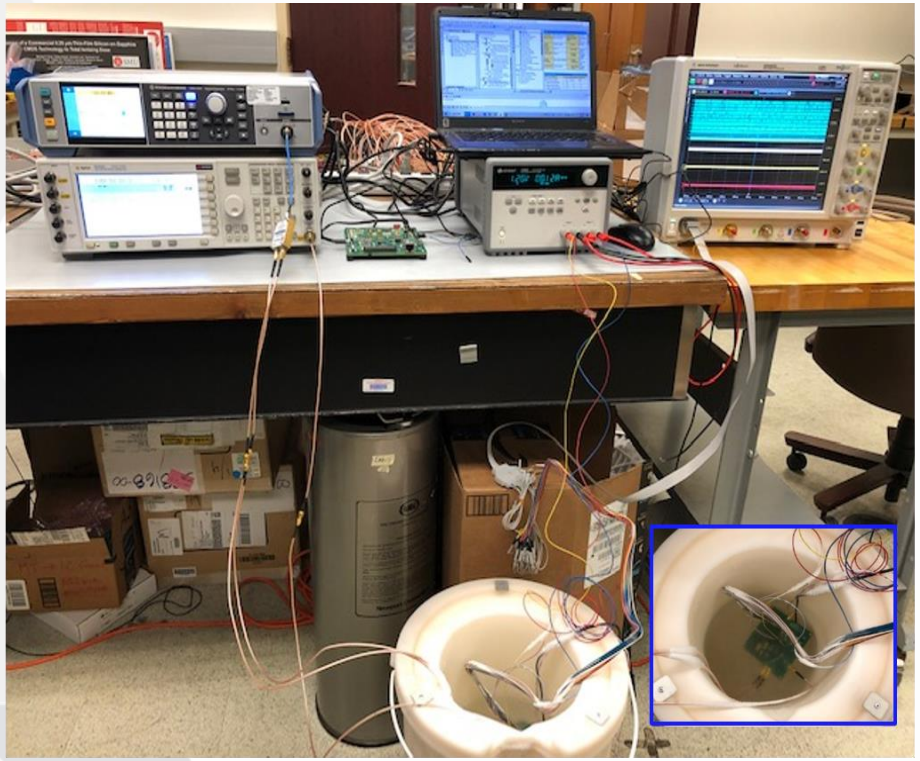


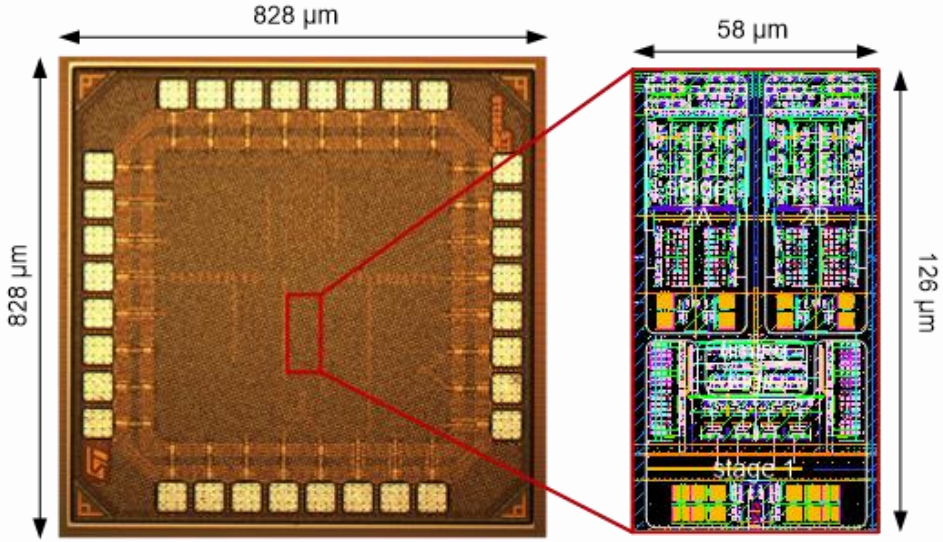
Layout of 22FDX 160Gbps (total), <1pJ/bit ADC I/O interface that supports >50mm trace length

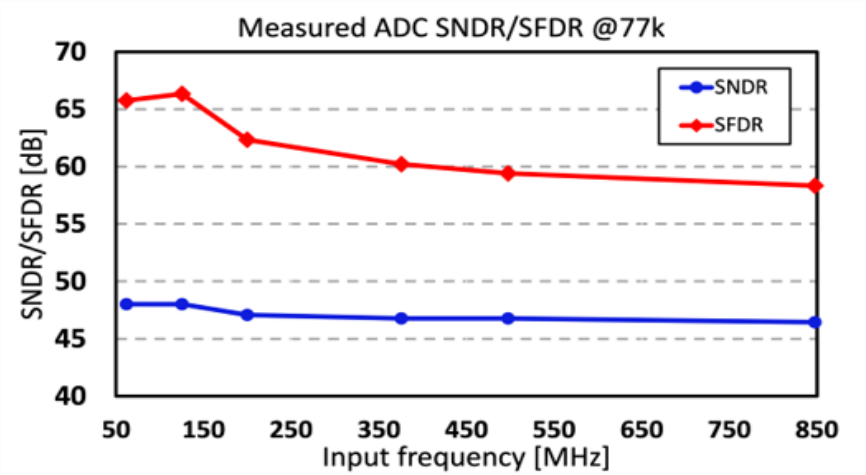
- Low-power high data bandwidth die-to-die/die-to-FPGA I/O interface IP
- Verified in GF 22FDX process
- Suitable for both organic and Si interposer chiplet interfaces

New in 2021: Cryogenic High-BW, Low-Power ADC

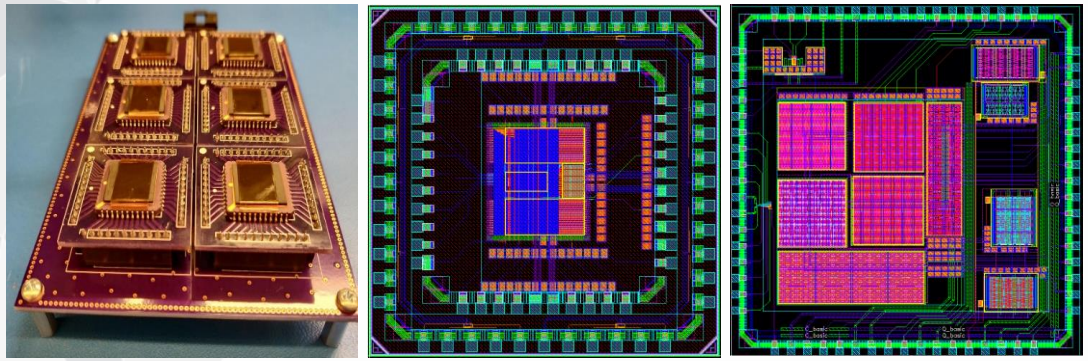
10-bit, 1GS/s ADC operated at 77K



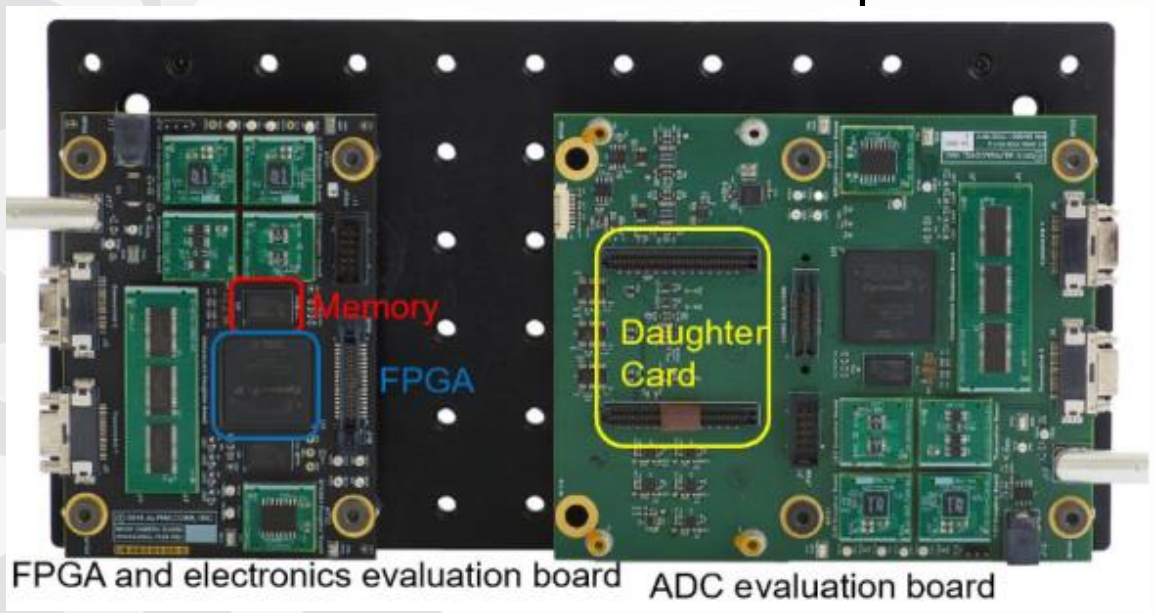




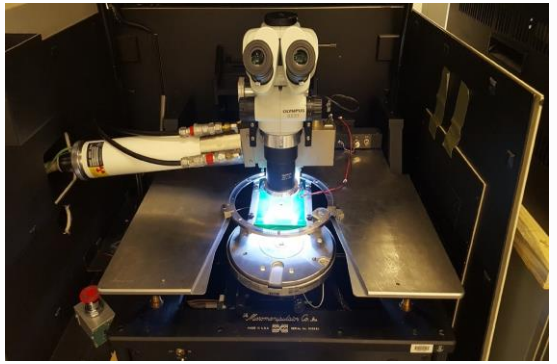
New in 2021: Radiation Test Capability

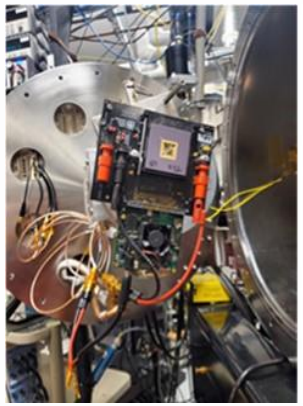


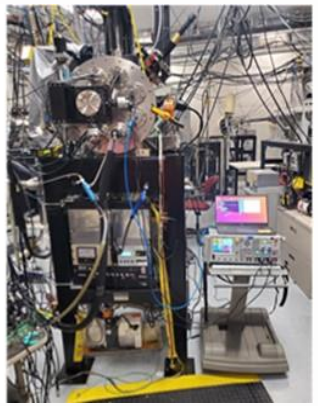
22nm CMOS Test Chips



Eval Board







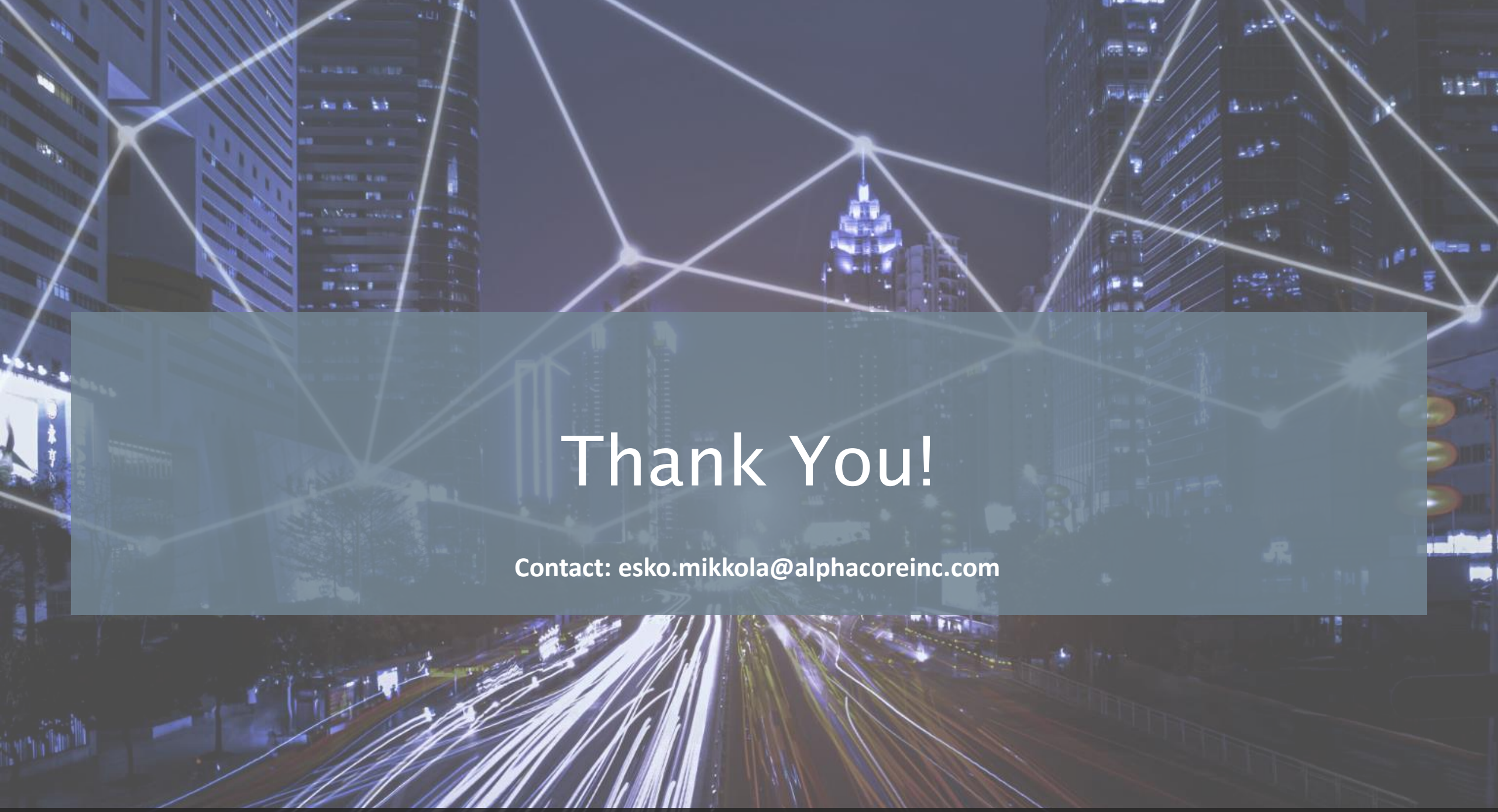
TID (gamma, X-ray), Heavy Ion, Neutron, Proton Testing

Summary

Alphacore's IP is available for the Streaming Readout Community

- ✓ ***High Bandwidth***
- ✓ ***Low Power***
- ✓ ***Silicon Proven***
- ✓ ***Design Kits Available Now***
- ✓ ***Custom ASIC and RHBD Services***
- ✓ ***Please contact us to talk in detail about your requirements***

Low risk, Best-in-Class Performance and Power



Thank You!

Contact: esko.mikkola@alphacoreinc.com