# Development of FELIX for DAQ System in Nuclear and Particle Physics Experiments

Mathieu Benoit, Filiberto Bonini, Hucheng Chen, Dimitrios Matakias, Shaochun Tang,
Hao Xu, Elena Zhivun

Streaming Readout IX Workshop, Dec 10, 2021

# Outline

- Introduction to FELIX
- FELIX for ATLAS TDAQ Phase-2 Upgrade
- FELIX-based DAQ system for NPP experiments

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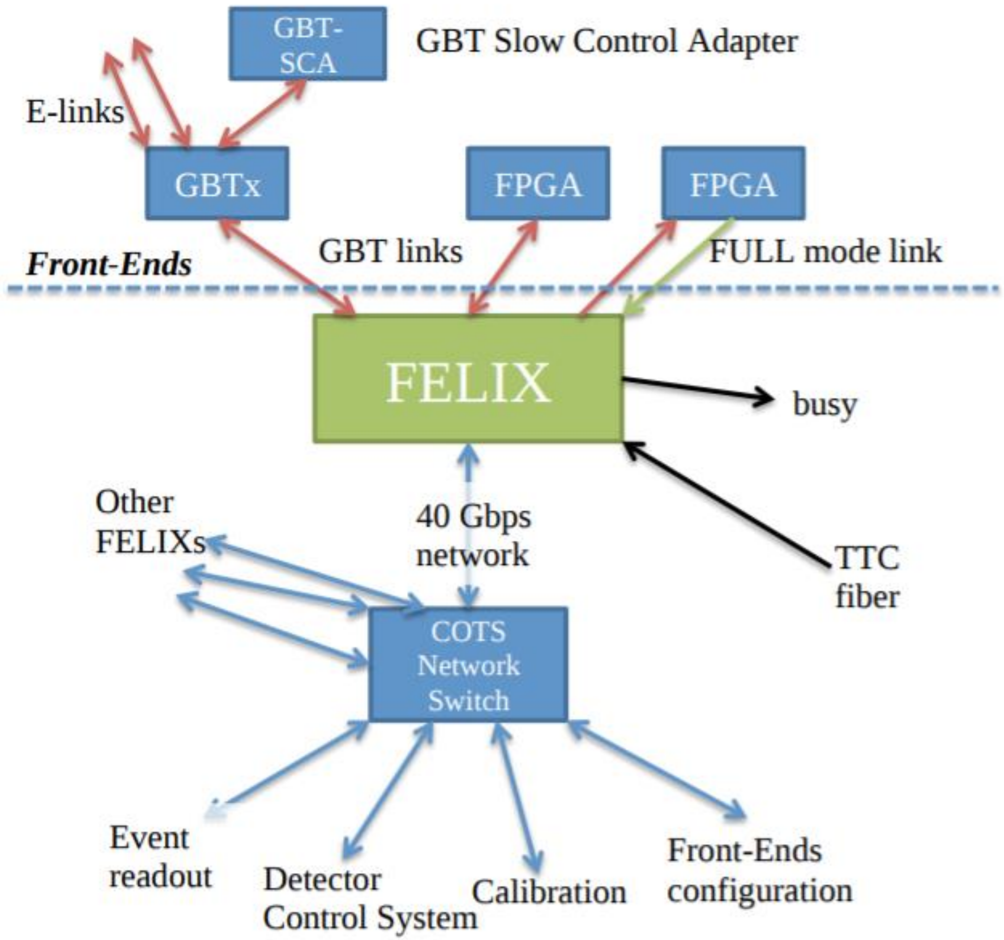
# FELIX - FrontEnd LInk eXchange

FELIX: data/signal/message routing from/to FE

- Router between FE serial links and commercial network
- Data transport decoupled from data processing
- Get and distribute TTC (Timing, Trigger and Control) signals
- GBT-mode configurable e-links
- Detector independent

More information is available on FELIX website:
https://atlas-project-felix.web.cern.ch/atlas-project-felix/




FELIX functionalities

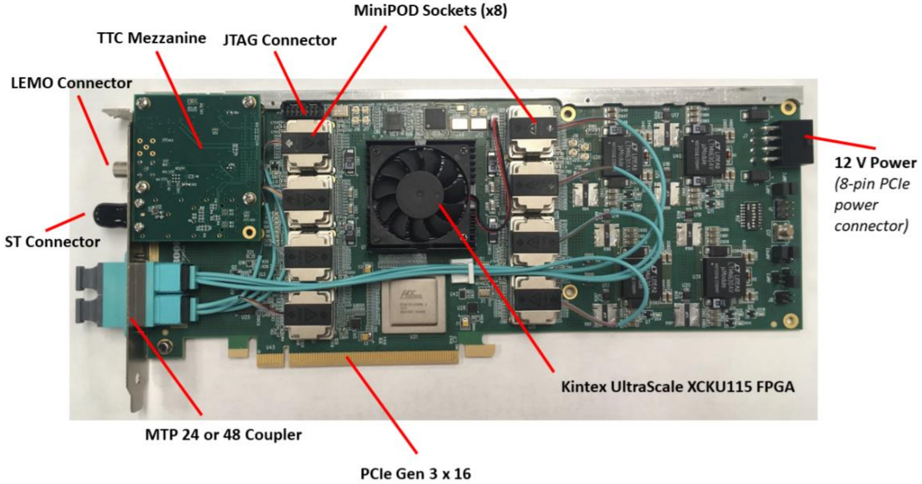
# Hardware FLX-712

FLX-712 hardware

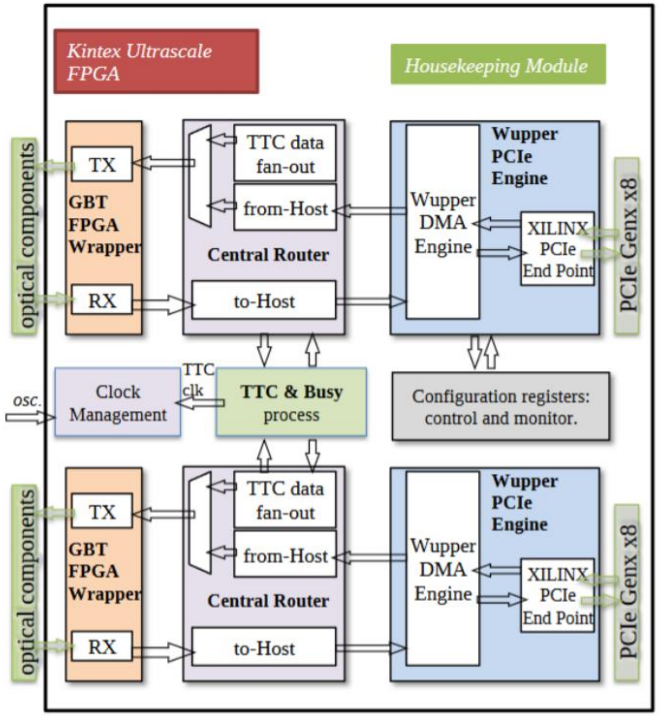
- Xilinx Kintex Ultrascale FPGA
- 24/48 duplex optical fibers for FE
- PCIe Gen3 x 16 lanes

FELIX firmware supports both of GBT mode and Full mode

- GBT mode
  - Firmware to interface FELIX to GBTx ASICs
  - GBTx = radiation hard chip aggregating FE electrical links, coupled to optical transceiver
  - GBT = protocol used by the GBTx
  - One link (4.8 Gb/s) divided into several e-links
  - Up to 48 GBT links per FLX-712
- Full Mode
  - Firmware to interface the FELIX to other FPGA-base systems
  - Up to 24 channels per FLX-712, 9.6 Gb/s each



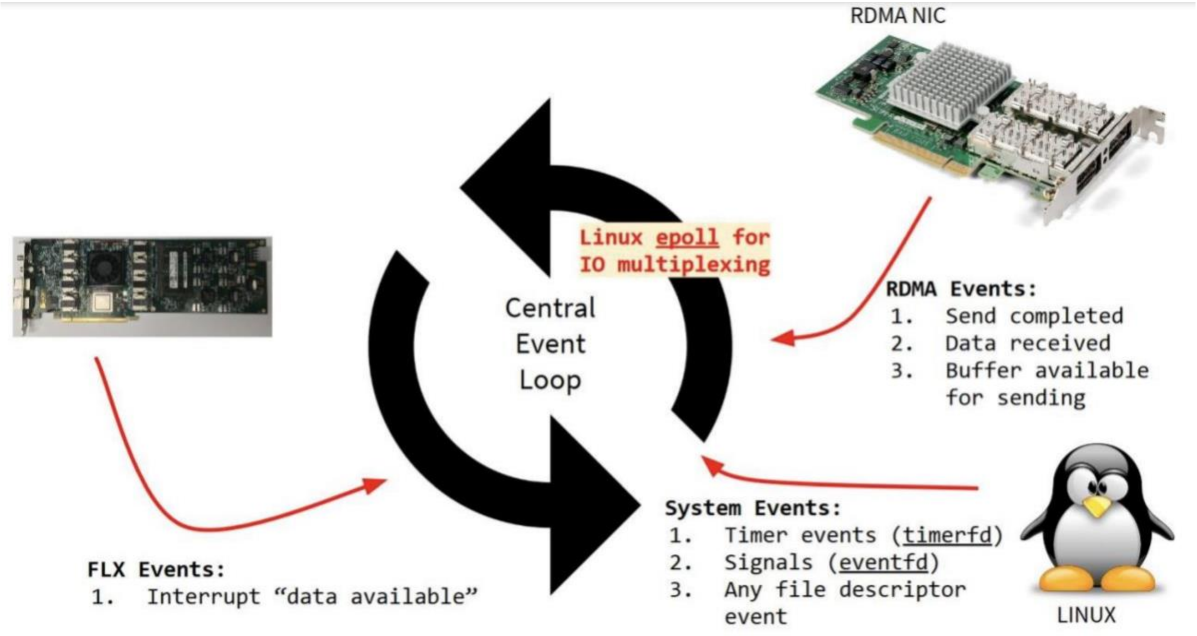

Picture of FLX-712




Block diagram of FLX-712 firmware

# FELIX Software

- Each FELIX server hosts up to two FELIX cards and one NIC.
- Low level software has been developed for basic configuration and monitoring.
- High level software has been developed for data rate and channel monitoring.




FELIX software development

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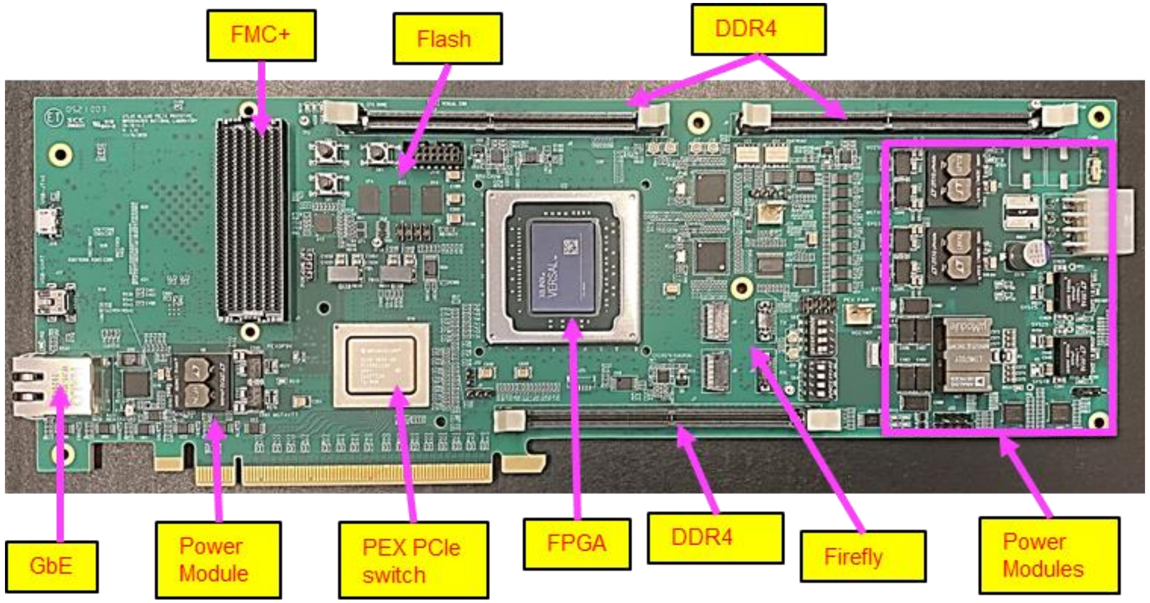
# FELIX for ATLAS Phase-2 Upgrade

FPGA: Xilinx Versal XCVM1802

- High speed optical links
  - 12 x FE-Links: 1 pair of Samtec Firefly 25Gb/s 12-ch modules
  - 16 GTY links @ 25Gb/s on FMC+
- Dual PCIe Gen4 x 8, up to 256 GT/s
  - 16 x GTY links
- 3 x Mini-UDIMM DDR4 Modules
  - Accessible by both PL and PS through NoC
- FMC+ mezzanine card
  - 34 x differential pairs from XPIO banks
  - 16 x GTY links
- Peripherals:
  - Micro SD 3.0 and QSPI flash for system boot
  - USB - I2C/UART
  - GbE RJ45




Picture of assembled FLX-181

# Status of FLX-181

Hardware

- Three boards have been produced for firmware development
  - One is being used for ATLAS firmware development at Nikhef
  - One is being used for DUNE firmware development at CERN
  - One is kept at BNL for hardware and firmware development

Firmware

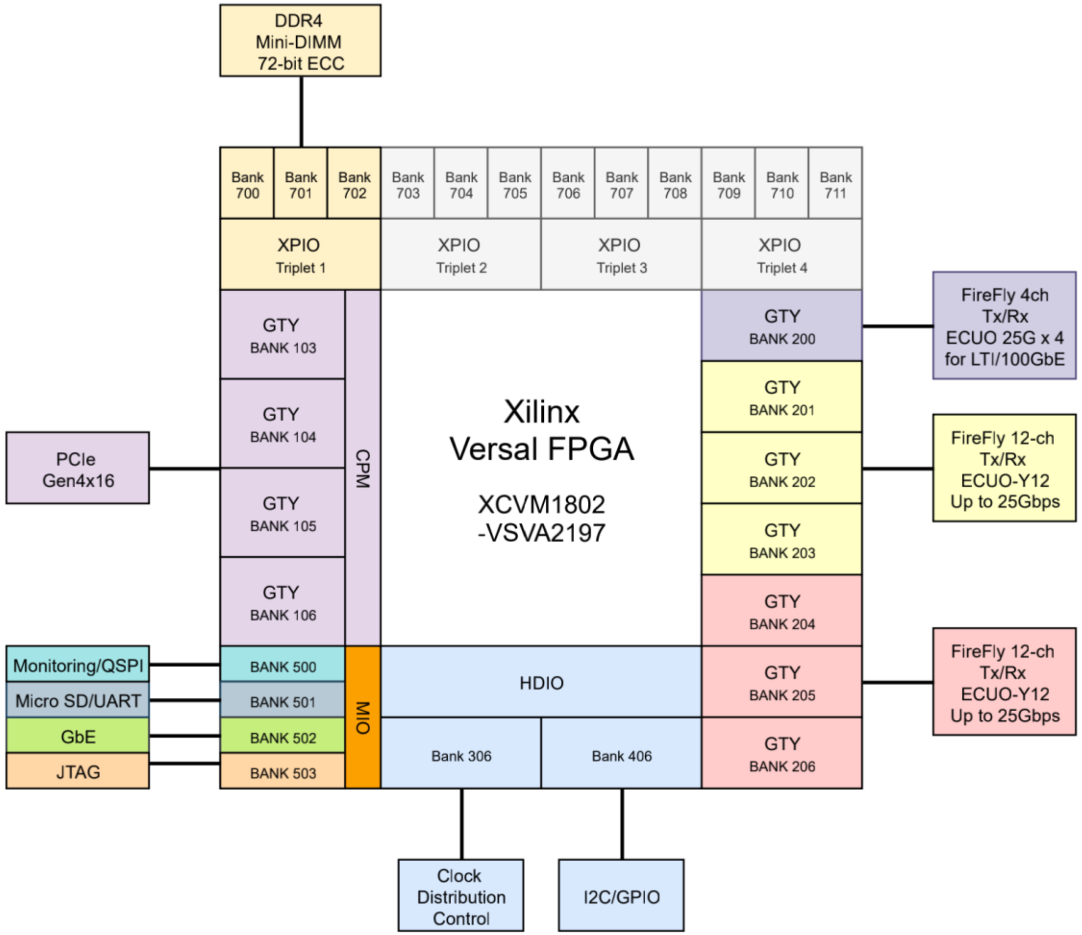
- PCIe Gen4x16 has been developed
- 24 channel GBT mode is being implemented

Photo of FLX-181 with 25Gbps FireFly FMC+

# Revision for FELIX Prototype

Make the board to be a design toward 24-ch FELIX production, to meet all known requirements

- Main features of FLX-182:
  - XCVM1802 production chip
  - PCIe Gen 4x16
  - 24 FireFly links w/ 3 optional configurations
    - 24 links @25Gbps
    - 24 links @10Gbps
    - 12 links @25Gbps + 12 links @10Gbps
  - 100GbE or LTI interface
  - 1 DDR4 Mini-UDIMM
  - 1 GbE




Block diagram of FPGA functionalities on FLX-182

# Development Plan

- FLX-182
  - Schematics design is done. Layout design will be finished by March 2022.
  - FLX-182 will be available in summer 2022 for firmware development.

- 48-ch FELIX
  - FPGA: Versal Premium
  - Transceivers: Up to 100+ GTYP/GTM
  - PCIe Gen 5 up to 16 lanes
  - Design will start in Q4 of 2022, first board is expected to be available in Q3 2023.

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# ATLAS TDAQ for HL-LHC

- Trigger rate: 1 MHz
- Data rate: 5.2 TB/s
- 17093 optical links from detectors

FELIX:

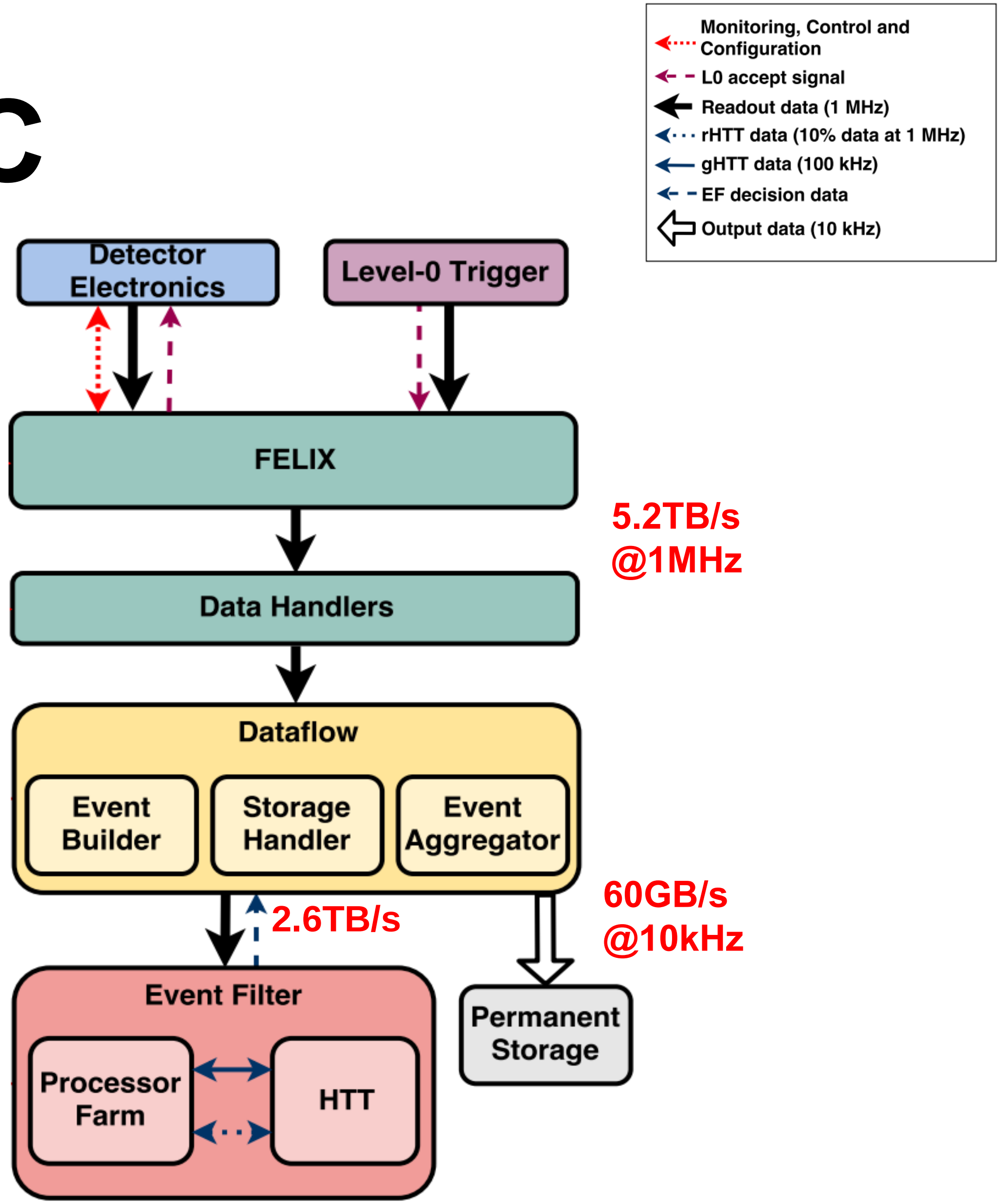
- 545 FLX cards for HL-LHC
- Distribute trigger & command signals to the Front-Ends
- Transmits the full detector data up to the Data Handlers

Data Handlers:

- Receives the data from FELIX servers over the network at 1 MHz
- Performs data formatting and send data fragments to the Dataflow system

Dataflow:

- **Event Builder** builds event records and manages the storage volume of the Storage Handler system
- **Storage Handler** buffers event data before and during processing by the Event Filter
- **Event Aggregator** collects, formats and transfers the output to CERN permanent storage

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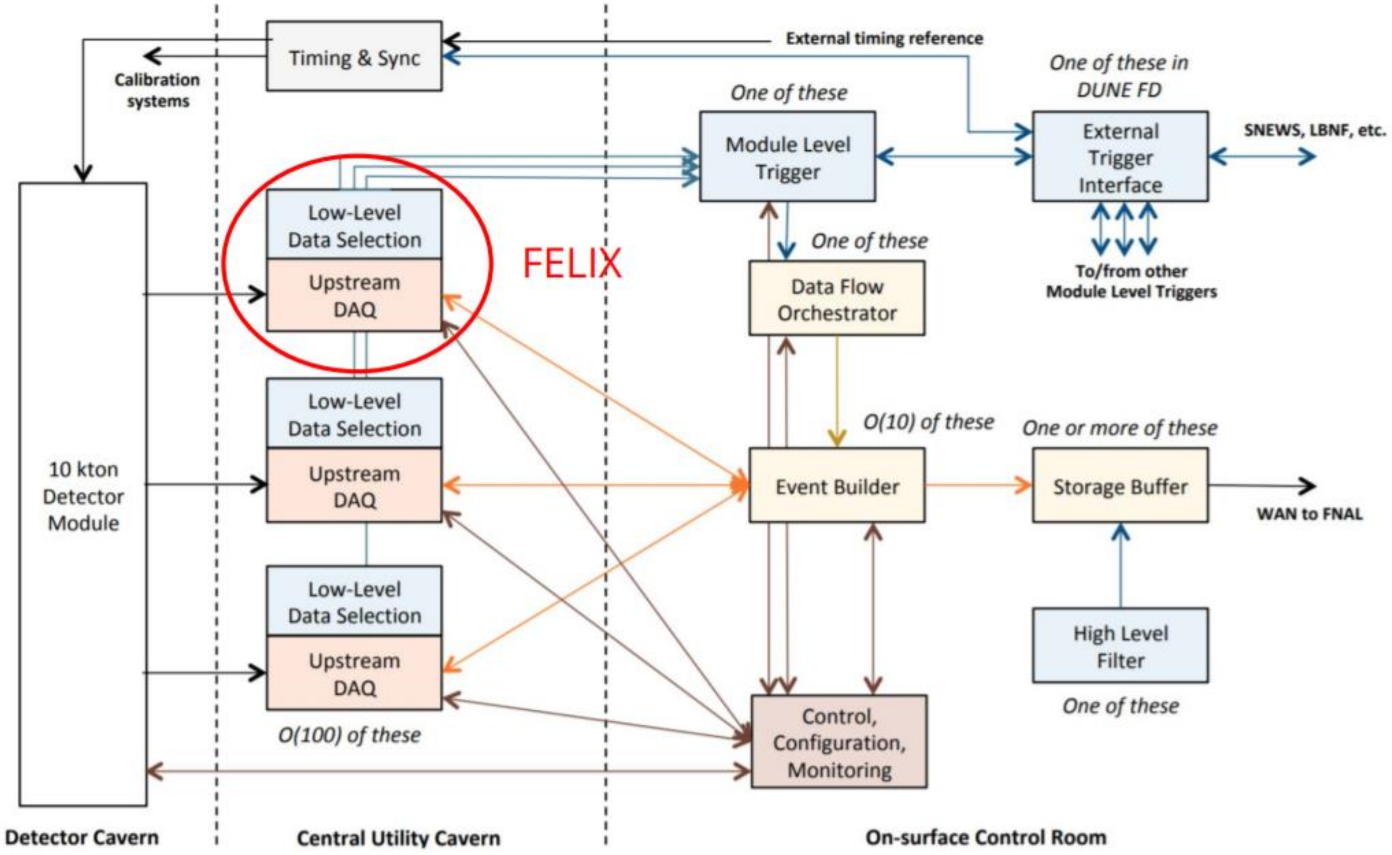
# DUNE DAQ




FELIX has been successfully used in the application framework of ProtoDUNE DAQ, to be further developed for DUNE DAQ

- ~11.3Tb/s data streaming via 1,500 fibers per 10kton SP module (384k ADC channels)
- Supernova Burst trigger
  - 10s transient buffer (15TB for one detector super module)
  - On trigger: 100s continuously persisted data stream (150TB)

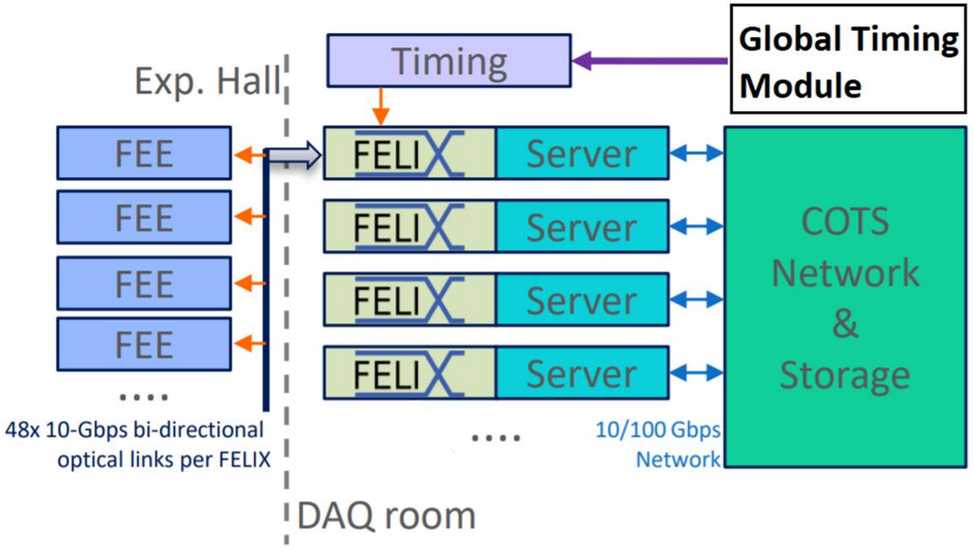
# sPHENIX Streaming DAQ

- All three sPHENIX tracking detectors use streaming readout
- Completed construction of sPHENIX FELIX DAQ interface (~50)

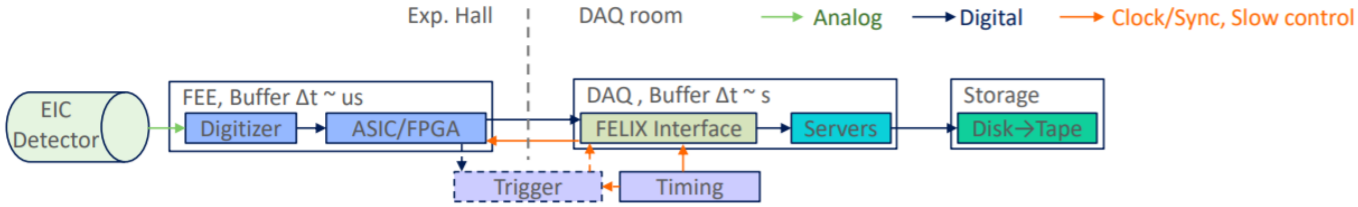
MVTX RU

INTT ROC

TPC FEE




Architecture of sPHENIX streaming DAQ




Data Flow

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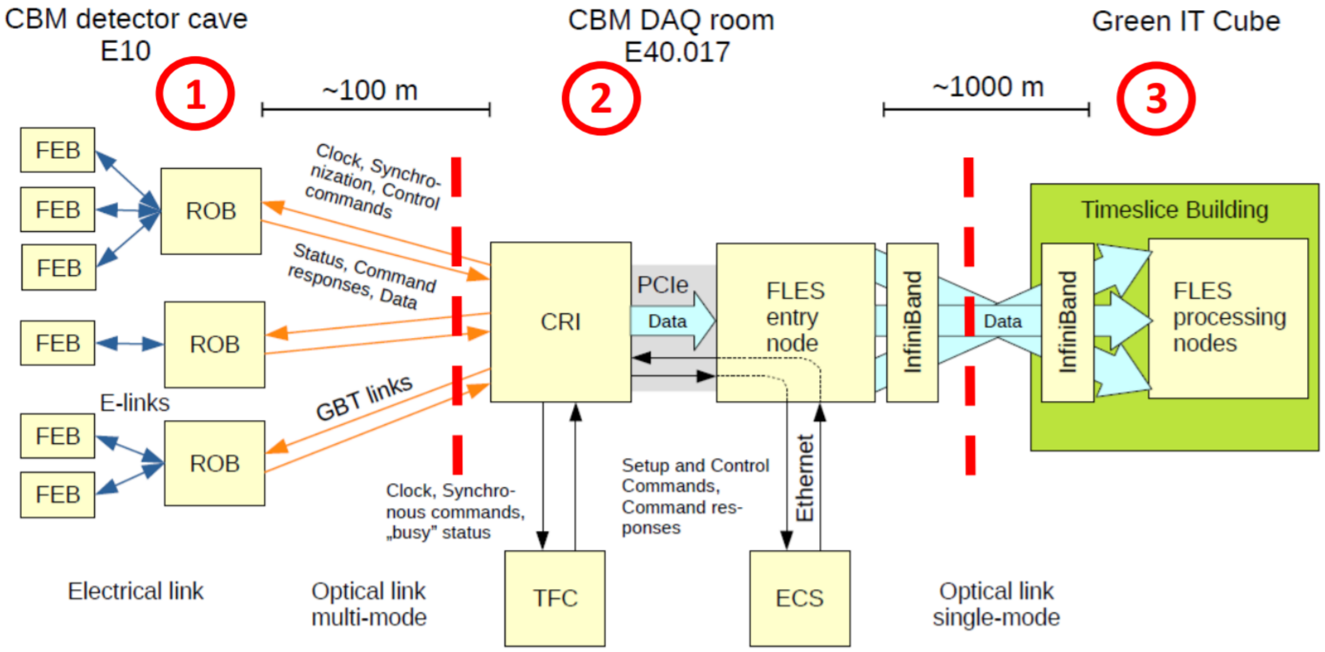
# CBM Readout System




The CBM readout and control architecture
*from David Emschermann's slides on Dec. 8th.

FELIX is used as CRI1 to send the data to FLES

https://indico.phy.ornl.gov/event/112/contributions/566/attachments/492/1342/20211208_169_sro9_cbm_daq_v02.pdf

**The readout system of the CBM experiment**

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

David Emschermann
Workshop IX on Streaming Readout
ORNL – Zoom – 08. December 2021

CBM

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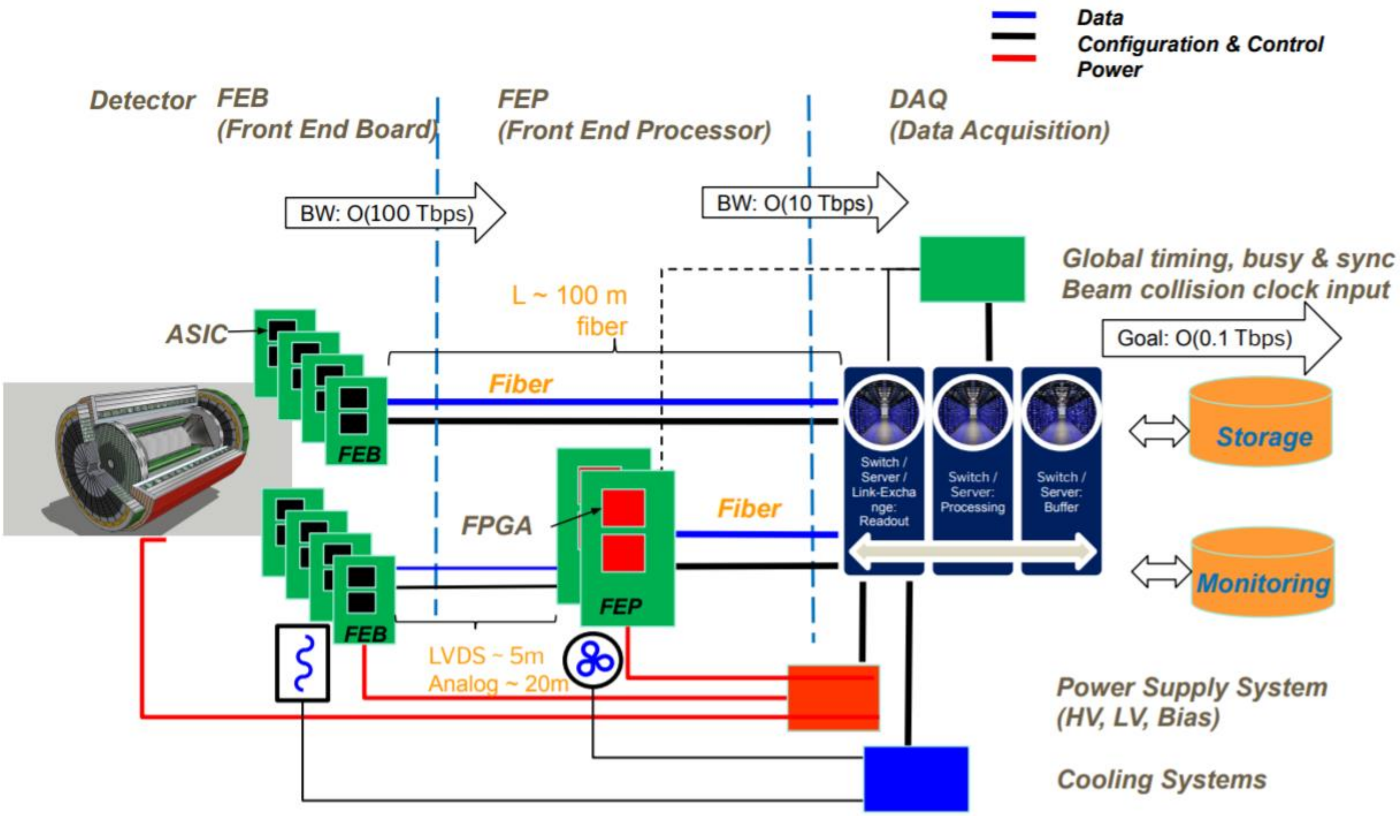
# EIC Streaming DAQ

- Triggerless readout front-end (buffer length : μs)

- DAQ interface to commodity computing (e.g. FELIX). Background filter if excessive background rate

- Disk/tape storage of streaming time-framed zero-suppressed raw data (buffer length : s)

FELIX can meet the requirements of EIC streaming DAQ




EIC streaming readout architecture